Pre-Conference Seminar C: New Challenges in SSD Controller Design

This seminar will describe new challenges in designing SSD controllers. The following topics will be covered:

- Ethernet Storage. Speaker: Rob Davis, Nvidia
- Computational Storage. Speaker: Pankaj Mehra, Elephance
- Flash Translation Layer concepts for TLC and QLC NAND Flash. Speaker: Roman Pletka, IBM Zurich Research
- Error Correction, Signal Processing and Error Recovery Techniques for TLC and QLC NAND Flash. Speaker: Jeff Yang, Silicon Motion

This seminar is intended for engineers who want to learn the latest concepts for designing SSD controllers. This seminar is also useful for engineers who plan to integrate SSD controllers in solid state disks for data center applications and new use centers such as Computational or Ethernet Storage.

Speakers:

Rob Davis is the Vice President of Storage Technology at the NVIDIA Networking Platform Group where he focuses on ways to apply high-speed interface technology to storage systems. He came to NVIDIA through the Mellanox acquisition. As technology leader and visionary for more than 35 years, he has been a key evaluator and decision maker for the development of storage networking products. He is currently leading the development and marketing of products based on NVMe over fabrics, which will allow for the high-speed networking of PCIe-based storage. Davis was previously Vice President and Chief Technology Officer at QLogic, where for 15 years he drove development and marketing of Fibre Channel, Ethernet and InfiniBand technology into new markets such as blade servers. Prior to QLogic, Davis spent 20 years at Ancor Communications, which QLogic acquired in 2000. At Ancor, Davis served as Vice President of Advanced Development, Director of Technical Marketing, and Director of Engineering. He drove development and marketing of their Fibre Channel products in the early 90s and their InfiniBand products in the late 90s. Davis' in-depth expertise spans Virtualization, Ethernet, Fibre Channel, SCSI, iSCSI, InfiniBand, RoCE, SAS, PCI, PM, SATA, and Flash Storage.

Pankaj Mehra is Founder of Elephance, a company developing powerful new software concepts for disaggregated memory. Pankaj has held executive positions in the Memory industry since 2013 when he took over as CTO of Fusion-io, later serving as VP and Senior Fellow at both acquirers SanDisk and Western Digital. He became an HP Distinguished Technologist in 2004 for his pioneering work on RDMA-attached persistent memory devices and filesystems. Later he founded HP Labs Russia and served as its Chief Scientist until 2010. Pankaj's international experience spans academia, industry and government. His publications include 3 books and

over 100 papers and patents. Pankaj holds Ph.D. in Computer Science from The University of Illinois at Urbana-Champaign.

Roman Pletka is a research staff member and master inventor for cloud storage, data, and AI systems at the IBM Zurich Research Laboratory where he focuses on non-volatile memory technologies in storage systems. He is a frequent speaker at international conferences, has published over 20 articles and obtained more than 100 patents in managing non-volatile memories, security, scalability, and availability of distributed storage systems as well as quality-of-service in high-speed networks, active networks, and network processors. He has made presentations at many international conferences including the ACM International Conference on Systems and Storage (SYSTOR) and the Nonvolatile Memory Workshop. He has over 17 years' experience in storage systems research. He earned a PhD in computer networking from ETH Zurich, Switzerland and an MS in the same subject from EPFL (Swiss Federal Institute of Technology of Lausanne).

Jeff Yang is a Principal Engineer of Algorithm & Technology team at Silicon Motion. Prior to Silicon Motion, he has worked with Realtek Inc. on several WiFi projects. He holds He holds a M.S.E.E. from National Taiwan University, Taiwan. His research in error correcting codes addresses effective encoding/decoding algorithms and VLSI architectures. His current research interests include error correcting codes system for NAND flash applications.

Session Organizer:

Erich Haratsch is Senior Director Architecture at Marvell, where he leads the architecture definition for Bravera™ SSD controllers and other memory-based products. Prior to joining Marvell, he worked at Seagate and LSI, where he worked on Nytro® and SandForce® branded SSD controllers. Earlier in his career, he developed signal processing and error correction technologies for multiple generations of HDD controllers at LSI and Agere Systems. He started his career at AT&T and Lucent Bell Labs, where he worked on Gigabit Ethernet over copper, optical communications and the MPEG-4 video standard. He is the author of over 40 peer-reviewed journal and conference papers, and holds more than 200 U.S. patents. He also is a Senior Member of IEEE, and earned his MS and PhD degrees from the Technical University of Munich (Germany).