GEORGE AND ANGELIKI PERLEGOS CHARITABLE TRUST

Contacts Nancy B. Green
The William Baldwin Group
+1 650 856 6192
nbgreen@william-baldwin.com

John Bryant
George and Angeliki Perlegos Charitable Trust
+1 408 857 7312
jbryant@brianti.com

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SEMICONDUCTOR PIONEER GEORGE PERLEGOS HONORED WITH LIFETIME ACHIEVEMENT AWARD

10th Anniversary of the iPhone Marks IC Memory Innovations that Fostered the Development of Smartphones, Self-driving Cars and the Internet of Things

SANTA CLARA, CA, August 8, 2017– The Flash Memory Summit today granted its 2017 Lifetime Achievement Award to George Perlegos, founder of three successful semiconductor firms, for a portfolio of IC memory innovations that have contributed to the development of virtually every leading edge electronic product on the market today. Mr. Perlegos' contributions include:

N-MOS EPROM N-MOS EPROM (Intel (INTC), 1974). Gordon Moore said the erasable programmable read only memory (EPROM) was "**as important in the development of the microcomputer industry as the microprocessor itself."** [1] From computers to pacemakers, the processors that power them need programs to tell them what to do. In the old days programs were stored on large expensive external disks. In 1970 Dov Frohman developed the first EPROM (Intel 1702) using a *P-MOS floating (unconnected) gate structure*. In 1974 Mr. Perlegos designed the Intel 2708 N-MOS EPROM based on a new process that used *channel injection* and a *single dual layer polysilicon cell* to create a dense, fast access non-volatile memory. The device did not require power to maintain its contents and could be easily erased for reprogramming by shining UV light through a window on the package. When paired with the Intel 8080, the first commercially successful integrated processor, low-cost, low-volume systems became feasible.

[1] *A Revolution in Progress: A History of Intel to Date*, (Intel Corporation, 1984), p. 22.

Electronic system design migrated from the assembly of a myriad of hardware-only components to the use of software as the core of the design. This development constituted the dawn of the embedded computing era. (ISSCC, Feb 18, 1977. Patent 3,938,108, filed Feb 3 1975)

+5 volt only EPROM (Intel, (INTC) 1976) - Early EPROMs required 3 different voltages to operate (-5V, +5V and +12V), necessitating an array of external power supplies. Mr. Perlegos exploited a *self-aligned polysilicon gate structure* and *ion implantation in the channel* to enhance channel injection, enabling single 5V operation. Intel's 5 volt 2716 eliminated the need for the extra components, reducing both the size and cost of end-products. System design was simplified, and battery powered products became a realistic possibility.

16-Kbit EEPROM with single-byte erasure, 10,000 read/write cycles. (Intel, 1978) - Previous non-volatile data storage memories were small (<1Kbits) and could be erased and re-programmed only a few times. Building on work done by Dawon Kahng (Bell Labs, Patent 3500142) Mr. Perlegos utilized *two-layer poly stack-gate technology* and *very thin oxide (<100A) tunneling* for both program and erase to create Intel's 16 Kbit 2816, non-volatile data memory. For the first time single bytes could be changed without having to erase and re-program large memory blocks, and with an endurance of 10,000 erase/write cycles local data storage no longer needed battery back-up. In addition, with the elimination of the UV light erase requirement, the device package could be made smaller and the device could be erased in-situ. Henceforth portable electronic systems could update themselves in the field which greatly simplified and accelerated the growth of electronic portable devices. (Patent 4,203158. Continuation of Feb 24, 1978. ISSCC, Feb, 1980. Patent 4,266,283, Feb 16, 1979.) (Figures 1, 2, 3)

5-volt in-system programmable/erasable EEPROM (SEEQ, 1981). First generation EEPROMs required high voltage (+12V) pulses to erase/program necessitating the addition of an additional power supply in system. At SEEQ Technologies, Mr. Perlegos utilized *oxynitride dielectrics and an integrated voltage multiplier* to eliminate the need for the external 12V supply and support the *tunnel programming* from a single +5 volt supply. These advances simplified system design and reduced programming power requirements to reduce battery size and costs. They remain in use

today, throughout the flash memory industry, in virtually every embedded control system (smart phones, laptops, cars, IoT devices, etc.). (ISSCC Feb 11, 1982) (Figure 4)

First 5-V Only NOR flash memory. (Atmel, 1988). Although EPROMs were low cost they could not be erased and reprogrammed in-system. EEPROMs allowed in-system changes but were expensive. Mr. Perlegos used proven *tunneling erase/program technology* to introduce the first 5V only Flash memory which allowed large blocks to be erased at once, providing a solution for the nascent cell phone market. With the capability to change the program code remotely Flash memory allowed the early cell phone makers to update their products after shipment which accommodated the evolving standards.

World's first flash microcontroller. (Atmel, 1994) Under Mr. Perlegos' leadership, and employing many of the previously mentioned innovations, Atmel combined its Flash memory process with a CMOS logic process to produce the first Flash based microcontroller (MCU), the 89C51. By separating the program and data storage memories, the 89C51 allowed remote updates in-situ while maintaining permanent data storage. To take full advantage of the capabilities of on chip Flash and EEPROM memory, the Atmel team optimized a new microcontroller architecture (AVR™) to produce a next generation capability of embedded intelligence. Integrating the Flash based MCU with specific peripheral circuits has led to low cost single chip solutions for a growing universe of embedded systems which continues today with the IOT industry. (Patents 5493534, 1999 and 6032248, 1998) (Figure 5)

In 2000, seven years before the existence of the smart phone, Mr. Perlegos predicted, "You'll want your phone to do everything. You'll want to see a picture on your phone someday and you'll want to look at the stock market and be able to buy something. And what everyone wants to be able to do is E-commerce, which means images [and security]. As we bring images to phones you'll need a camera. . . . You'll be able to scan your finger and it will recognize you and turn your cell phone on. Nobody else [will be able to] open it" (World Report Silicon Valley, 28, October 2000)

Smartphones would not employ commercially viable fingerprint authentication until 2013. E-commerce was nascent; Amazon's U.S retail market share was less than 1/10% Today it is over 5%.

Cell phones were flip phones that ONLY made calls and sent texts - no pictures, no Internet, no e-commerce, no security.

According to Alan Niebel, 22 year Flash veteran and CEO of WebFeet Research, "On the 10th anniversary of the iPhone, it's appropriate to credit the technologies that made smartphones possible. George Perlegos' vision, hard work, and technical acumen contributed directly and substantially to the way we live today, and the way we will live in the future. The explosion of the Internet of Things is another example. Many of those "things" that are controlled using the Internet are based on self-programming Flash MCUs, one of George's patents. That allows them to sense, take action, communicate and take instructions via the Internet."

Today, Mr. Perlegos is thinking about the next 20 years of innovation in technology and medical research.

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About George Perlegos.
George Perlegos is trustee of the George and Angeliki Perlegos Charitable Trust, which provides grants to promote scientific advances toward the treatment and cure of progressive diseases such as IgA nephropathy and degenerative diseases (Parkinson's, ALS, MS, etc), and to promote research in technology directions. He is also Chairman of the Perlegos Capital Management LP investment group. He attended San Jose State University (BSE,1972) and Stanford University (MSE, 1975. He resides in Fremont, CA.

Mr. Perlegos founded three successful semiconductor companies: SEEQ Technologies (1974), Chips and Technology (1984), and Atmel (1984). Atmel was acquired by Microchip (MCHP) in 2016.) Mr. Perlegos holds 16 patents for innovations in memory technology and device physics. http://patents.justia.com/inventor/george-perlegos

Relevant technical papers on the technologies are available below:

A 16Kb electrically erasable nonvolatile memory http://ieeexplore.ieee.org/document/1156030/

A 5V-only 16K EEPROM utilizing oxynitride dielectrics and EPROM redundancy
http://ieeexplore.ieee.org/document/1156369/

High performance, MOS EPROMs using a stacked-gate cell
http://ieeexplore.ieee.org/document/1155707/

The Computer History Museum has compiled Mr. Perlegos' oral history of his contributions to non-volatile memory and embedded technology at:
(http://archive.computerhistory.org/resources/access/text/2013/11/102746703-05-01-acc.pdf)

Additional quotes and background information are available from the Flash Memory Summit:

https://www.flashmemorysummit.com/English/News_Info/Lifetime_Achievement_Award_2017.html

About the George and Angeliki Perlegos Charitable Trust.
The George and Angeliki Perlegos Charitable Trust, located in Fremont, CA, provides grants to promote scientific advances toward the treatment and cure of progressive diseases such as IgA nephropathy and degenerative diseases (Parkinson's, ALS, MS, etc), and to promote research in technology directions.

About the Flash Memory Summit.
Flash Memory Summit, produced by Conference Concepts, showcases the mainstream applications, key technologies, and leading vendors that are driving the multi-billion dollar non-volatile memory and SSD markets. FMS is now the world's largest event featuring the trends, innovations, and influencers driving the adoption of flash memory in demanding enterprise storage applications, as well as in smartphones, tablets, and mobile and embedded systems. Information is available at http:/www/FlashMemorySummit.com.

GLOSSARY

George Perlegos Lifetime Award - August 8, 2017

MOS-FET: Metal-Oxide-Semiconductor Field-Effect-Transistor. MOS-FETs are the most common type of transistors in use in integrated circuits. The transistor has three electrodes (source, drain and gate). The source and drain are connected to regions in the (Silicon) substrate that have been "doped" with impurities that cause the source and drain to have different current carrying characteristics from the substrate. Thus, applying a voltage differential between the source and drain will not cause current flow between them. The substrate between the source and drain is called the channel. The channel is covered by an insulator which is, in turn, covered by the gate. By applying sufficient voltage to the gate, current can be made to flow from source to drain in the substrate. Hence, the device acts like a switch with current flow determined by the gate voltage.

***N-MOS versus P-MOS*:** The first IC developments used P-MOS (the source and drain are doped to be P-type and the substrate is doped to be N-type). Later, to achieve faster operation with lower voltages the industry changed to N-MOS (the source and drain are doped to be N-type and the substrate is doped to be P-type).

Floating (unconnected) Gate Structure: By encasing the gate with an insulator the gate will be unconnected to any conductor (floating in the insulator). If a charge is placed on the floating gate the charge will stay there until enough energy is injected into the device to cause the charge to dissipate. When the gate is charged the resulting electric field will affect the current flow in the channel below. Consequently, the transistor is a non-volatile memory element that will retain its programmed state without having to be powered. Studies have shown that floating gate structures can retain their charge for many years.

Single Dual Layer Polysilicon Cell: Adding another gate conductor on top of the insulator covering the floating gate creates a dual layer gate structure. The top gate controls current flow in the channel below it by adding to or subtracting from the electric field created by the charge that is trapped in the floating gate. The material used for the floating gate and the top gate is poly-crystalline silicon (polysilicon).

Channel Injection: In order to "inject" charge onto the floating gate, high energy electrons must be present in the vicinity. By putting a voltage differential on the source and drain and supplying sufficient voltage to the top gate, a high energy current can be made to flow in the channel. Some of the electrons that are flowing in the channel will gain sufficient energy to escape from the substrate and make their way to the floating gate. Once there, they lack sufficient energy to escape and are hence "trapped" there. Eventually the trapped charge will build to the point that the device is considered to be programmed.

UV-Erase: In order to remove the trapped charge from the floating gate, enough energy must be injected to give the electrons sufficient energy to escape. One method to do that is to shine a bright ultra-violet light onto the chip. The trapped electrons on the floating gate will absorb energy from the light to the point that they escape and hence erase the memory.

ION Implantation. Adding specific impurities to the silicon substrate will cause its electrical behavior to change in a controlled way, called doping. One method of adding the impurity is using very high temperatures to cause the impurity to diffuse into the silicon. Another method (called ion implantation) is to inject the impurity directly into the silicon by use of a high energy ion accelerator.

ION Implantation in the Channel: The voltage required on the gate to cause the channel to conduct current can be adjusted by adding specific impurities to the channel area.

Self-Aligned Polysilicon Gate Structure: In semiconductor manufacturing the polysilicon gates are placed on the substrate first and etched to their final shape. Then they are used as a mask for ion implantation of the source/drain below. As a result the edges of the source/drain will be directly under the edges of the gate with little overlap.

Very Thin Oxide (<100A) Tunneling. Although silicon dioxide is an excellent insulator, electrons can be made to flow through the oxide in the presence of a high electric field. This effect is called field electron emission or Fowler-Nordheim Tunneling. By purposely overlapping a portion of the source with the floating gate and making the insulator oxide between them very thin (<100A), a Fowler-Nordheim tunneling current flow will be achieved when a sufficient voltage differential is applied to the source and the top gate. In this way, the trapped electrons on the floating gate can escape and the gate will be erased without the use of UV light.

Oxynitride Dielectrics*:* Mixing nitrogen into the oxygen used to form the insulator over the channel results in an insulator that allows lower operating voltages (5V), while not breaking down when subjected to the higher program/erase voltages (>10 volts).

Integrated Voltage Multiplier. The program/erase operations of floating gate structures require high voltages (>10 volts). By charging chip capacitors (in parallel) and discharging them (in series), higher voltages can be achieved from the single external 5V (or 3V) supply. The on-chip circuit that performs this task is called a charge pump or voltage multiplier.

Figure 1- EEPROM cell data cycling to 10000 times and its threshold after Tunneling both positive and negative 110277

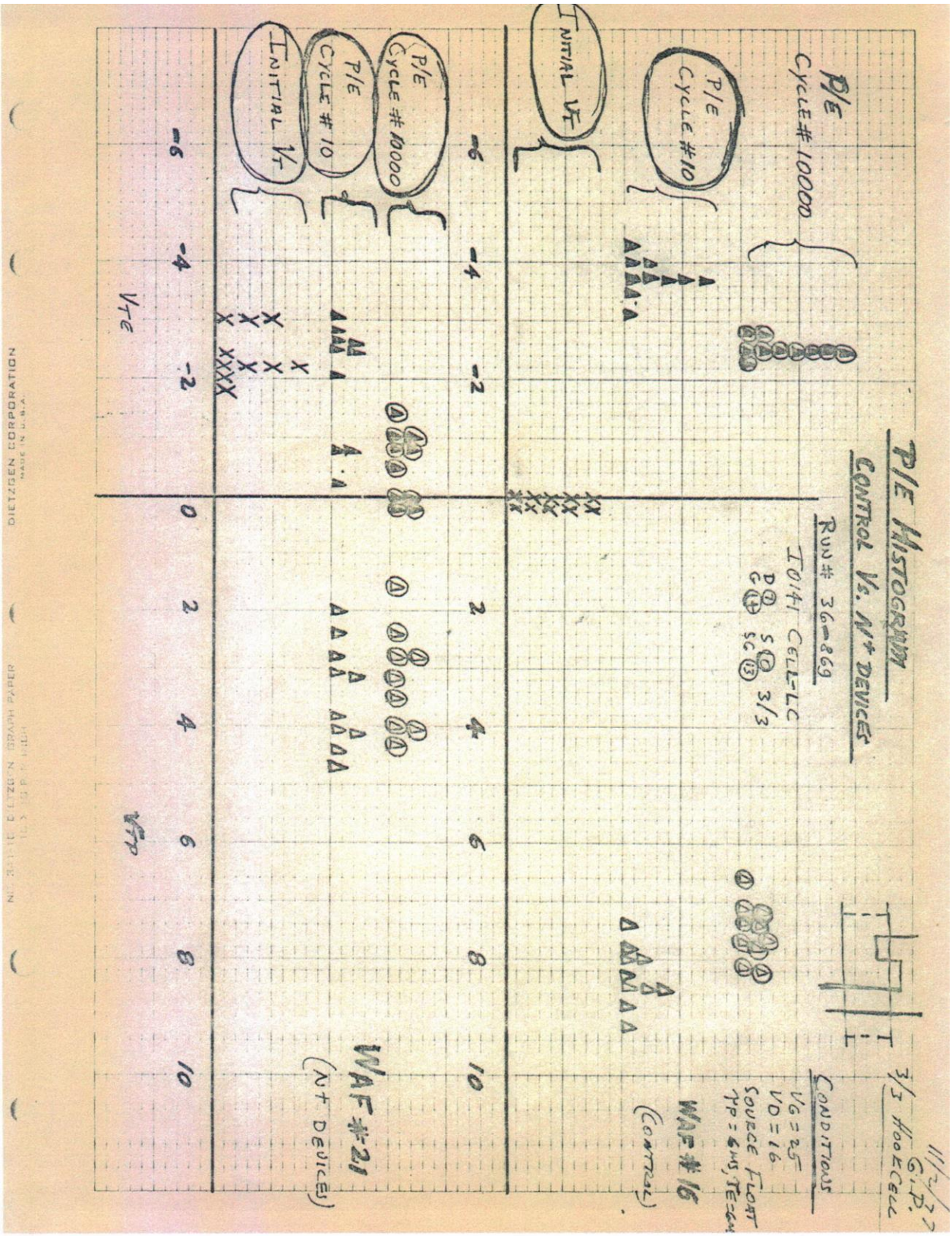
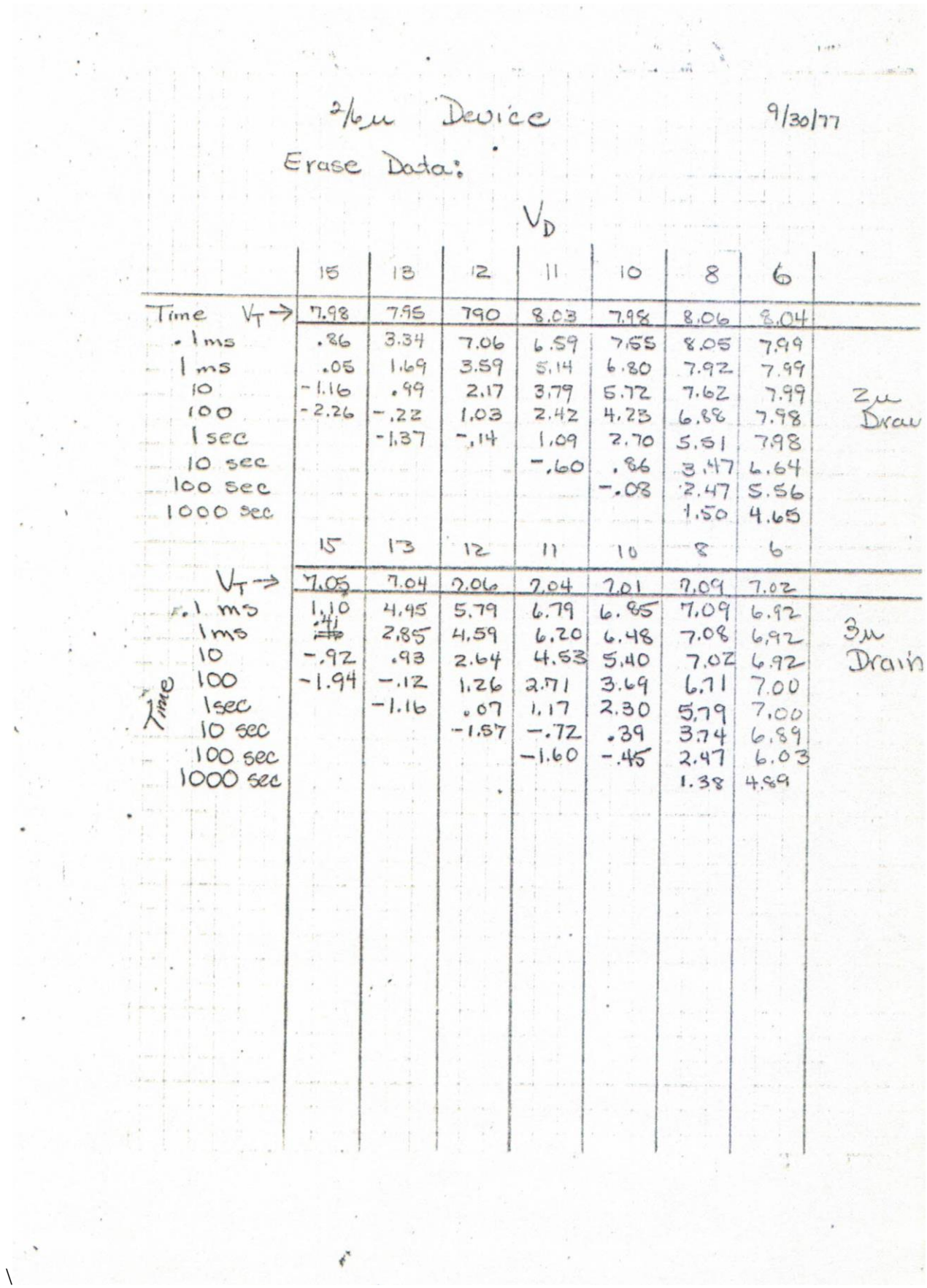


Figure 2-EEPROM cell data with Tunneling as a function of time, Drain voltage, and area



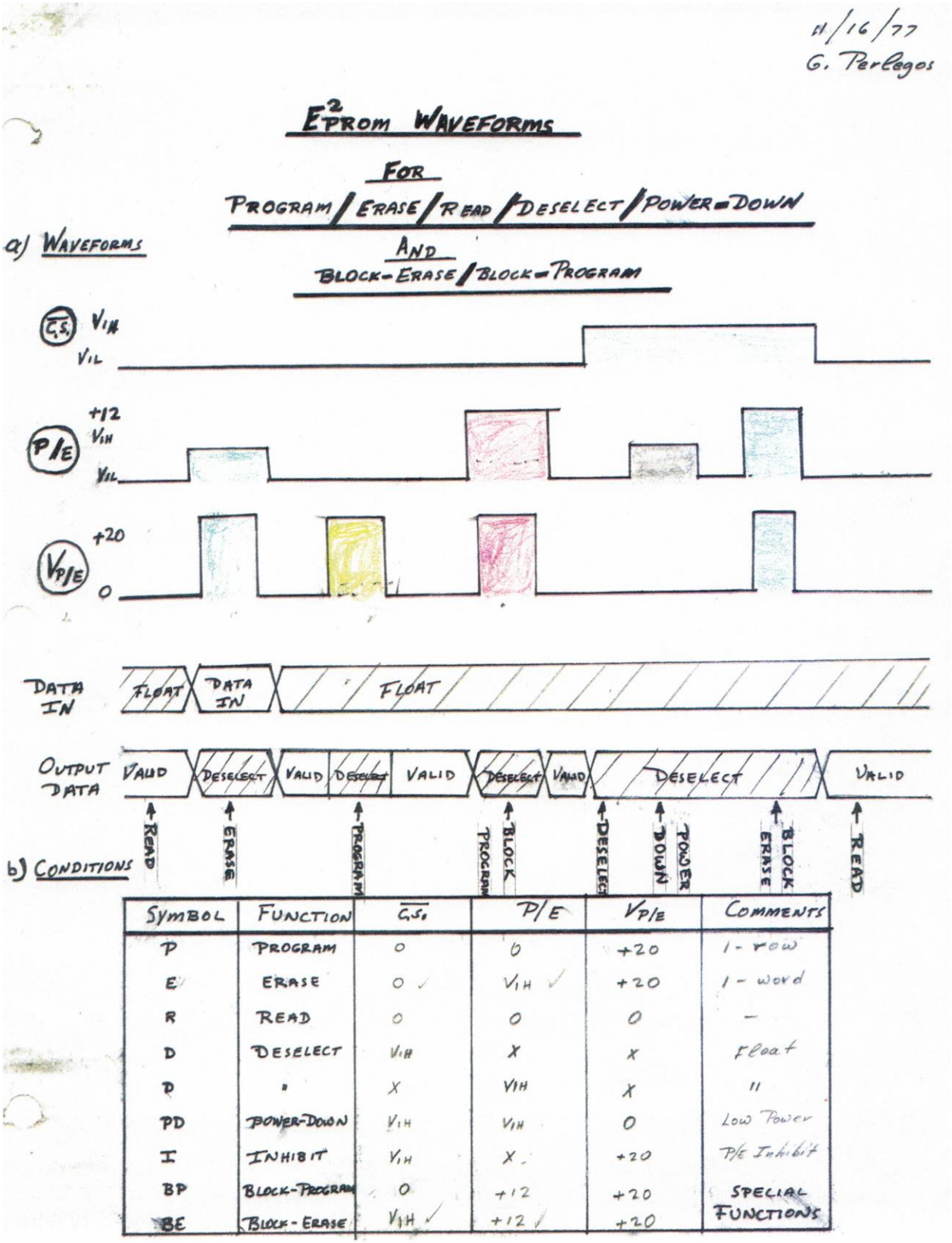
2/6μ Device 9/30/77

Erase Data:

V_D

Time V_T →	15	13	12	11	10	8	6	
	7.98	7.95	7.90	8.03	7.98	8.06	8.04	
.1ms	.86	3.34	7.06	6.59	7.55	8.05	7.99	
1ms	.05	1.69	3.59	5.14	6.80	7.92	7.99	
10	-1.16	.99	2.17	3.79	5.72	7.62	7.99	2μ Drain
100	-2.26	-.22	1.03	2.42	4.23	6.88	7.98	
1 sec		-1.37	-.14	1.09	2.70	5.51	7.98	
10 sec				-.60	.86	3.47	6.64	
100 sec					-.08	2.47	5.56	
1000 sec						1.50	4.65	
	15	13	12	11	10	8	6	
V_T →	7.05	7.04	2.06	7.04	7.01	7.09	7.02	
.1 ms	1.10	4.45	5.79	6.79	6.85	7.09	6.92	
1ms	~~.41~~	2.85	4.59	6.20	6.48	7.08	6.92	3μ Drain
10	-.92	.93	2.64	4.53	5.40	7.02	6.92	
Time 100	-1.94	-.12	1.26	2.71	3.69	6.71	7.00	
1sec		-1.16	.07	1.17	2.30	5.79	7.00	
10 sec			-1.57	-.72	.39	3.74	6.89	
100 sec				-1.60	-.45	2.47	6.03	
1000 sec						1.38	4.89	

Figure 3-EEPROM 2816 Target spec defining for the first time how an EEPROM device will operate as a memory to read and write 8 bit words plus other functions



SYMBOL	FUNCTION	$\overline{C.S.}$	P/E	$V_{P/E}$	COMMENTS
P	PROGRAM	0	0	+20	1 - row
E	ERASE	0	V_{IH}	+20	1 - word
R	READ	0	0	0	–
D	DESELECT	V_{IH}	X	X	float
D	"	X	V_{IH}	X	"
PD	POWER-DOWN	V_{IH}	V_{IH}	0	Low Power
I	INHIBIT	V_{IH}	X	+20	P/E Inhibit
BP	BLOCK-PROGRAM	0	+12	+20	SPECIAL FUNCTIONS
BE	BLOCK-ERASE	V_{IH}	+12	+20	