Flash Memory SUMMIT

NAND and NOR Convergence

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Datalight
Software for Trustworthy Data on Successful Devices

In the Beginning, There Was NOR

- Similar interface to RAM meant easy integration

NOR Attributes

- Ships with all blocks known “good”
- High erase counts for long life in the field
- Code executes directly from within NOR chip, not requiring loading to RAM
- Offers fast boot times by jumping directly to an OS stored in NOR and booting
- …but cost per bit is high

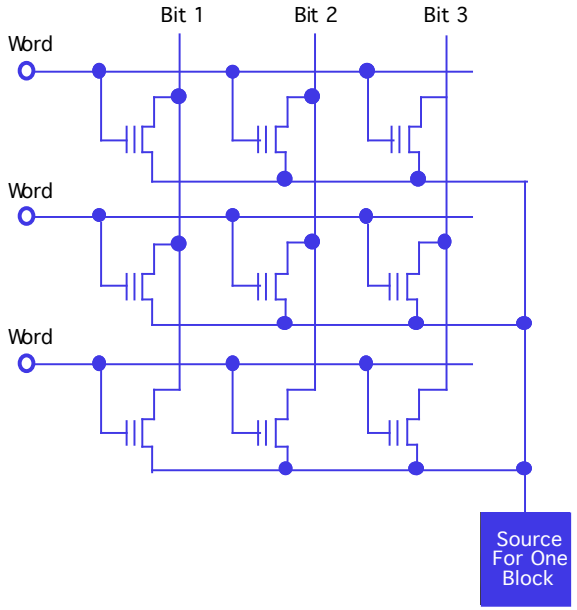
Along Came NAND

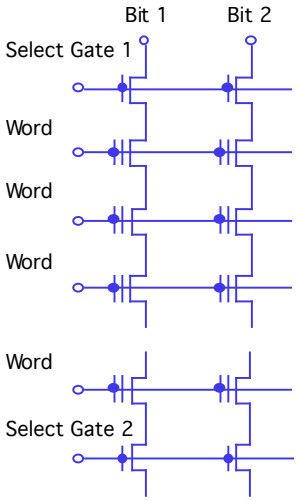
- Evolved from byte-addressable EEPROM
- Low cost per bit
- Available in high densities, fast write access -- ideal for data storage devices
- Bit read errors occur, read back a page with one or more bits different than they were programmed
- Though all flash have limited erase cycles typically NAND has lower erase cycle count than NOR
  - increases necessity for wear leveling operations
- Manufacturing considerations

Cell Organization is Different

NOR cell organization allows for individual access to each cell

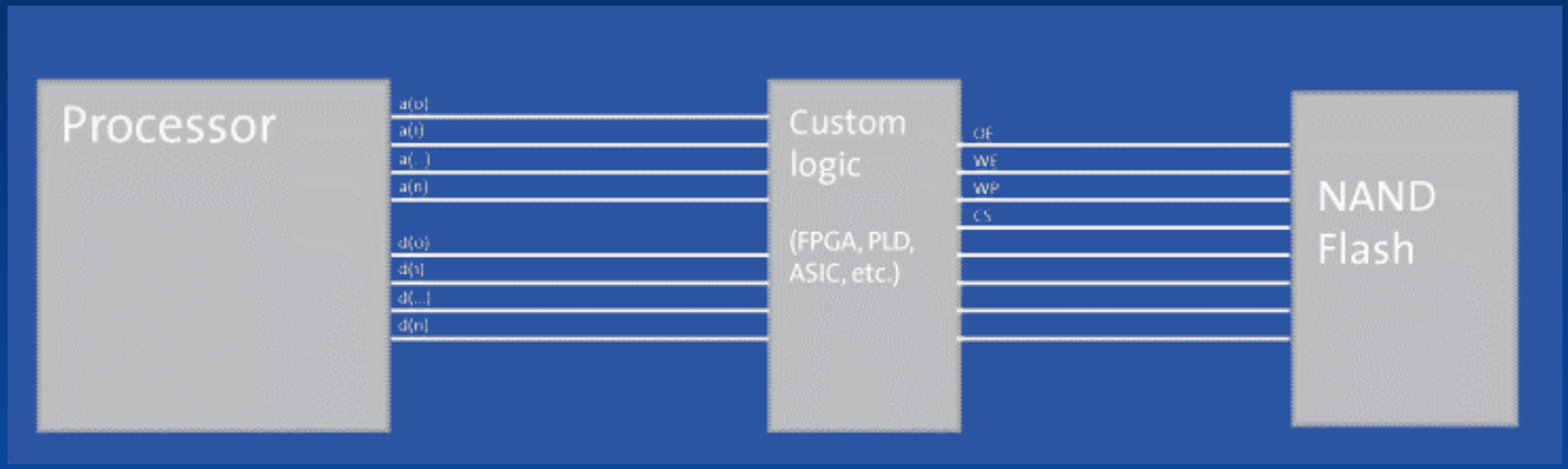
NAND cell organization accesses each cell through adjacent cells





Interfaces Are Different

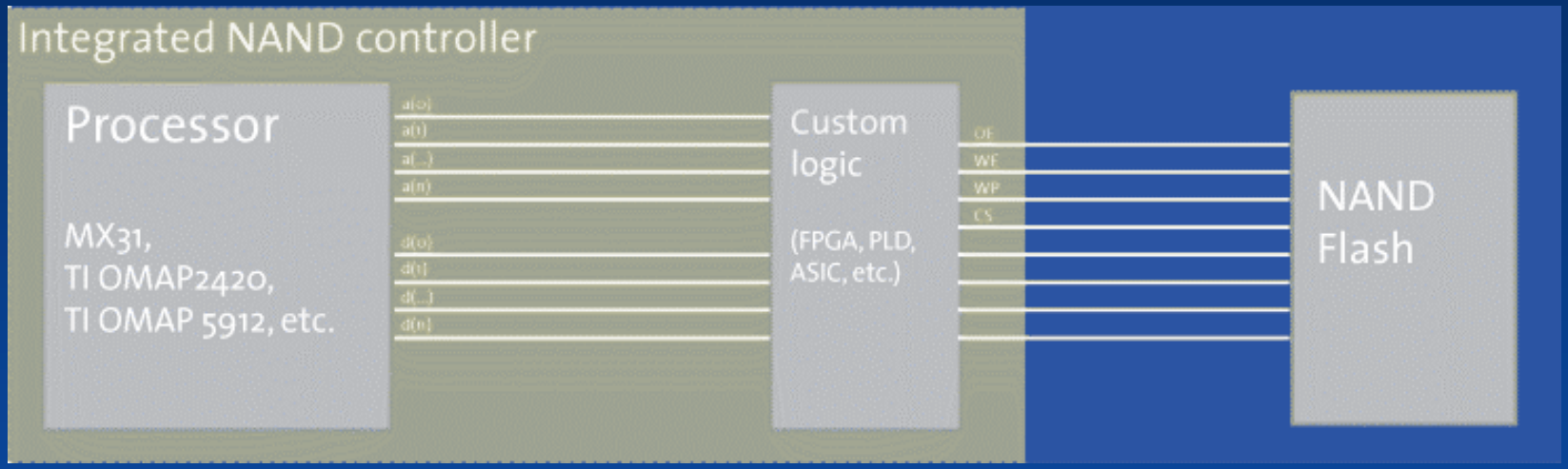
Integration got more complex



Different Approaches to Simplify Integration Have Emerged

- Integrated NAND Controllers
- Hybrid technologies

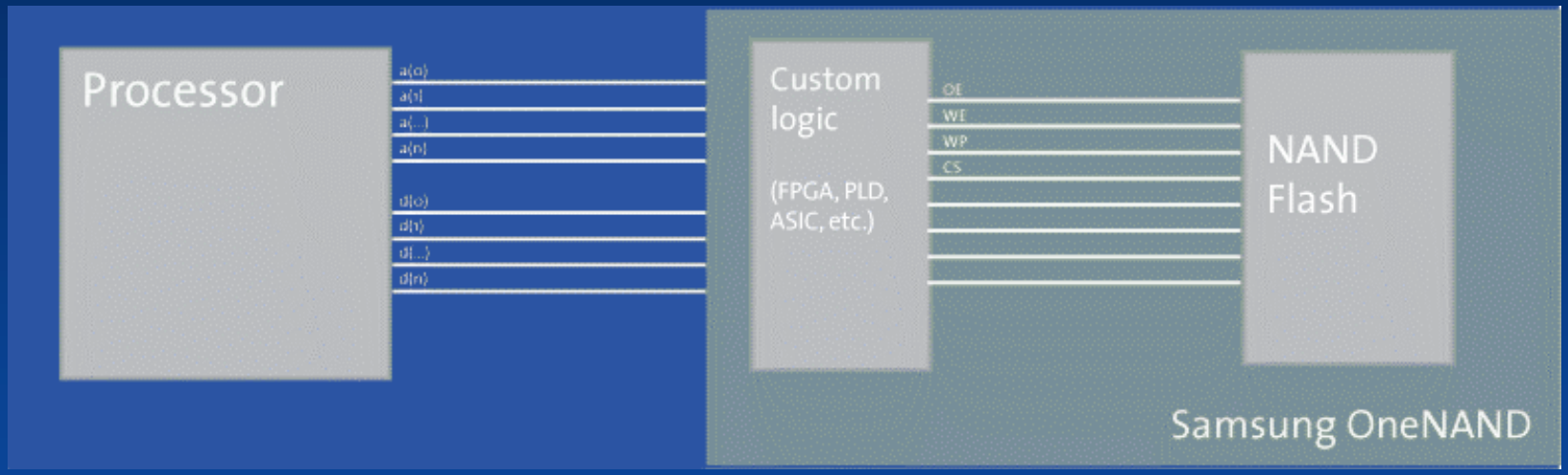
Integrated NAND Controllers



Integrated NAND Controllers

- NAND Controller design goals:
  - to hide NAND complexities by having software send programming and read info to a predefined set of registers and not have software access the NAND directly
  - to allow developers freedom of choice in NAND chip selection.
- Leading companies
  - Qualcomm- MSM5600
  - Freescale - iMX21, iMX31
  - Toshiba - TX493x Series
  - Intel – Monohan

Hybrid Solutions



Hybrid Solutions

- Samsung OneNAND™
  - single-die chip with standard NOR interface using NAND Flash Array
  - performance advantages over NAND and NOR
- Spansion OrNAND™ MirrorBit® architecture
  - well-suited for data storage in wireless handsets,
  - delivers NAND interface and cost structure of traditional NAND solutions with reliability and fast read performance of NOR Flash memory.

90nm Intel NOR - “Sibley”

- First NOR multi-level cell (MLC) flash memory device manufactured on Intel's 90 nanometer technology
- Offers fast NOR read speeds to enable zero-wait code execution up to 108 Mhz
- Write speeds up to 500 kB per second enables rapid data storage of multimedia images
- Increases NOR flash density reach with 512Mb device, as well as multiple RAM interfaces to provide the greatest design flexibility

Today's Designs

- Existing designs rely on both NAND and NOR arrays to balance cost per bit and reliability goals
- Hybrid chips and integrated NAND controllers promise benefits of NOR and NAND within a single solution
- MLC, like Sibley, offer benefits but demand supporting software evolve

In Summary

Choices to Address Key Design Considerations

High Performance, Low Cost and Middle Density Storage Arrays

- Hybrid technologies
  - Samsung OneNAND
  - Spansion OrNAND
- Continuing challenge
  - Emerging technologies not yet widely support with software

Write Performance and Design Simplicity

- Integrated NAND Controller
- Continuing challenges
  - controller availability
  - a sharp learning curve
  - software support

Long-term High Performance and Reliability

- Convergence
- Continuing challenges
  - innovation
  - software

Future Thoughts

- Increasing demand for storage means higher densities and larger arrays
- Time-to-market demands require simplification of hardware design and more hardware standards
- Differentiation will come from software

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Or drop by the Exhibit Hall!