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Flash Memory *Trends & Perspectives*

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Semiconductor Insights

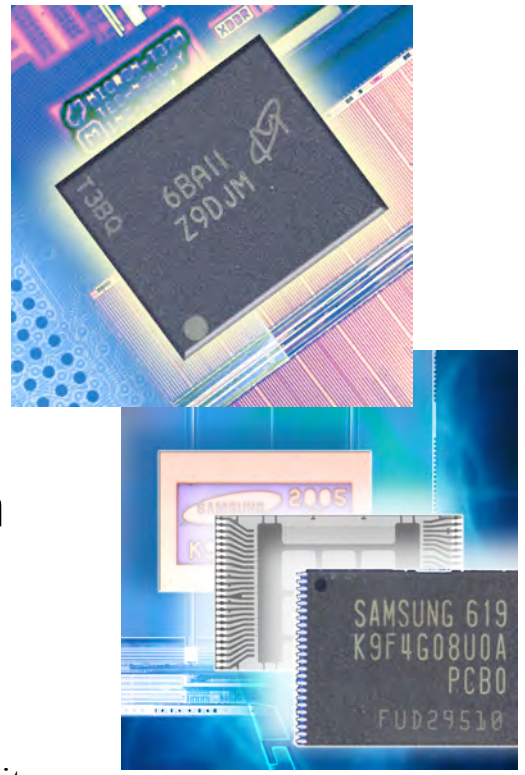
Memory Roadshow Outline

1. Introduction of Semiconductor Insights
2. NAND Technology
   - Technology Hurdles
   - NAND Device Trends (Die Size, Cell Size, Architecture)
   - MLC vs SLC
3. NOR Technology
   - NOR Device Trends (Die Size, Architecture)
   - High Level Device Analysis
4. Flash Processes
5. Trends & Perspectives

Semiconductor Insights

- World's leading technical advisor to global microelectronics industry
- Support clients with in-depth technical investigation of IC's and electronic systems to…
  - Assert their IP rights
  - Develop & commercialize new technologies and products
- Clients
  - Major electronics and semiconductor corporations in Japan, Korea, Taiwan, Europe, & North America and their representing law firms

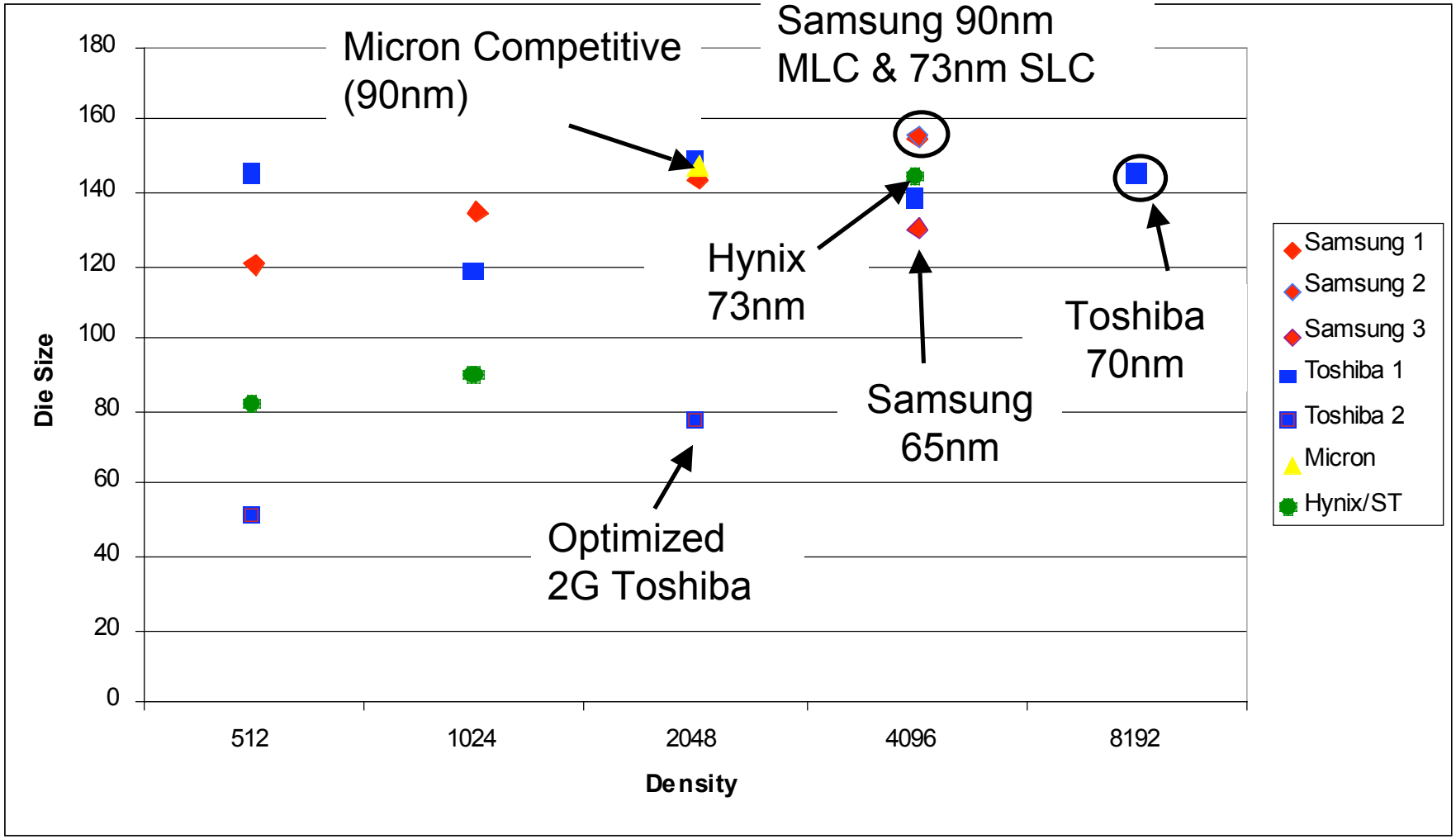
- TECHinsights helps technology companies…
  - Solve technical problems to:
    - Build competitive position
    - Assess new market entry
- Memory is one of eight areas of expertise
- Memory expertise includes
  - NAND Flash
  - NOR Flash
  - DRAM
  - eMemory
  - SRAM
  - New & Other Technology Related to Silicon Data Storage



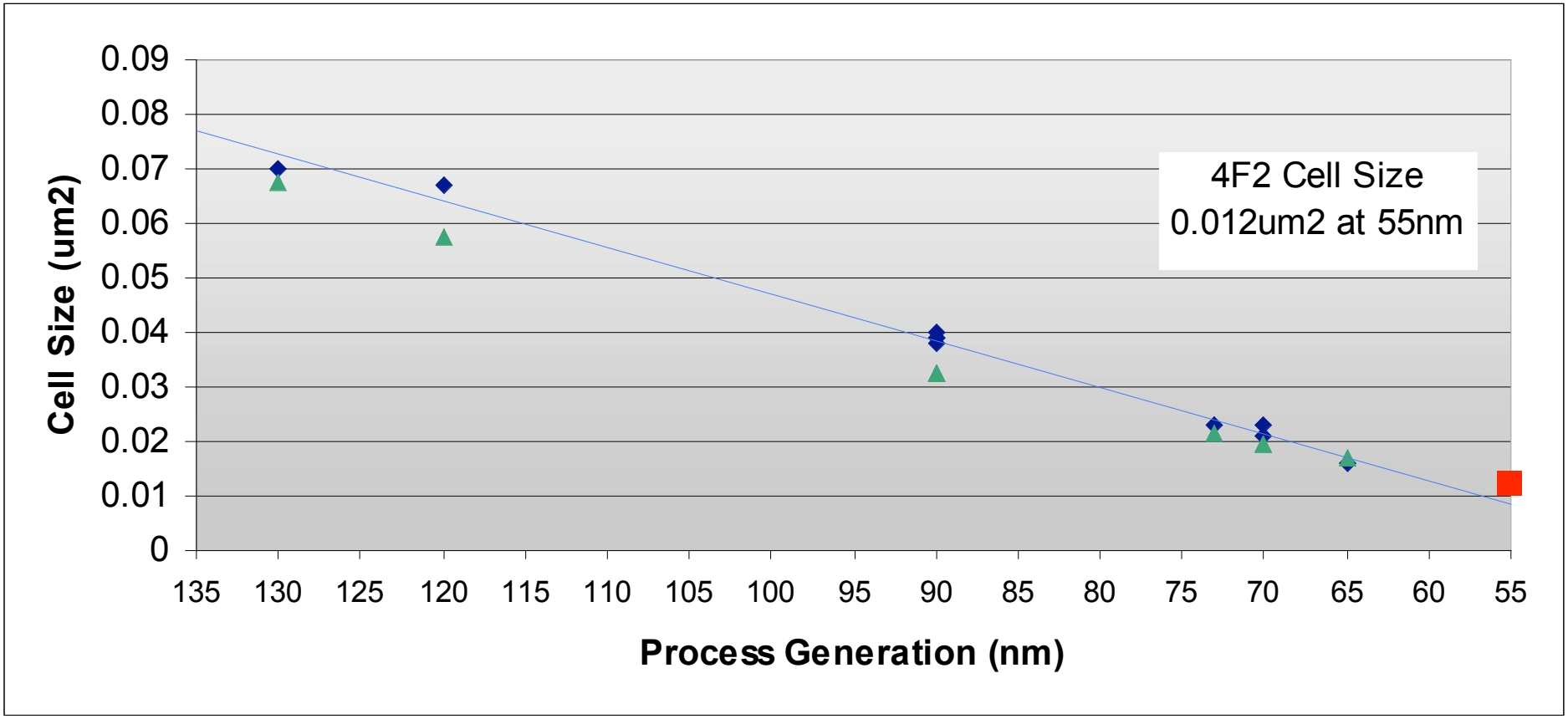
NAND Technology Hurdles

- NAND competes on density and cost, reliability is not as good as NOR but use ECC.
  - Use advanced processes
  - Minimize Die Size
  - Use MLC technology
- MLC Technology
  - Difficult to sense voltage levels as technology scales
  - Reliability is not as good as SLC but good enough

NAND Die Size Trends – Small Die, Low Cost



NAND Flash Cell Sizes



Evaluated Leading-edge NAND Flash Devices

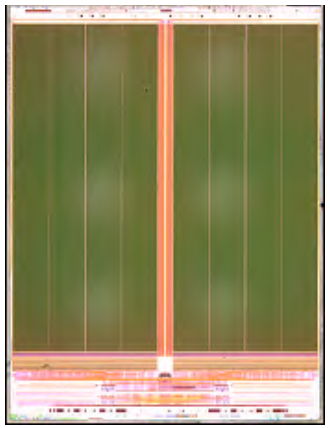
Manuf.	Part Number	Technology	Die Capacity (Gbit)	Die Size (mm^2)	Die Density (Mbit/ mm^2)
Samsung	K9F4G08U0A	65nm SBC	4	131	31.3
Samsung	K9G4G08U0M	90nm MLC	4	156	26.2
Samsung	K9F4G08U0M	73nm SBC	4	155	26.4
Toshiba	TH58NVG3D4BTGI0	90nm MLC	4	138	29.0
Hynix/ST	NAND04GW3B2BN6	73nm MLC	4	144	28.4
Toshiba	TC58NVG3D4CTG00	70nm MLC	8	145	56.5

NAND Flash Architecture Convergence

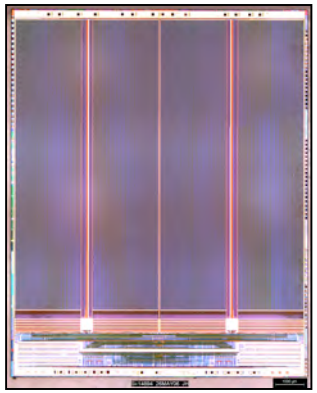
Samsung 2Gbit 90nm

Micron 2Gbit 90nm

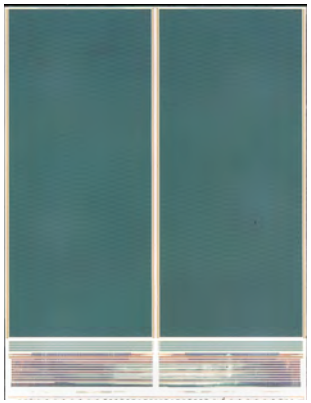
Toshiba 4Gbit 90nm



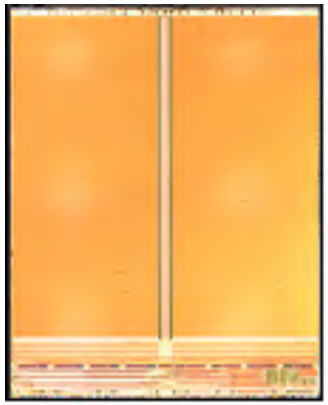
Samsung 4Gbit 73nm



Samsung 4Gbit 65nm



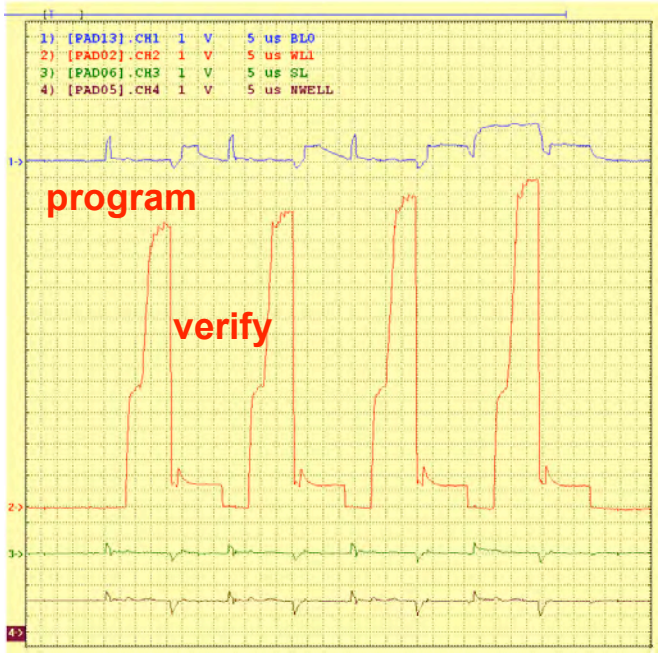
Toshiba 8Gbit 70nm

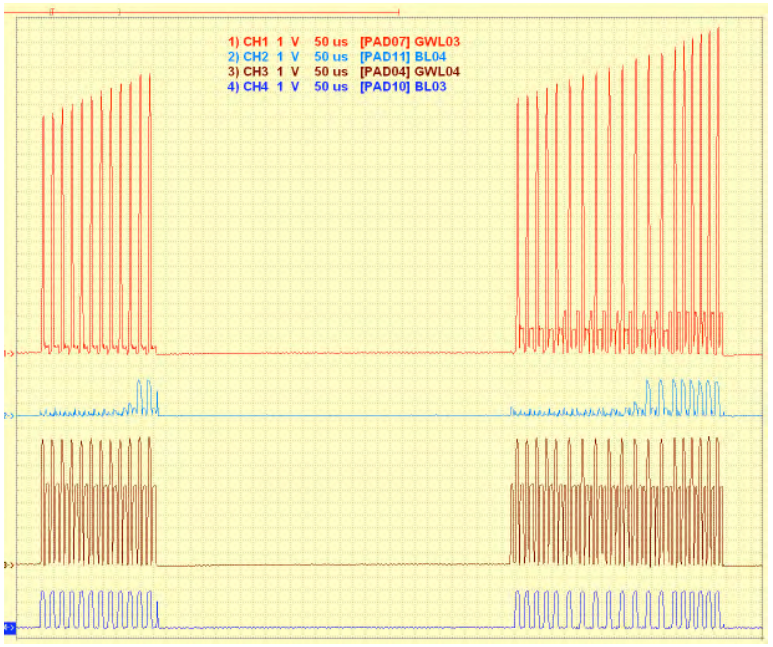


Hynix 4Gbit 73nm

Common Architectural Layout

SLC vs MLC – Lower Cost but Added Complexity





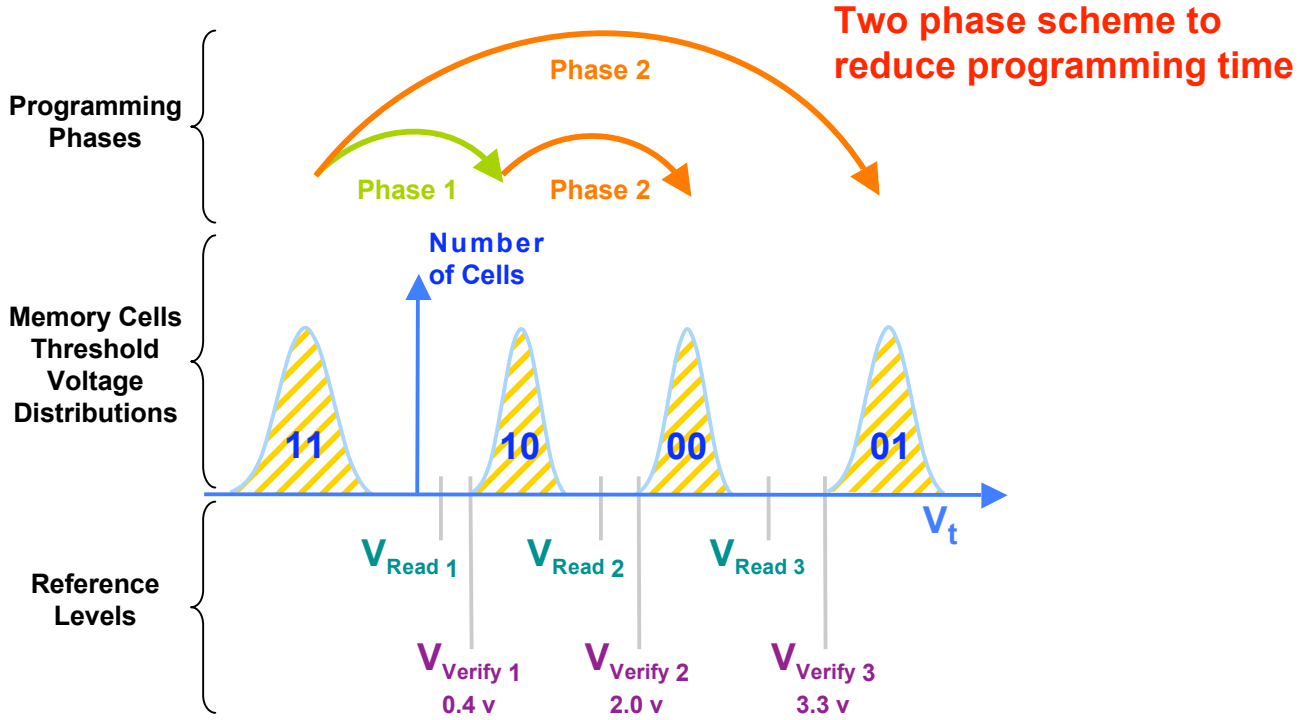
SLC

- Simpler programming algorithm
- More reliable
- More expensive

MLC

- Complex programming algorithm
- Cost advantages
- Less reliable

Toshiba Programming Algorithm

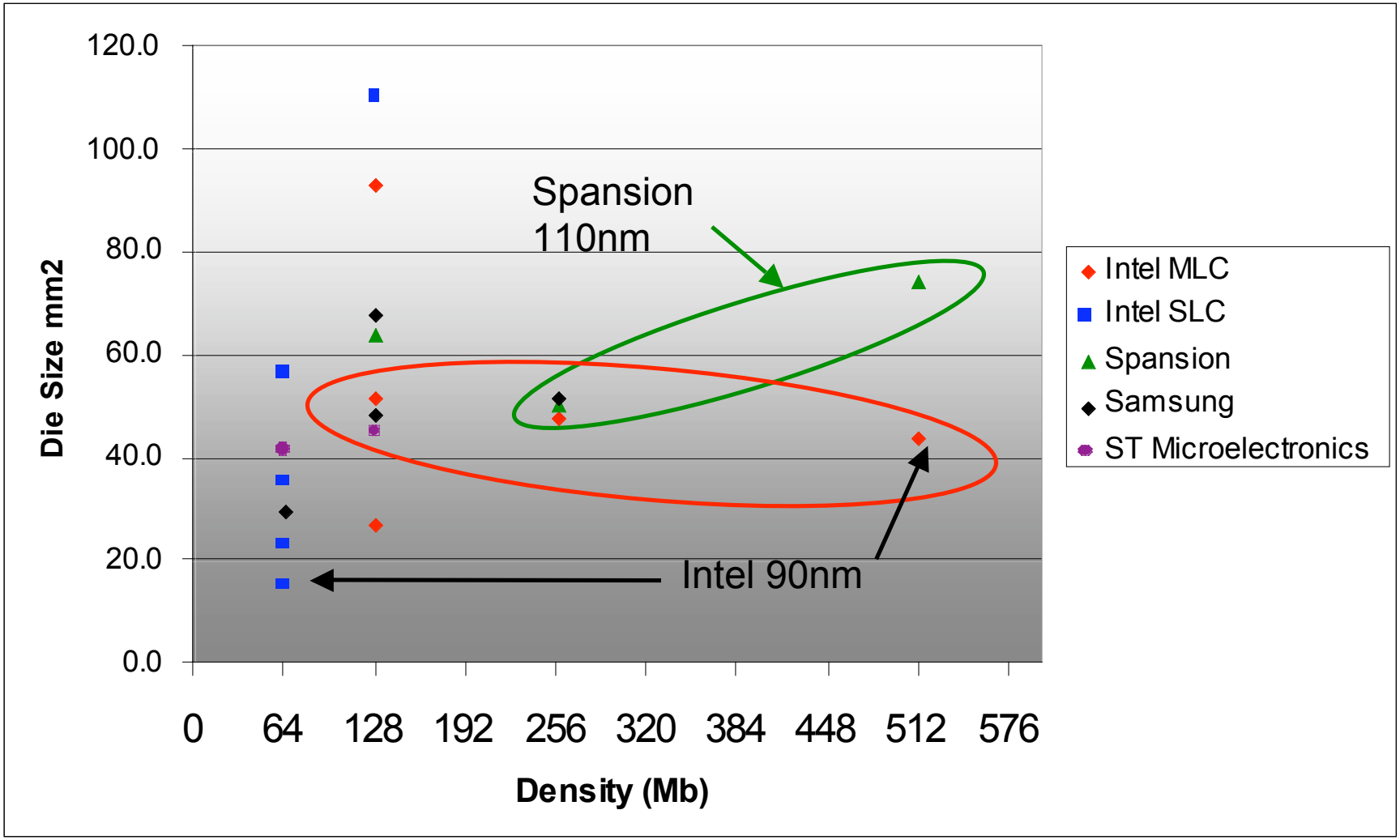


Memory States Illustration

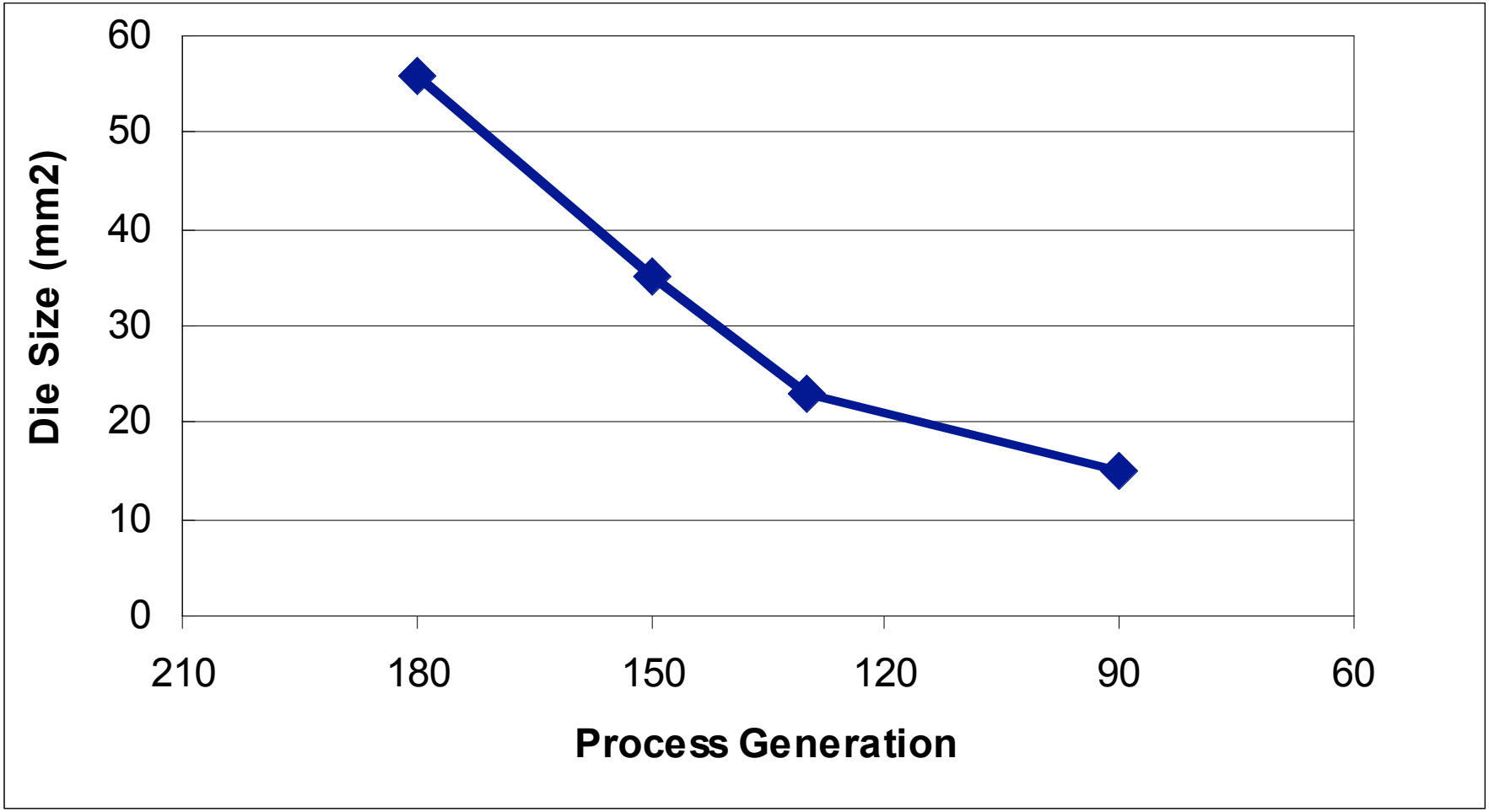
NOR Technology Hurdles

- NOR used in wide variety of applications (Ease of use and increased reliability)
- Reliability is key for NOR
  - Technology scaling
  - MLC sensing in upcoming generations
- Density

NOR Flash Die Size/Density Trends



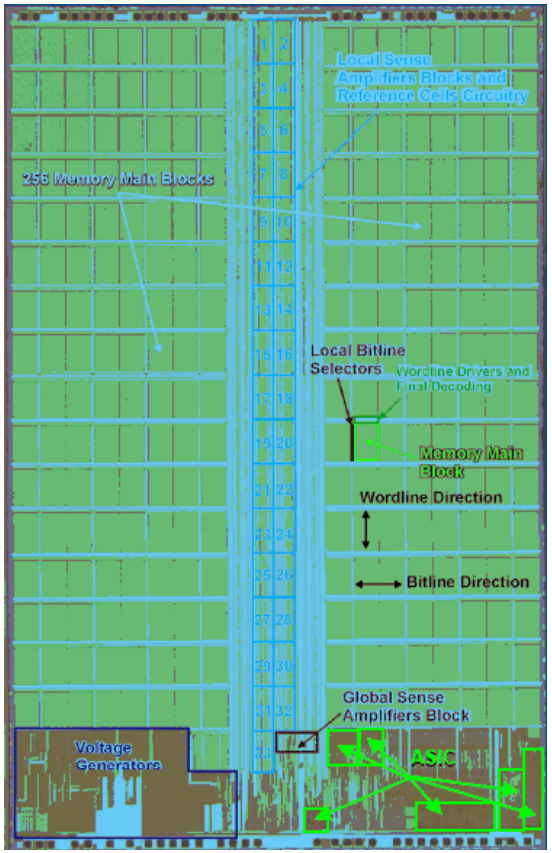
Intel 64M SLC Die Sizes



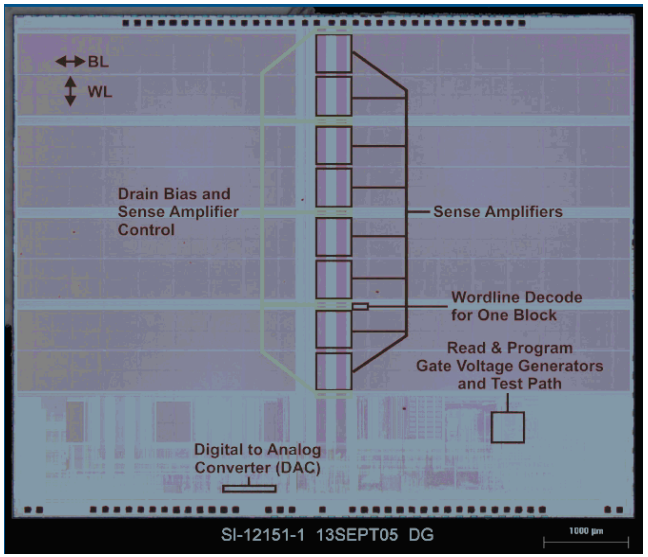
Flash Device Comparison

Device	Part Number	Die Size (mm^2)	Die Efficiency (Mb/mm^2)	Process (nm)
Spansion 3.0 V 512 Mb (MBC) trapped charge	GL512N11FAE01	74.69	6.85	110
Spansion 1.8 V 256 Mb (MBC) trapped charge	WS256NOLBAW01	50.35	5.08	110
Intel 1.8 V 256 Mb (MLC) floating gate	28F256L18	47.85	5.35	130
Intel 1.8 V 512 Mb (MLC) floating gate	28F512EM	43.8	11.69	90
Intel 1.8 V 64 Mb floating gate	28F640EW	15.12	4.24	90

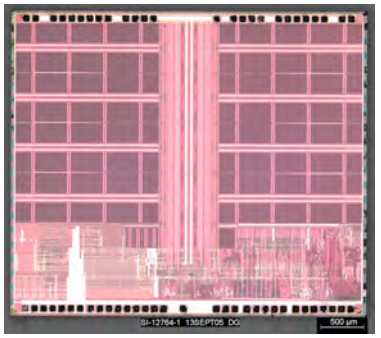
Intel Flash Products



Intel L18 (130nm)
47.9mm^2



Intel M18 (90nm)
43.8mm^2



Intel Wireless (90nm)1 5.1mm^2

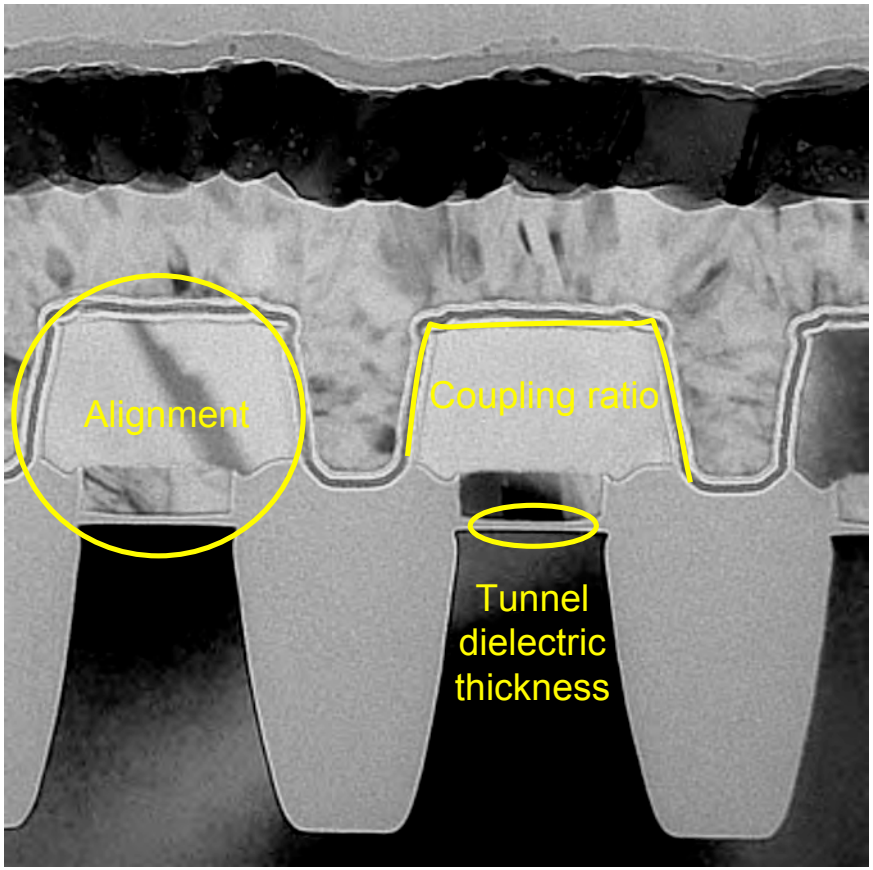
Spansion Mirrorbit Devices

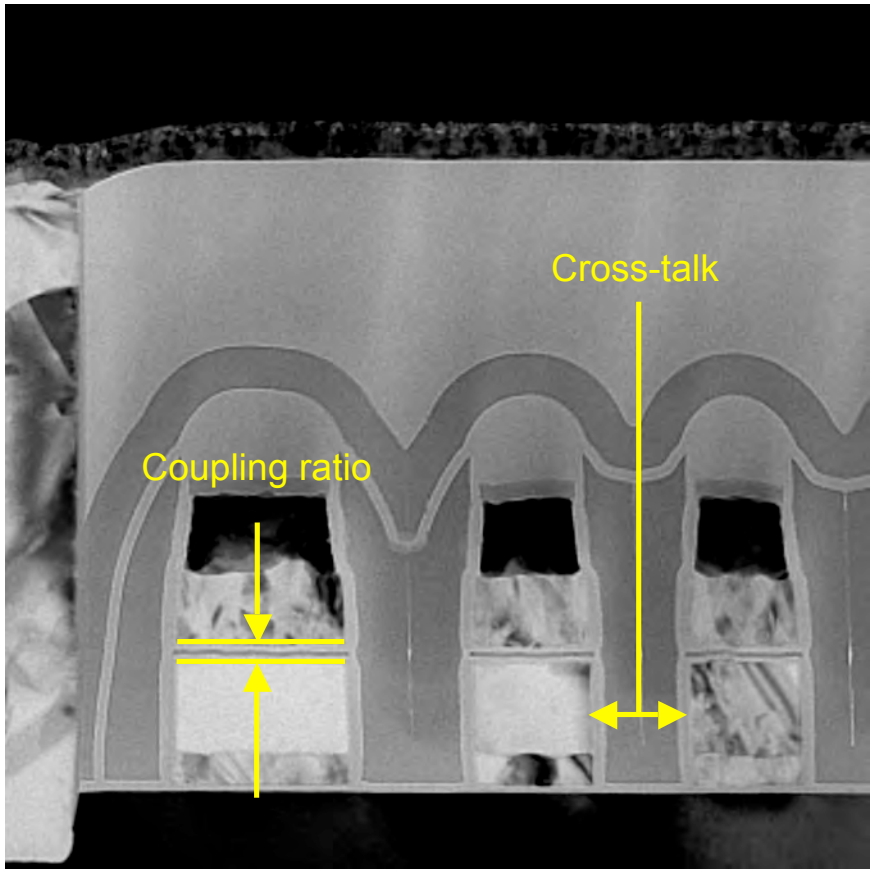
Spansion 3.0v
110nm 512Mb

Spansion 1.8v
110nm 256Mb

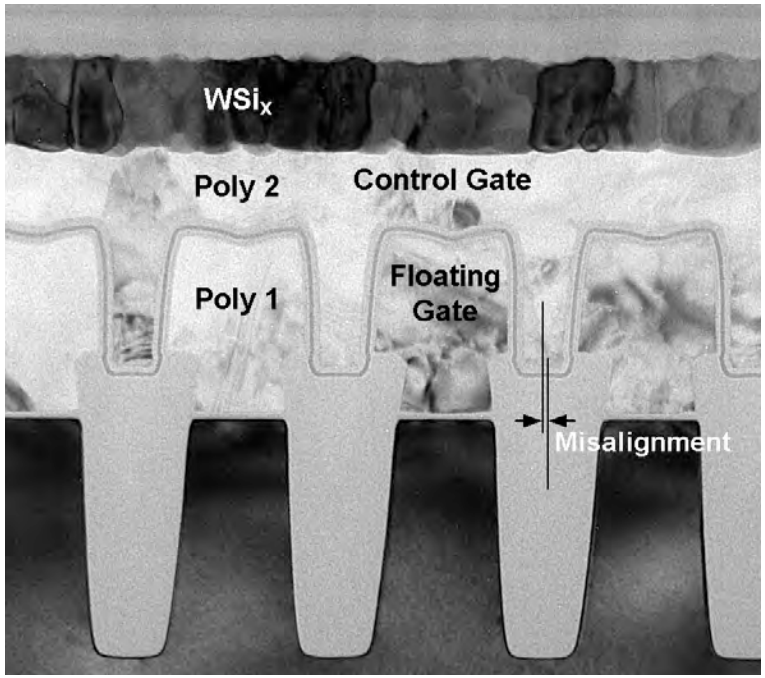
AMD 3.0v
230nm 64Mb

Scaling Challenges



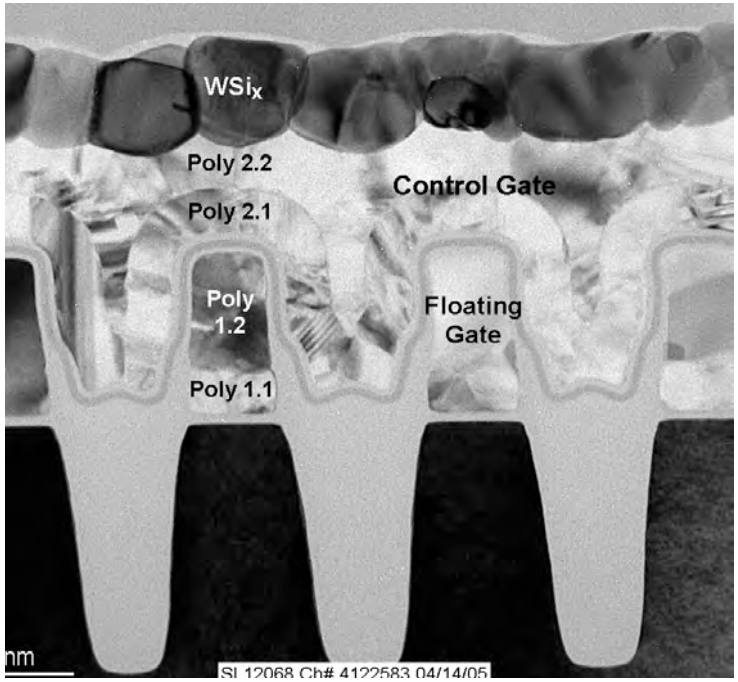


Flash Cell Types



SA-STI Cell

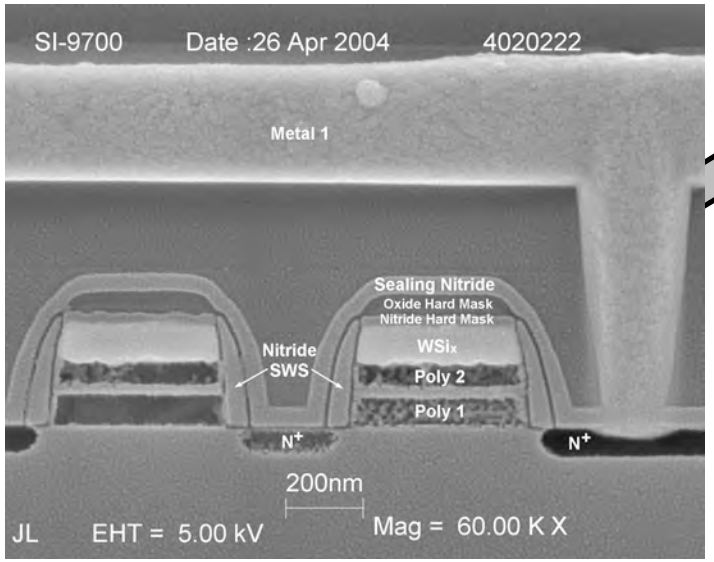
- Used by most manufacturers up to 90nm node and some beyond
- Misalignment Problems

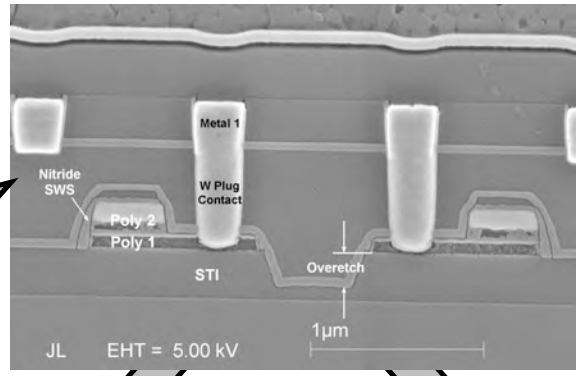


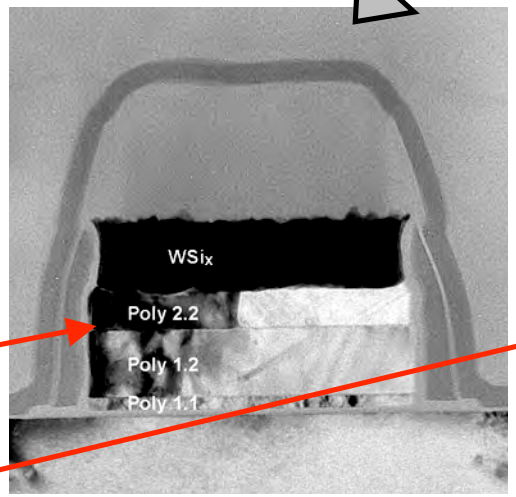
Fully Aligned Cell

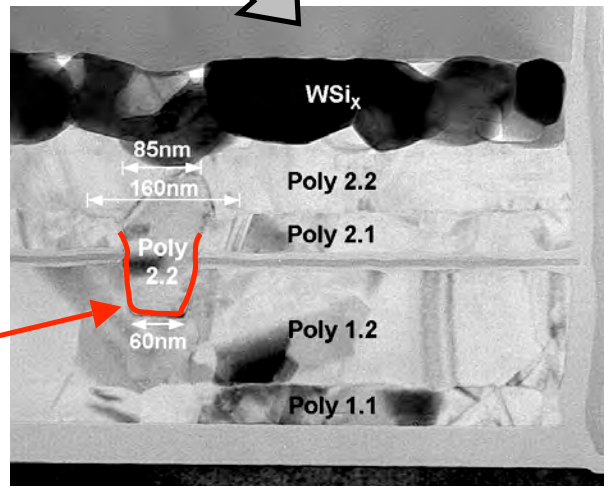
- Used by Toshiba at 90nm and Samsung at 73nm and 65nm
- No misalignment problems

Peripheral Gate Stack





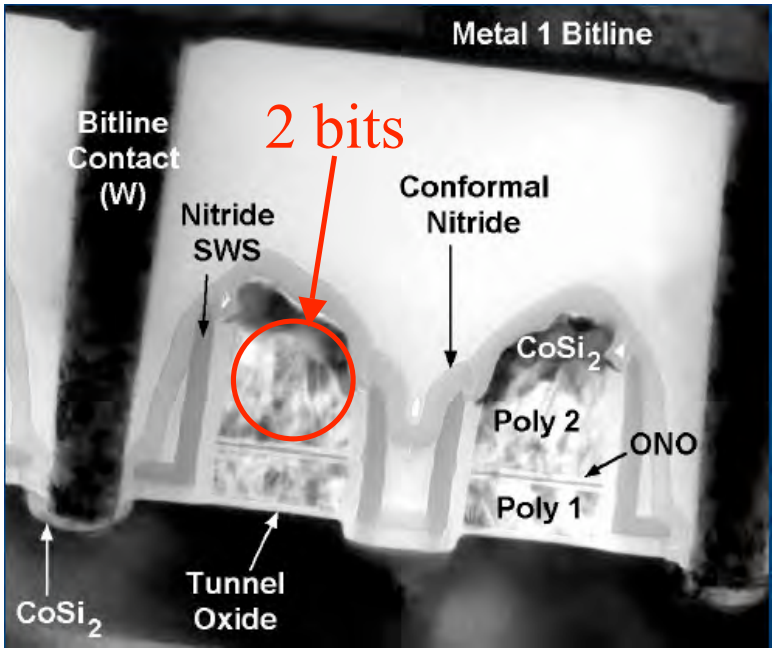


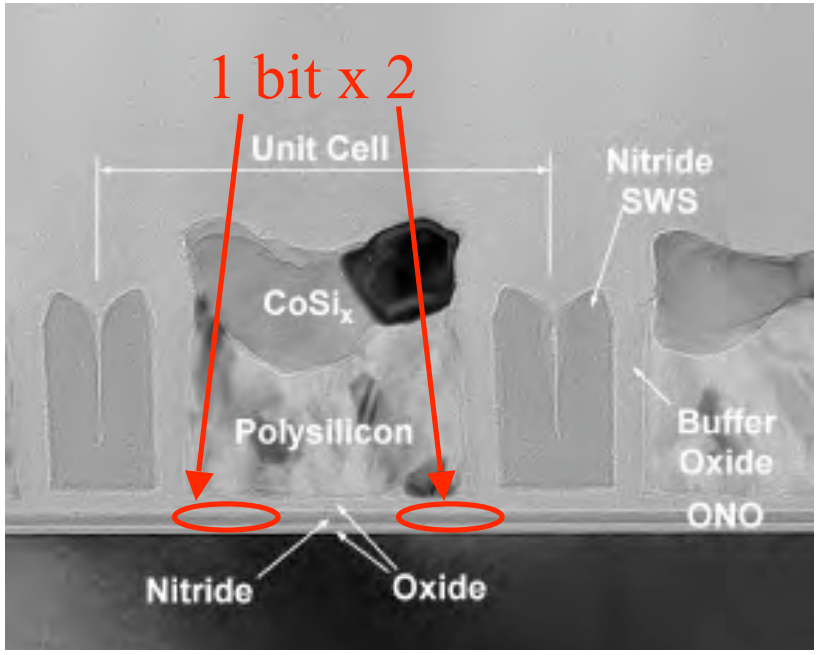


No ONO

Contact Window

Floating Gate (StrataFlash) vs NROM (Mirrorbit)





Floating Gate (StrataFlash)

- Store electrons in floating gate
- Multi-Level Sensing

NROM

- Storage in Nitride layer
- 2 bits per cell but two physical locations in cell

Current Technology

- NAND architecture converging although some variations in design
- 1st Generation NAND sizes between 135mm^2 & 160mm^2
- MLC manufacturers increasing, cost savings but added complexity & less reliability
- Cell basic structure unchanged through several generations in NAND with SA-STI, manufacturers adopting completely self aligned cell others likely to follow
- Tunnel oxide and inter-poly dielectric almost unchanged up to 90nm generation

Technology Trends

- We believe that the current floating gate planar cell structure can be scaled to the 45 nm node - More revolutionary technologies may be required to go beyond:
  - TODAY
    - Both MLC and NROM technologies are viable
    - FRAM gaining acceptance in niche markets
    - Matrix OTP memory – disposable digital film
  - TOMORROW
    - Will MLC or NROM technology scale better
    - PCRAM – Devices soon?
    - Non-planar cell structure (FinFET or recessed-channel)
    - Samsung recently announced 50nm 16G flash memory die using 3D-transistor architecture (which is probably Samsung's proprietary recessed-channel technology)
    - Nanocrystal technology ~ Electrons trapped into silicon nanocrystals that act as nano-floating gates

Questions

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