Pre-enabling designs with ONFI (Open NAND Flash Interface)

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ONFi OPEN NAND FLASH INTERFACE

Agenda

- Reasons for ONFI
  - Current situation
  - Why ONFI is needed
- What is ONFI
- How to use ONFI
- Current status

Inconsistency of NAND Flash

- Higher Performance
  - Parallel operations
  - Faster timing
- Higher Density
  - (Multi-level cell) MLC
  - Fewer erase cycles
- Process Improvements
  - 70nm, 55nm.....

Similar: Basic Commands

- Basic commands *typically* common
  - Reset, Read ID, Read, Page Program, Erase, ...
- More complex operations all over the map

Table 1. Command Sets

Function	1st. Cycle	2nd. Cycle
Read	00h	30h
Read for Copy Back	00h	35h
Read ID	90h	-
Reset	FFh	-
Page Program	80h	10h
Cache Program	80h	15h
Copy-Back Program	85h	10h
Block Erase	60h	D0h
Random Data Input*1	85h	-
Random Data Output*1	05h	E0h
Read Status	70h	

*Samsung K9K4G08U0M datasheet

FUNCTION	1st CYCLE	2nd CYCLE
READ 1	00h	30h
READ FOR COPY-BACK	00h	35h
READ ID	90h	-
RESET	FFh	-
PAGE PROGRAM (start)	80h	10h
COPY BACK PGM (start)	85h	10h
CACHE PROGRAM	80h	15h
BLOCK ERASE	60h	D0h
READ STATUS REGISTER	70h	-
RANDOM DATA INPUT	85h	-
RANDOM DATA OUTPUT	05h	E0h
CACHE READ START	00h	31h
CACHE READ EXIT	34h	-
LOCK BLOCK	2Ah	-
LOCK TIGHT	2Ch	-
UNLOCK (start area)	23h	-
UNLOCK (end area)	24h	-
READ LOCK STATUS	7Ah	-

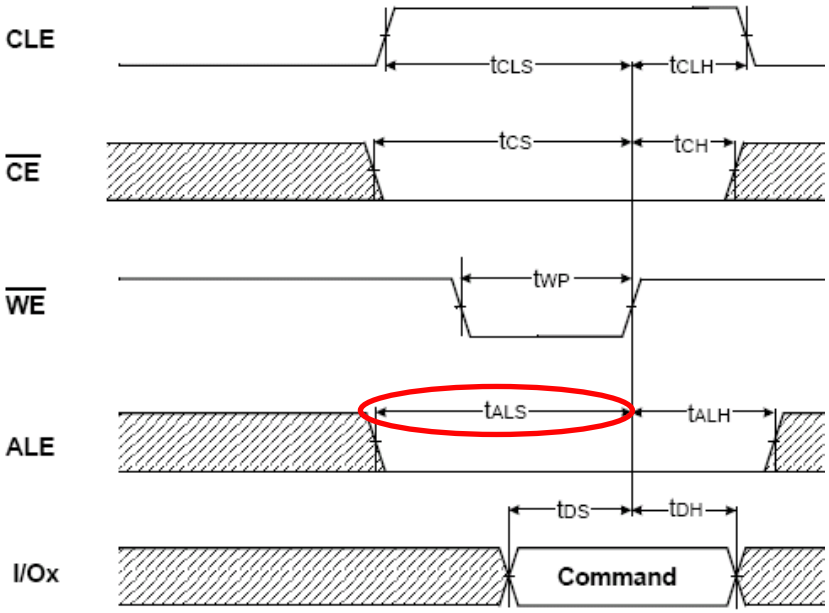
Table 4: Command Set

*Hynix HY27UG084G2M datasheet

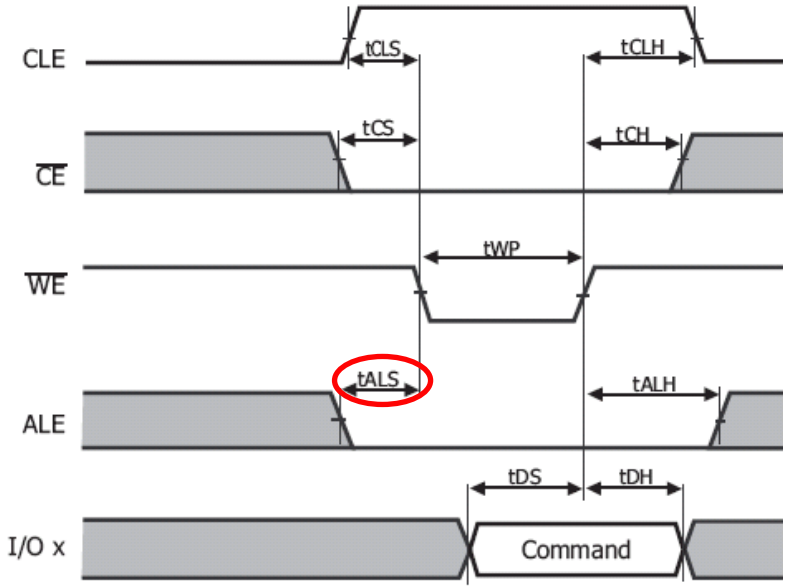
*Other names and brands may be claimed as the property of others

Similar: Timing

- Timing requirements are specified differently
- Min/max values are not necessarily the same for similar cycle time parts



*Samsung K9K4G08U0M datasheet



*Hynix HY27UG084G2M datasheet

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Similar: Status Values

- Status values dependent on command
- Often the same, but not required to be
  - Can you tell that these are the same??

I/O No.	Page Program	Block Erase	Cache Prorgam	Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Pass/Fail(N)	Not use	Pass : "0" Fail : "1"
I/O 1	Not use	Not use	Pass/Fail(N-1)	Not use	Pass : "0" Fail : "1"
I/O 2	Not use	Not use	Not use	Not use	Don't -cared
I/O 3	Not Use	Not Use	Not Use	Not Use	Don't -cared
I/O 4	Not Use	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Ready/Busy	Ready/Busy	True Ready/Busy	Ready	
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready	
I/O 7	Write Protect	Write Protect	Write Protect	Write I	

*Samsung K9K4G08U0M datasheet

*Hynix HY27UG084G2M datasheet

IO	Page Program	Block Erase	Cache Program	Read	Cache Read	CODING
0	Pass / Fail	Pass / Fail	Pass / Fail (N)	NA		Pass: '0' Fail: '1'
1	NA	NA	Pass / Fail (N-1)	NA		Pass: '0' Fail: '1' (Only for Cache Program, else Don't care)
2	NA	NA	NA	NA		-
3	NA	NA	NA	NA		-
4	NA	NA	NA	NA		-
5	Ready/Busy	Ready/Busy	P/E/R Controller Bit	Ready/Busy	P/E/R Controller Bit	Active: '0' Idle: '1'
6	Ready/Busy	Ready/Busy	Cache Register Free	Ready/Busy	Ready/Busy	Busy: '0' Ready': '1'
7	Write Protect	Write Protect	Write Protect	Write Protect		Protected: '0' Not Protected: '1'

*Other names and brands may be claimed as the property of others

Similar: Read ID

- The first and second byte are consistently manufacturer and device ID
- The number of remaining bytes and what they mean is up in the air

*Samsung K9K4G08U0M datasheet

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Don't care
4th Byte	Page Size, Block Size, Spare Size, Organization

*Toshiba TH58NVG1S3AFT05 datasheet

	Descripton	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98H
2nd Data	Device Code	1	1	0	1	1	0	1	0	DAH
3rd Data	Chip Number, Cell Type, PGM Page, Write Cache	0 or 1	0	0	0	0	0	0	1	81H or 01H
4th Data	Page Size, Block Size, Redundant Size, Organization	0 or 1	0	0	1	0	1	0	1	95H or 15H
5th Data	Plane Number, Plane Size	0 or 1	1	0	0	0	1	0	0	44H or C4H

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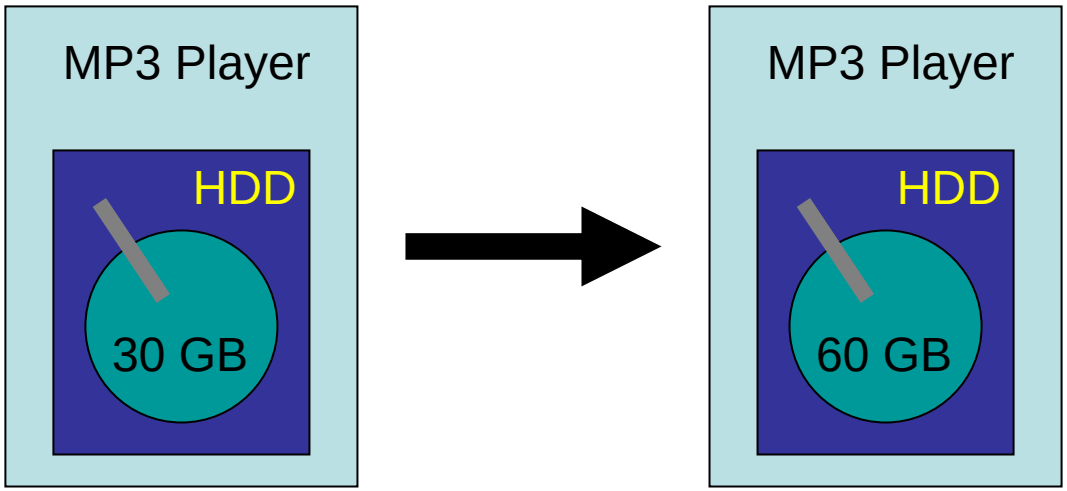
Similar Hinders NAND Adoption

- To deal with differences, the host must maintain a chip ID table of known devices
  - Table contains read/write timings, organization, status bit meanings, etc for each known NAND Flash part
- Situation has two major effects:
  - Precludes intro of new NAND devices into existing designs
  - Makes qualification cycles longer as each NAND device added requires changes to be comprehended
- Similar to the ancient disk drive interfaces that required a list of disk drive types in a BIOS table

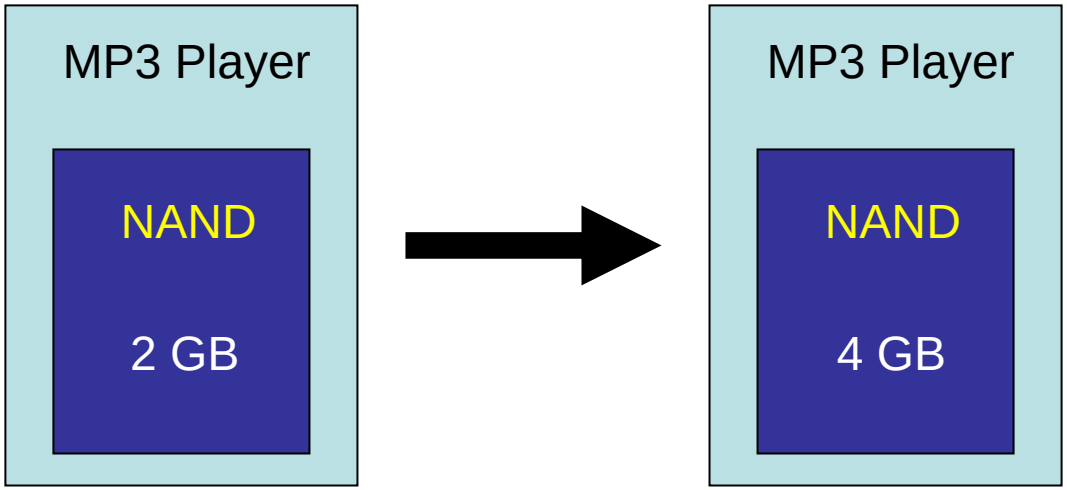
Lack of standard impacts platforms supporting a range of NAND

Product Update Cycle for HDD



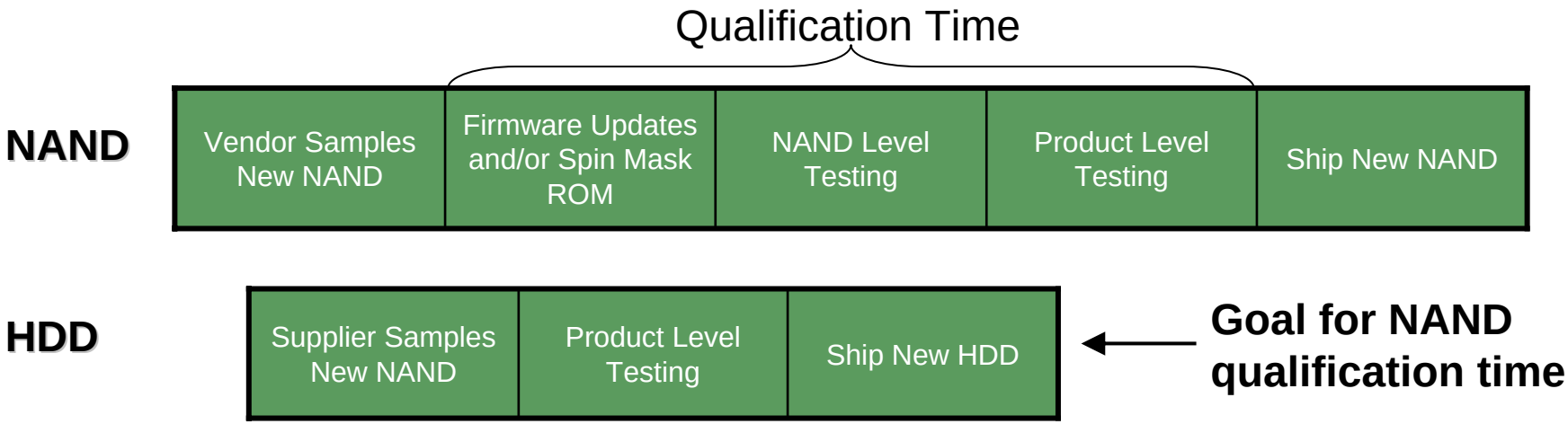
- No software changes required
- Product-level testing and validation focus
- Physical and logical interface standard

Product Update Cycle for NAND



- Firmware/software changes required
  - Change device ID table to support new component
  - Add support for new commands to maintain or increase performance
  - Update timing to comprehend new part
  - Update ECC to comprehend bit rate
- Potentially spin new Mask ROM (1 month delay)
- Complete re-test of firmware and/or software

Delayed Opportunities …



- NAND Flash requires more qualification time than other commodity memory products
- Lost revenue opportunity that could be rectified with standard interface
  - Impossible today for controller to anticipate and be prepared for upcoming Flash behavior

Lack of standard interface impacts time to market and revenue

What is ONFI

- ONFI is a specification for a standardized NAND Flash interface
- ONFI ensures no pre-association with NAND Flash at host design is required
  - Adds mechanism for a device to self-describe its features, capabilities, etc to the host via a parameter page
  - Features that cannot be self-described in a parameter page (like number of CE#) is host discoverable
- ONFI leverages existing Flash behavior to the extent possible
  - Intent is to enable orderly and TTM transition, so highly divergent behavior from existing NAND undesired
  - Where prudent for longevity or capability need, existing Flash behavior is modified or expanded
- ONFI enables future innovation
  - ONFI provides an infrastructure that supports future feature additions and enhancements in a structured way.

What is in ONFI

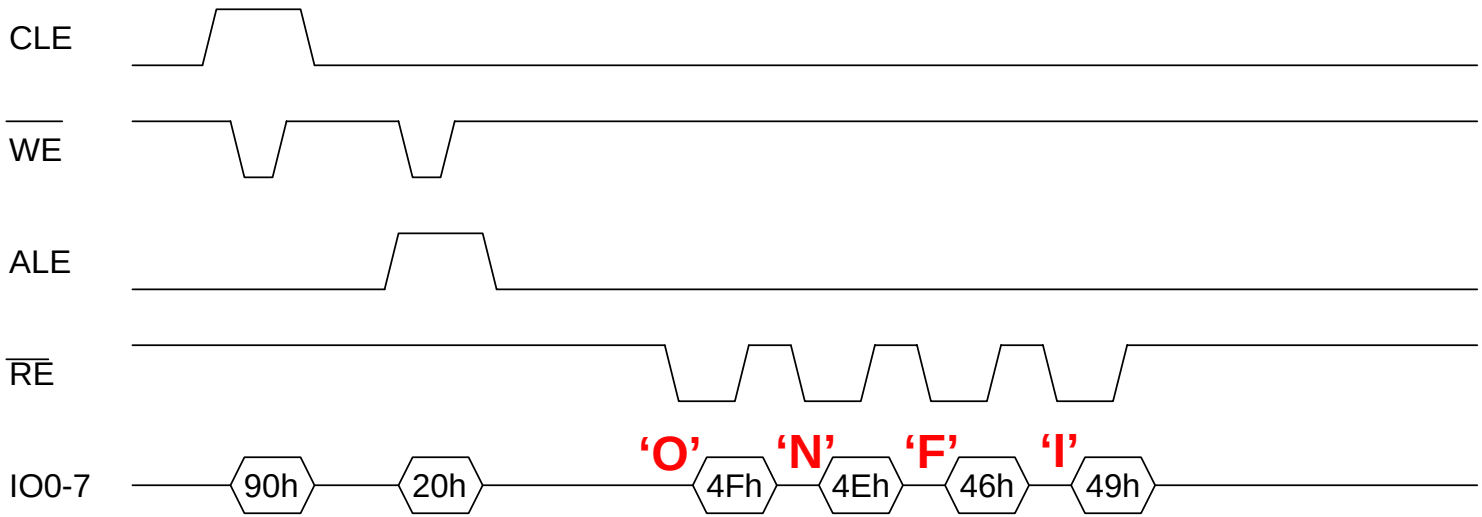
- Standardized pin-out
- Device Abstraction
- Standardized Command set
- Self-reporting
- Electrical parameters
- Timing
- Bad block marking

How to use ONFI

- ONFI is intended to be used to enable new NAND devices without having to update system software
  - Similar to flash already qualified
- The parameter page is a central part of the ONFI spec that is used to describe the NAND device's architecture and capabilities
- Key sections of the parameter page:
  - ONFI revision
  - Supported features
    - x16, on-board ECC, non-sequential page program, interleaving
  - Supported optional commands
    - Read Status Enhance, Page Cache Program, etc
  - Memory organization
    - Page size, max bad blocks, ECC, endurance, etc
  - Electrical characteristics
    - Timings supported
- ONFI can be used to standardize new features and faster performance.
- System software can be updated to make use of these features via ONFI

Determining ONFI Support

- Read ID is used by Flash parts today to report device ID for use in chip ID table lookup
- ONFI support is shown by responding to Read ID for address 20h with ASCII ‘ONFI’
- Support for vendor specific interface and ONFI allowed by changing address cycle to 20h from 0h



Command Set Overview

Command	O/M	1st Cycle	2nd Cycle	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy
Read	M	00h	30h		Y
Change Read Column	M	05h	E0h		Y
Read Cache	O	31h			
Read Cache End	O	3Fh			
Read Cache Enhanced	O	00h	31h		Y
Block Erase	M	60h	D0h		Y
Read Status	M	70h		Y	Y
Read Status Enhanced	O	78h		Y	Y
Page Program	M	80h	10h		Y
Page Cache Program	O	80h	15h		Y
Change Write Column	M	85h			Y
Read ID	M	90h			
Read Parameter Page	M	ECh			
Get Features	O	EEh			
Set Features	O	EFh			
Reset	M	FFh		Y	Y
Read for Copyback	O	00h	35h		Y
Copyback Program	O	85h	10h		Y

Timing Requirements

- NAND contains a lot of timing requirements and hence timings
- Reporting each and every timing value leads to validation challenge
  - Requires validation of all combinations
- To make timing information useful, organized into timing modes

Parameter	Description
tADL	Minimum ALE to data loading time
tALH	Minimum ALE hold time
tALS	Minimum ALE setup time
tAR	Minimum ALE to RE# delay
tBERS	Maximum block erase time
tCEA	Maximum CE# access time
tCH	Minimum CE# hold time
tCHZ	Maximum CE# high to output hi-Z
tCLH	Minimum CLE hold time
tCLR	Minimum CLE to RE# delay
…	…
tREH	Minimum RE# high hold time
tRHOH	Minimum RE# high to output hold
tRHW	Minimum RE# high to WE# low
tRHZ	Maximum RE# high to output hi-Z
tRLOH	Minimum RE# low to output hold
tRP	Minimum RE# pulse width
tRR	Minimum Ready to RE# low
tRST	Maximum device reset time
tWB	Maximum WE# high to R/B# low
tWC	Minimum write cycle time
tWH	Minimum WE# high hold time
tWHR	Minimum WE# high to RE# low
tWP	Minimum WE# pulse width

Timing Modes

- Timing modes define vast majority of required host timings as one “set”
- Three parameters are specified separately in RPP
  - Max page read time
  - Max block erase time
  - Max page program time
- Timing modes supported reported in timing parameters block of RPP

Parameter	Mode Example		Unit
	30		ns
	Min	Max	
tADL	100		ns
tALH	5		ns
tALS	10		ns
tAR	10		ns
tCEA		25	ns
tCH	5		ns
tCHZ		20	ns
tCLH	5		ns
tCLR	10		ns
tCLS	15		ns
…	…	…	ns
tWB		100	ns
tWC	30		ns
tWH	10		ns
tWHR	60		ns
tWP	15		ns

ONFI Technical Highlights

- ONFI support is identified via Read ID, the standard NAND chip ID command
- NAND devices report their capabilities using the Read Parameter Page
- ONFI standardizes the base subset of commands required to be supported by all NAND devices
- ONFI supports increased performance through parallelism made possible by multiple LUNs and interleaved addressing
- ONFI standardizes the pin-out and packaging to ensure no PCB changes are required for a new NAND part

ONFI provides the solid technical base necessary to confidently build NAND-based products

ONFI Status

- ONFI workgroup working on defining the specification
  - Solid revision 0.7
  - 1.0 Release Candidate expected by September
- Strong industry backing
  - ONFI founders are Hynix, Intel, Micron, Phison, Sony and STM
  - ONFI members currently include Alcor Micro, Avid Electronics, BitMicro, Cypress, DataIO, Denali, InComm, Intelliprop, Marvell, Powerchip Semiconductor, Seagate, Silicon Motion, Skymedi, Spansion
- ONFI web site is at http://www.onfi.org/

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Summary

- Lack of standard makes it harder for platforms to support a range of NAND components, including components introduced at a later date
- Lack of standard NAND Flash interface impacts time to market and revenue
- ONFI is being developed to solve the barriers to the rapid adoption of new NAND products
- ONFI enables NAND feature self- identification, and standardizes command set, pin-out, and packaging

OPEN NAND
FLASH INTERFACE