Architecture Exploration for Flash-Based Systems

Presented by Darryl Koivisto

CTO, Mirabilis Design Inc.

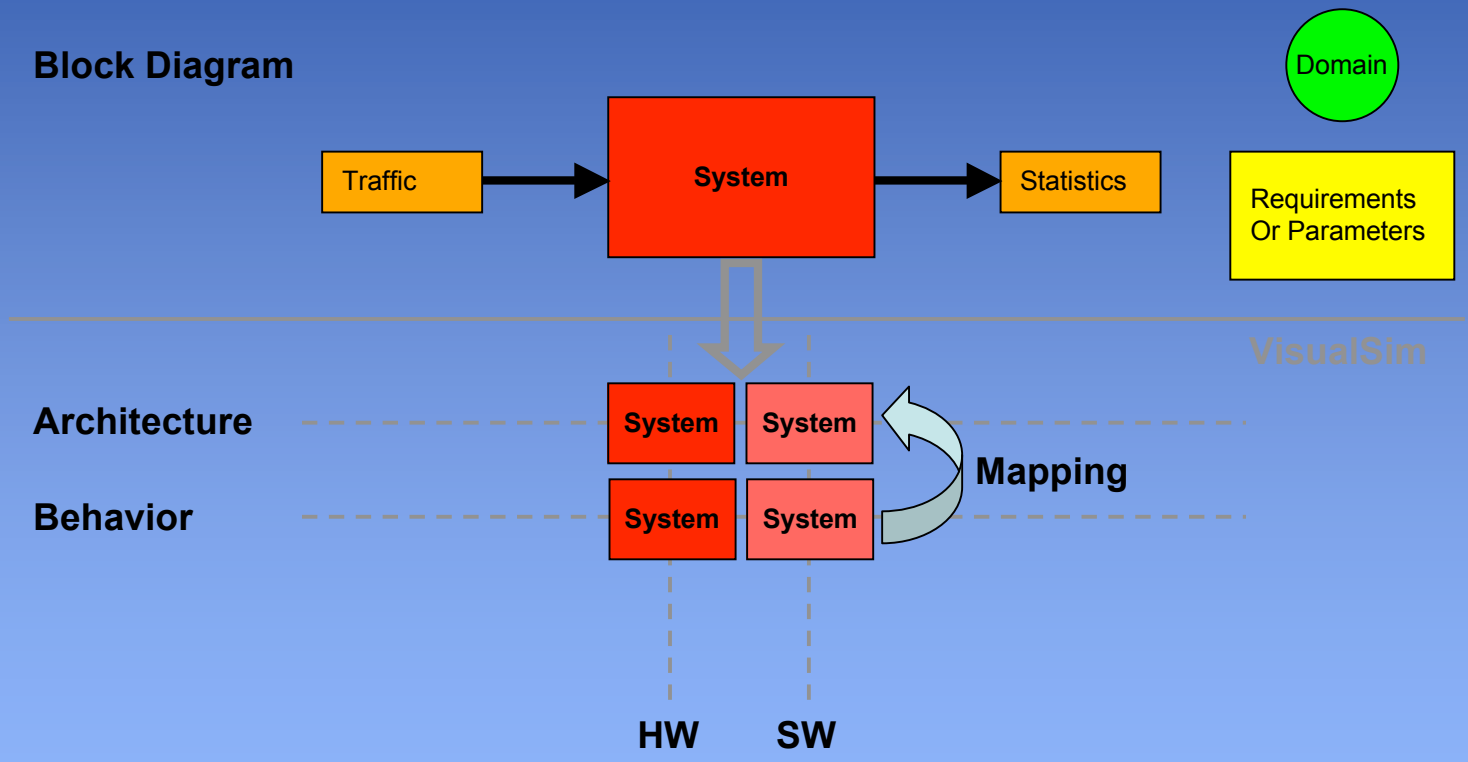
What is Architecture Exploration in the context of FLASH Memory?

- The ability to model FLASH memory in the context of actual system use for this common resource.
  - Model Abstraction
- Being able to accurately describe a FLASH memory in terms of system demands, application demands, and power considerations.
  - Model Traffic and Power Use
- Being able to obtain very useful statistics for elements of a typical system, such as processor, cache, SDRAM, or IO activity in terms of throughput, latency, or utilization.
  - Model Statistics: min, mean, max, and stdev

What are the advantages of FLASH Memory Architecture Exploration?

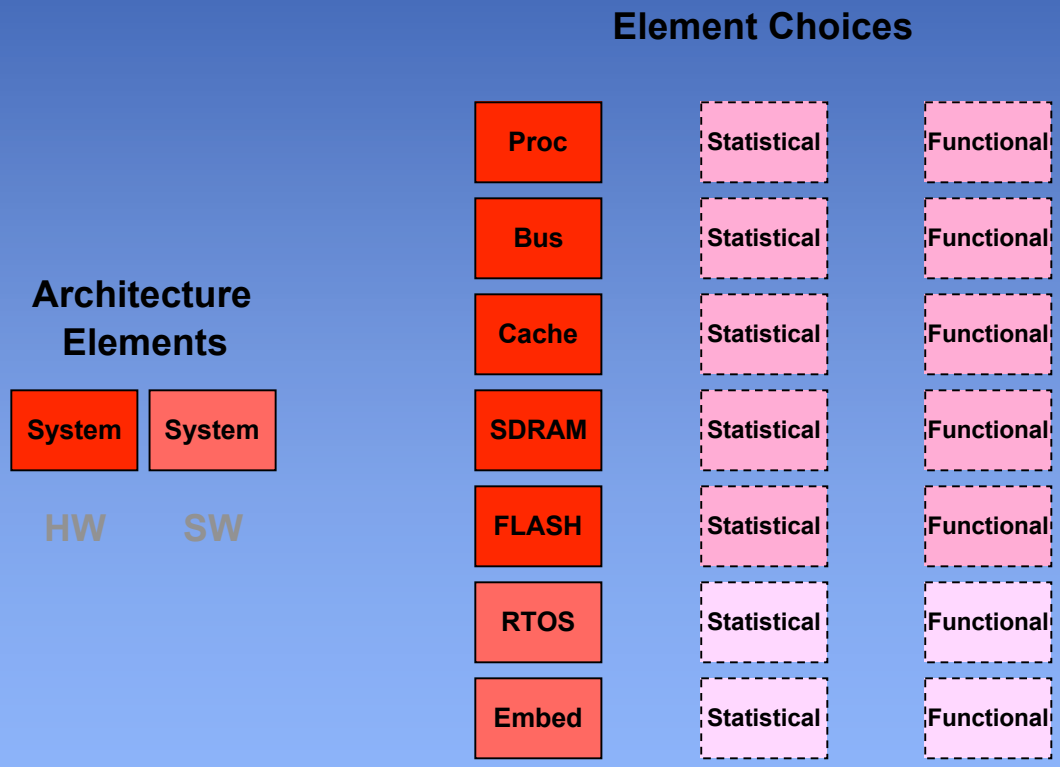
- In FLASH memory, complexity and concurrency can be difficult to determine the design effects of fast reads and slow writes.
  - Multi-Core Processors? Multiple DSP Hardware execution?
  - What is my video frame rate under worst case assumptions?
- One can determine peak usage of FLASH memory, whereas EXCEL spreadsheets can only provide average, or mean, estimates.
  - Is FLASH memory use less than 80% of peak utilization?
- Less Re-design, Re-spins.
  - Better Price-Performance of end product.
  - Higher Quality Design in less time.
  - More insight into Future Derivatives.

Modeling Views for FLASH Memory



Separating Behavior, Architecture, Software and Hardware.

Architectural View

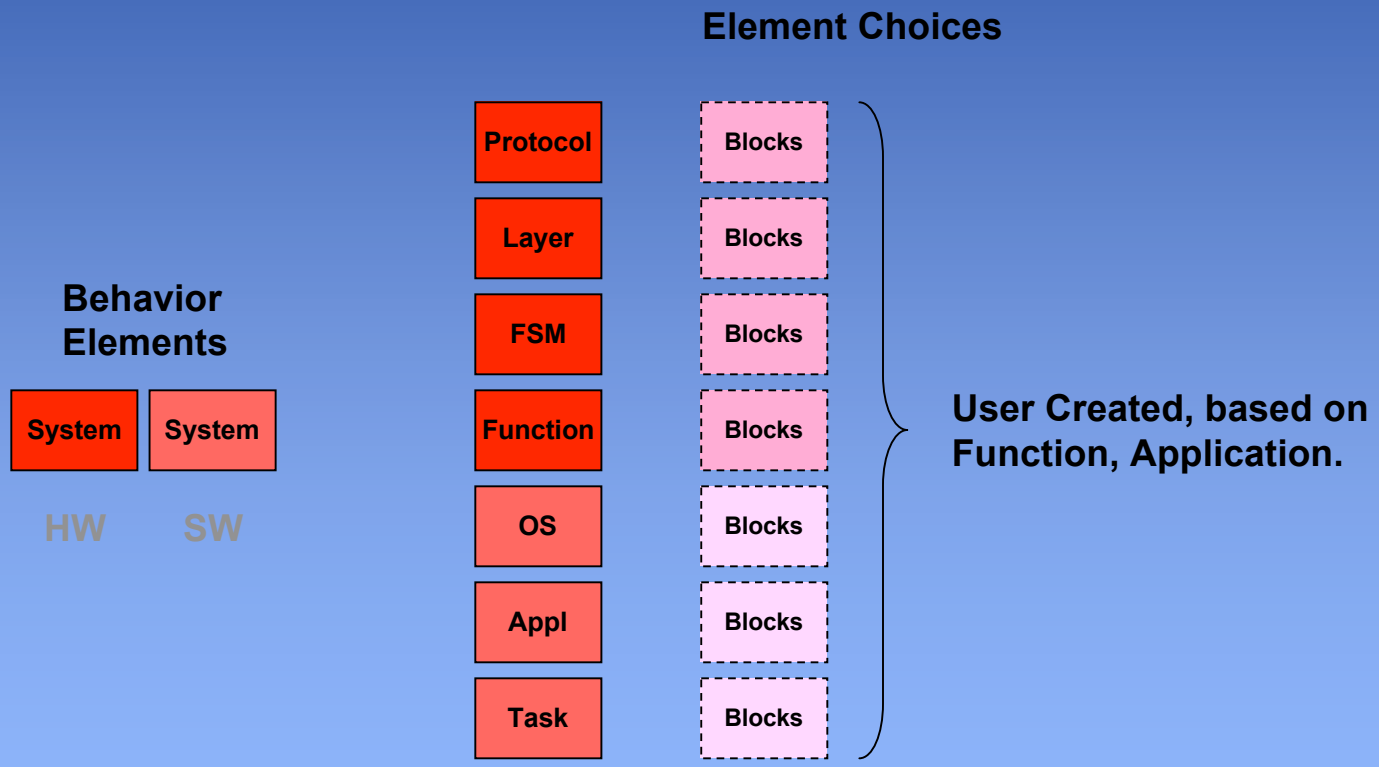


System Execution, Delays.

Architectural View, Library

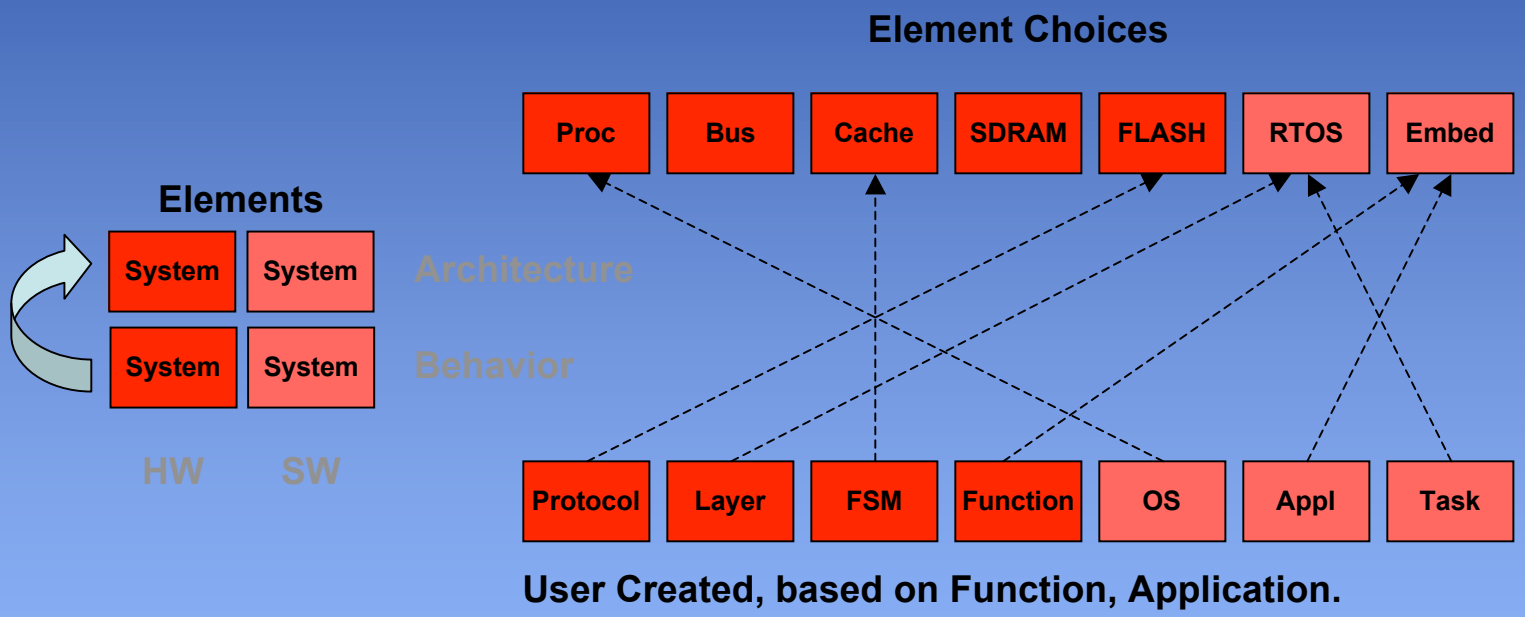
- Block Diagram oriented Hierarchical Blocks: Bus, Cache, RAM, FLASH, Processor (Registers, Pipelines, Parallel Execution, etc.), DSP, ASIC, FPGA, RTOS, SW Drivers, etc.
  - Plug-n-Play meaning they can be used interactively and in some cases recursively, such as processor pipelines.
  - Typical parameters include Speed_Mhz, Word_Width_Bytes, OH_Bytes, Burst_Size_Bytes, Source_Field_Name, Destination_Field_Name, Size_Bytes, Priority_Field_Name, etc.
- Performance Statistics Blocks: Latency, Throughput, Utilization
- Plotting Blocks: Linked to Statistics to selectively plot
- Power, Cost, Reliability, Switch-Over Blocks support for common subsystems, above.

Behavioral View



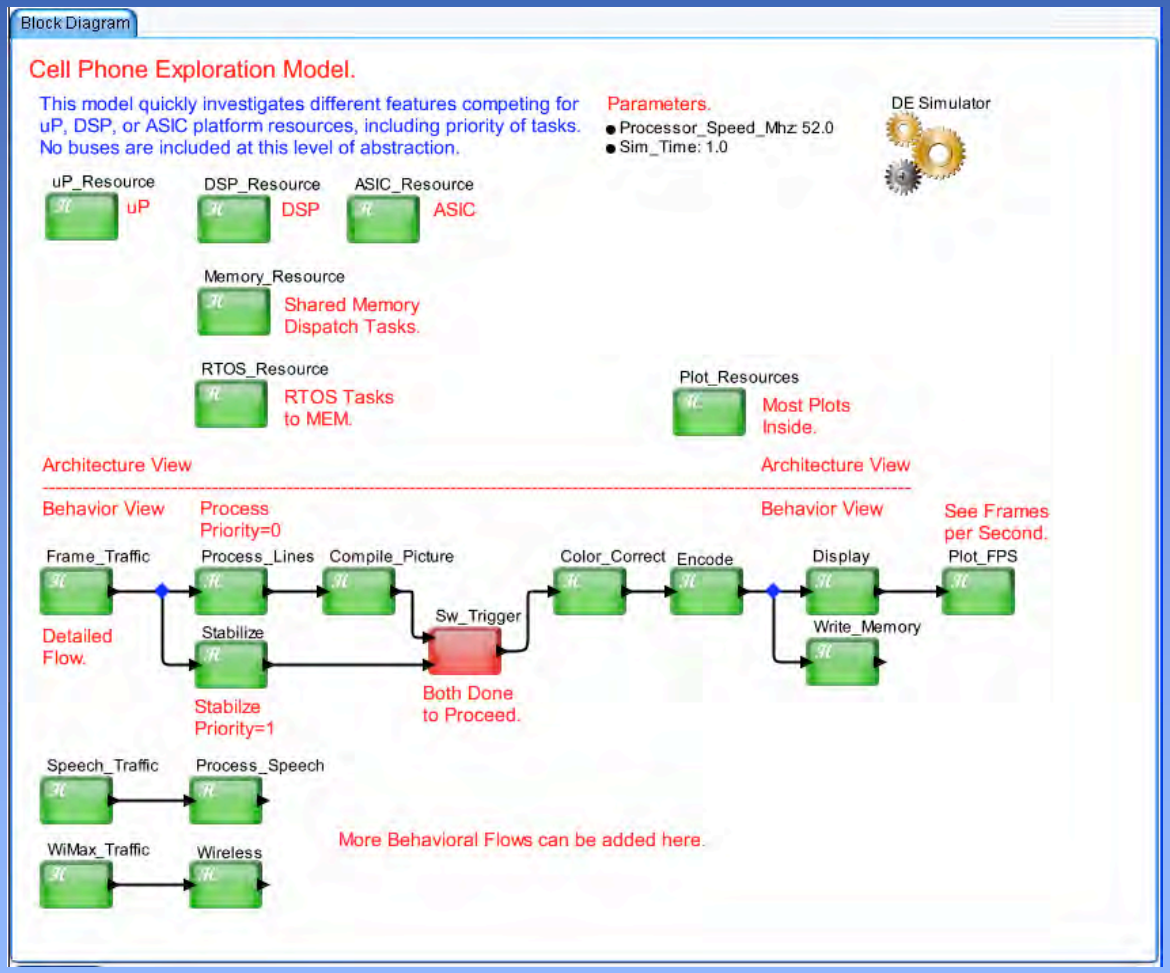
Typical System Flow, Algorithms, or States.

Mapping View

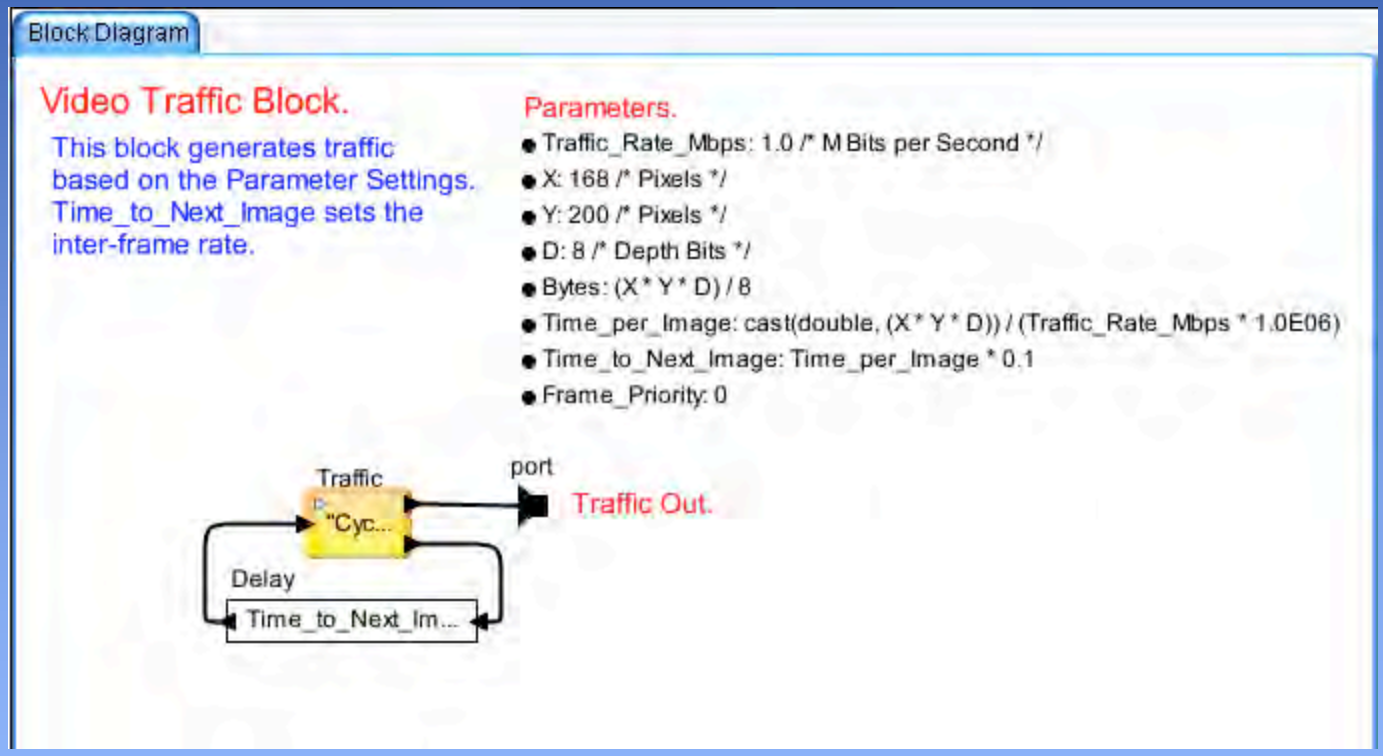


Static and Dynamic Mapping of Behavior to Architecture.

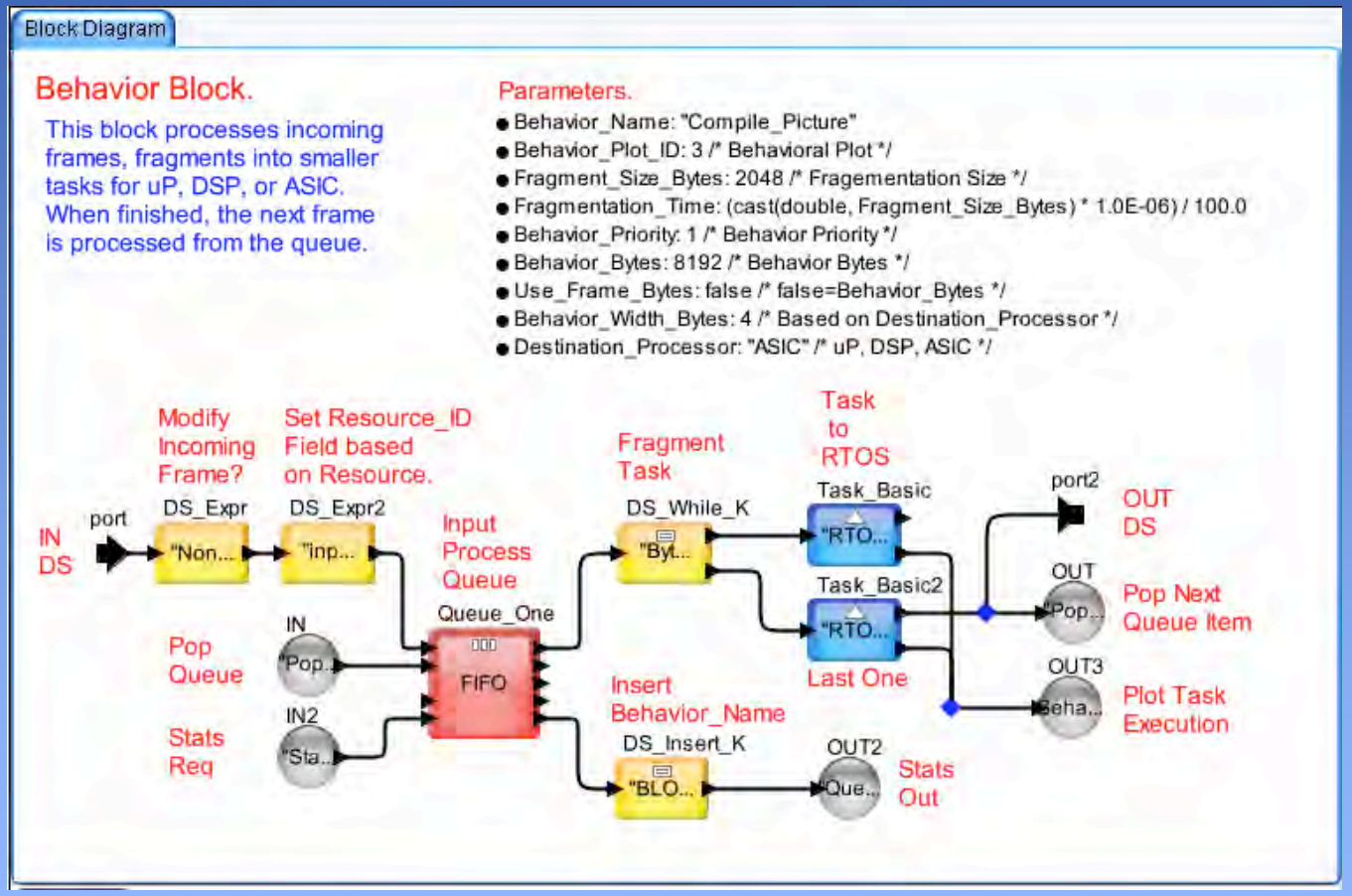
Model View


Block Diagram
Cell Phone Exploration Model.
This model quickly investigates different features competing for uP, DSP, or ASIC platform resources, including priority of tasks. No buses are included at this level of abstraction.
Parameters.
Processor_Speed_Mhz: 52.0
Sim_Time: 1.0
DE Simulator
uP_Resource
uP
DSP_Resource
DSP
ASIC_Resource
ASIC
Memory_Resource
Shared Memory Dispatch Tasks.
RTOS_Resource
RTOS Tasks to MEM.
Plot_Resources
Most Plots Inside.
Architecture View
Architecture View
Behavior View
Process Priority=0
Behavior View
See Frames per Second.
Frame_Traffic
Process_Lines
Compile_Picture
Color_Correct
Encode
Display
Plot_FPS
Sw_Trigger
Write_Memory
Detailed Flow.
Stabilize
Stabilze Priority=1
Both Done to Proceed.
Speech_Traffic
Process_Speech
WiMax_Traffic
Wireless
More Behavioral Flows can be added here.

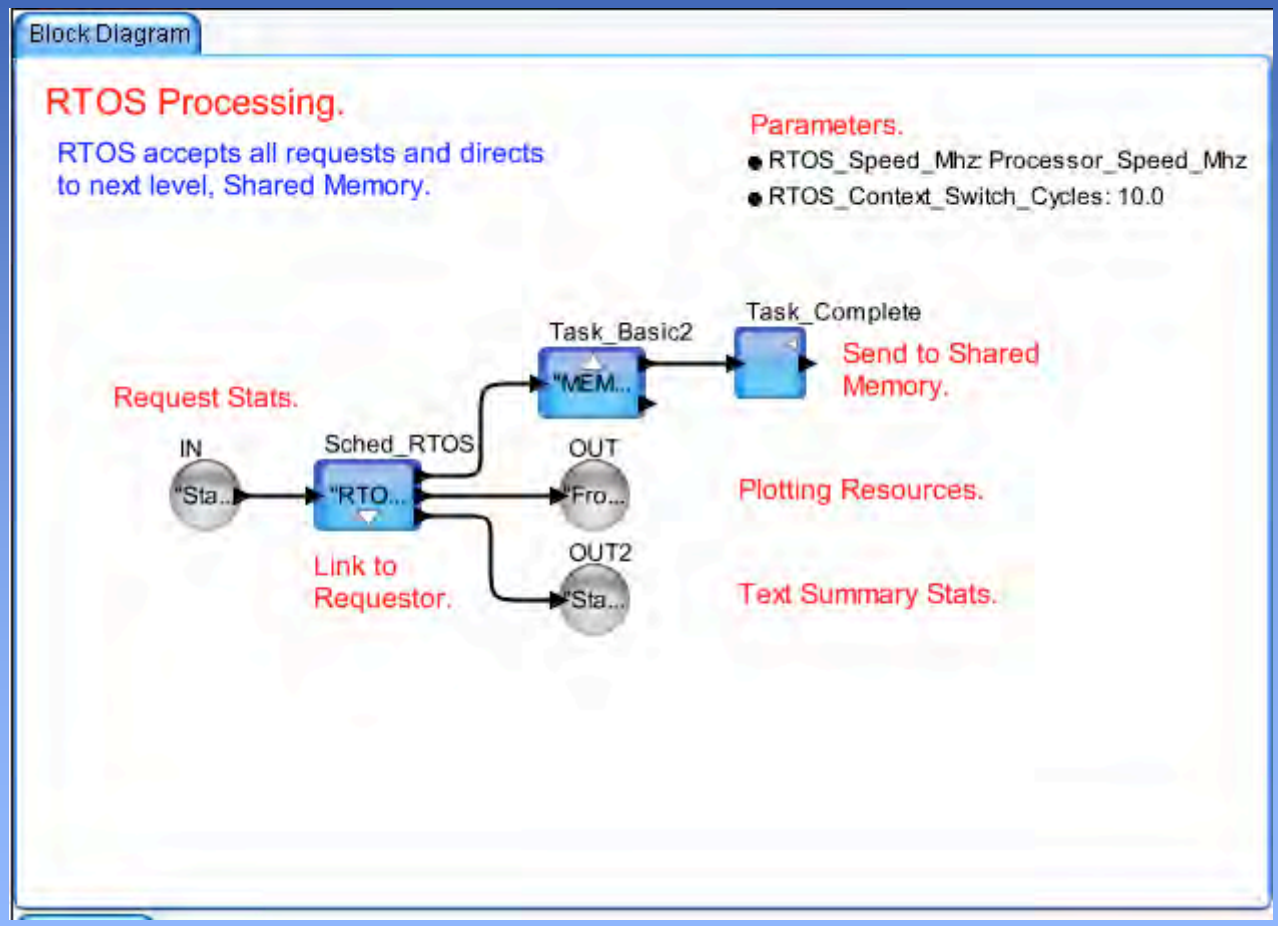
Model Traffic



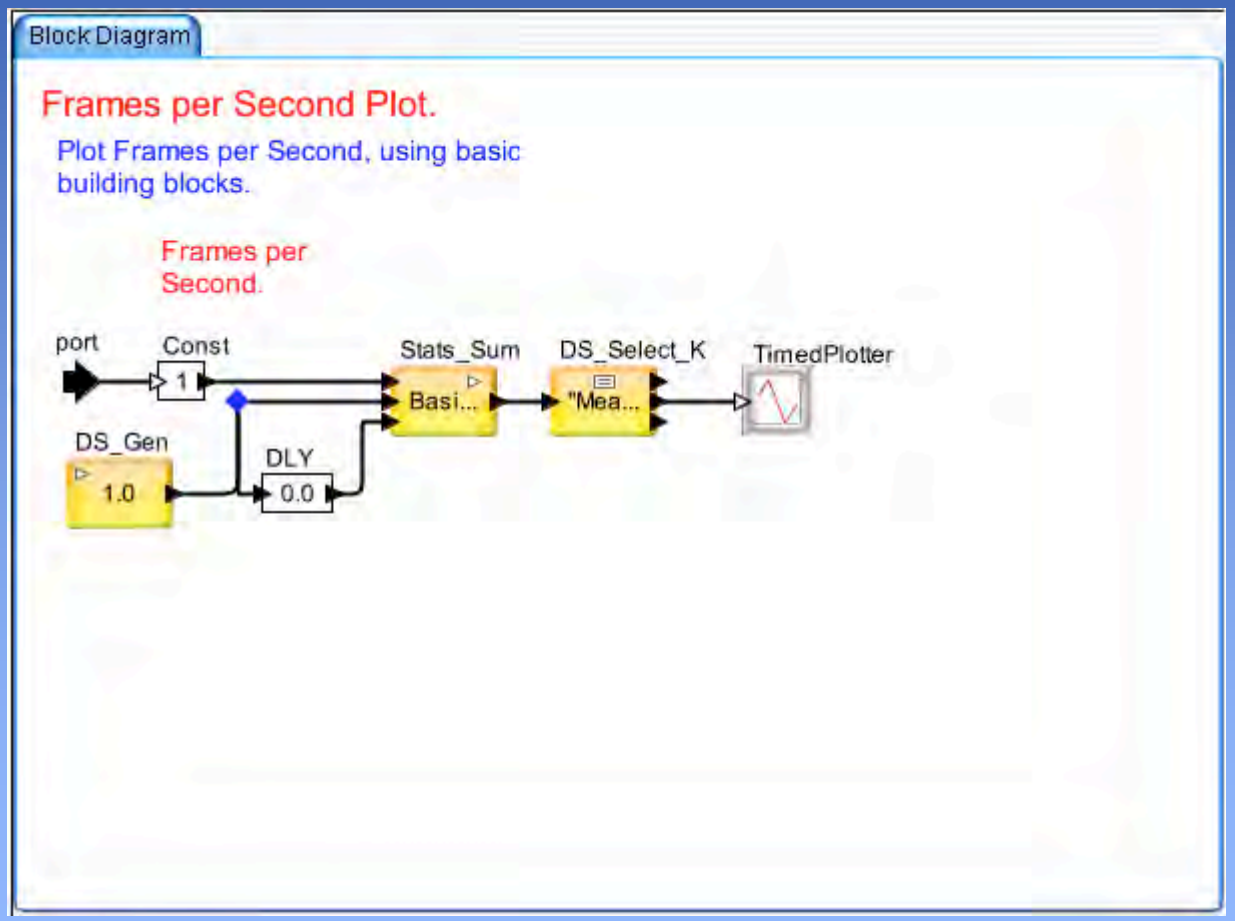
Model Behavioral Element



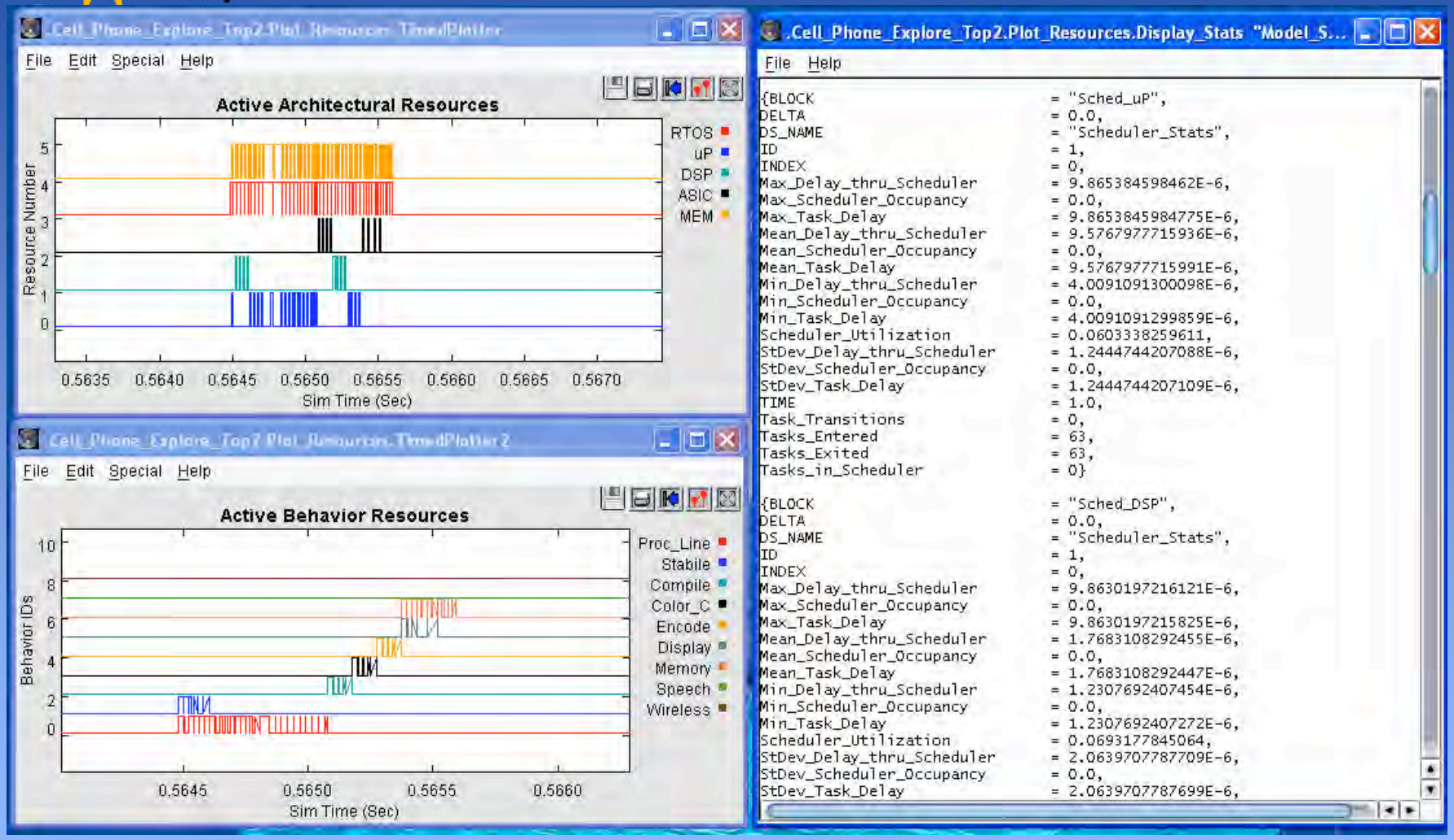
Model Architectural Element



Model Statistics



FLASH Memory Output



Darryl's Industry Association

- Over 30 years of system design experience
- Developed first Channel Interface design package at Amdahl
- CTO of Mirabilis Design's VisualSim performance simulator
- Created new methodology for architecture exploration of memory sub-systems and channels
- Chip Design
  - Signetics/Philips.
- Hardware Architecture
  - Amdahl.
- Software Architecture, System Architecture
  - Ford Aerospace/Loral.
- Software Modeling Tools
  - Systems and Networks, Cadence Design, Mirabilis Design.