NAND Error Correction Code Choices

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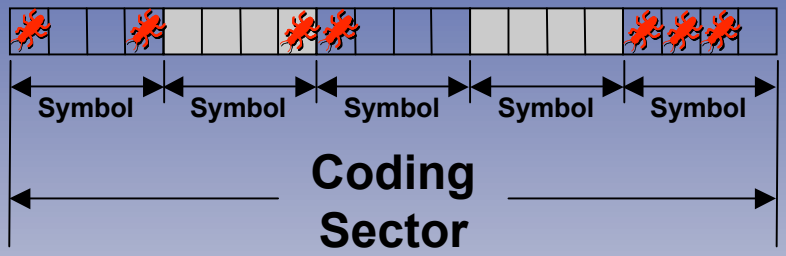
NAND Error Correction Choices

- Leading edge NAND requires multiple bit error correction
  - Hamming codes only correct single bit errors
  - Reed-Solomon
  - Binary BCH
- Metrics
  - Overhead requirements
  - Correction performance
- Reed-Solomon and binary BCH have different underlying structures: one is *symbol-based* and the other is *binary*

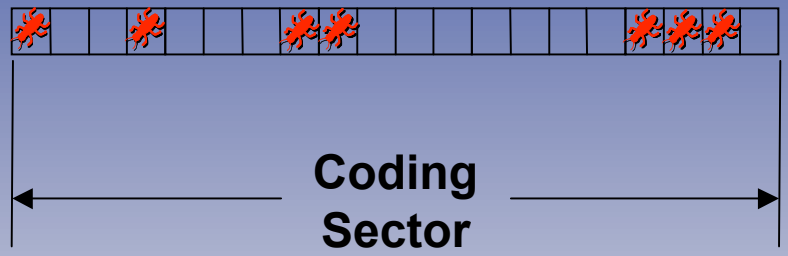
Comparing Symbol-Based to Binary Error Coding

Symbol-Based Code



- Symbol length: $m = 4$ bits
- Code length: $n = 5$ symbols
- Bit errors = 7
- Symbol errors = 4
- Error correction: $t = 4$
- Max error pattern: $t * m = 16$ bits

Binary Code



- Symbol length: $m = 1$ bit
- Code length: $n = 20$ symbols
- Bit errors = 7
- Symbol errors = 7
- Error correction: $t = 7$
- Max error pattern: $t * m = 7$ bits

Note – Code examples were shortened for demonstration purposes. Actual codes have strict relationships among the parameters that define the code like n, m and t.

Comparing Symbol-Based to Binary Error Coding

- **Common ECC Choices for MLC NAND**

Reed-Solomon

- Symbol length: *m* = 9 bits
- Code length: n = 470 symbols (528 bytes)
- Error correction: *t* = 4
- Redundancy[1] requirements: *2tm* = 72 bits
- Max error pattern: *t*m* = 36 bits

Binary BCH

- Symbol length: *m* = 1 bit
- Code length: n = 4224 symbols (528 bytes)
- Error correction: *t* = 4
- Redundancy[1] requirements: *13t* = 52 bits
- Max error pattern: *t*m* = 4 bits

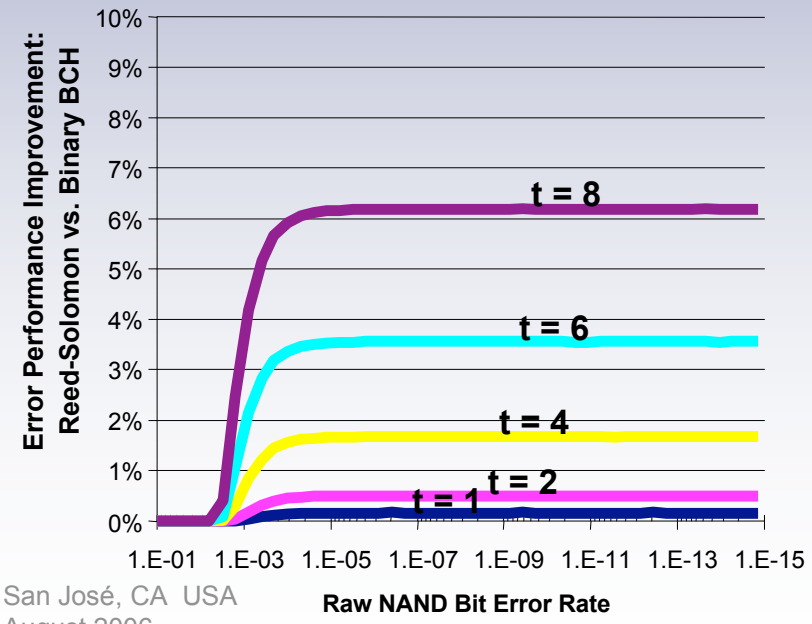
RS requires 39% more code redundancy for a given error correction.

RS can correct more bit errors but what does that mean for NAND Flash?

Note: (1) Redundancy is also referred as code overhead or parity and for NAND is typically stored in the spare area

Comparing Error Correction Performance

- Comparison of correction performance must be done in the context of the channel error conditions
- NAND error events are random and uncorrelated
- For NAND, Reed-Solomon corrects a few percent more error conditions than binary BCH
- A few percent change in error correction garners a generally insignificant improvement in the application bit error rate



Designed Error Correction Level	Typical Application Bit Error Rates(1)	
	Reed-Solomon	Binary BCH
t = 1	$2.34e^{-15}$	$2.34e^{-15}$
t = 2	$7.69e^{-15}$	$7.73e^{-15}$
t = 4	$3.41e^{-15}$	$3.47e^{-15}$
t = 6	$3.59e^{-14}$	$3.72e^{-14}$
t = 8	$3.09e^{-15}$	$3.28e^{-15}$

Notes:
1. Bit error rate is the ratio of error bits to the total number of bits read.

Conclusions

- Binary BCH is a better ECC solution for NAND than Reed-Solomon
  - 39% Reduction in code redundancy
  - Practically identical application-level performance

Thank You!

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