

An Introduction to Emerging Memory Technologies

Greg Komoto Manager, Strategic Planning Flash Memory Group Intel Corporation Email: greg.l.komoto@intel.com





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- Overview of Emerging Memory Alternatives
- Near Term Candidates
- Longer Term, Litho Defined Candidates
- Non Litho Defined Candidates
- Conclusions

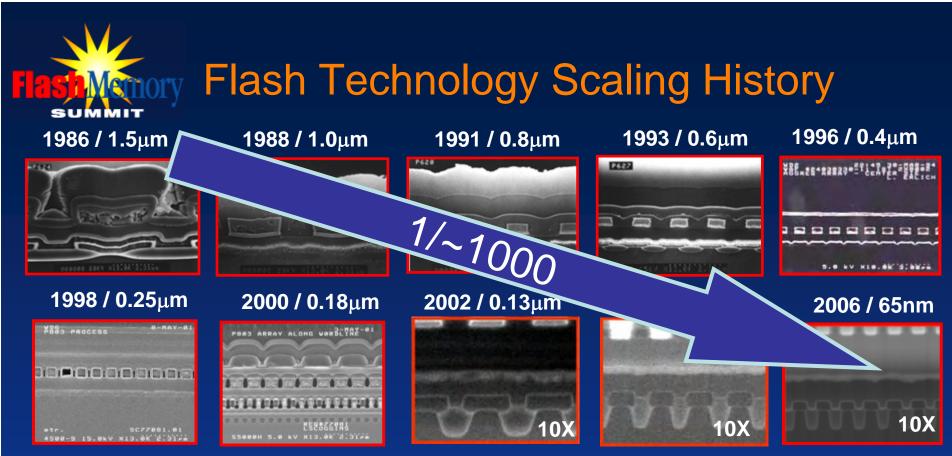




Overview of Emerging Memory Alternatives

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Volume Production Year / Technology Generation

Source: Intel

- Flash Invented in mid 1980's
 - NOR flash evolved from EPROM
 - NAND started as poly-poly erase cell later evolving to present structure
 - ~20 years & 10 Generations of High Volume Production
 - 8+ years & 5 Generations of MLC: 2bit / cell





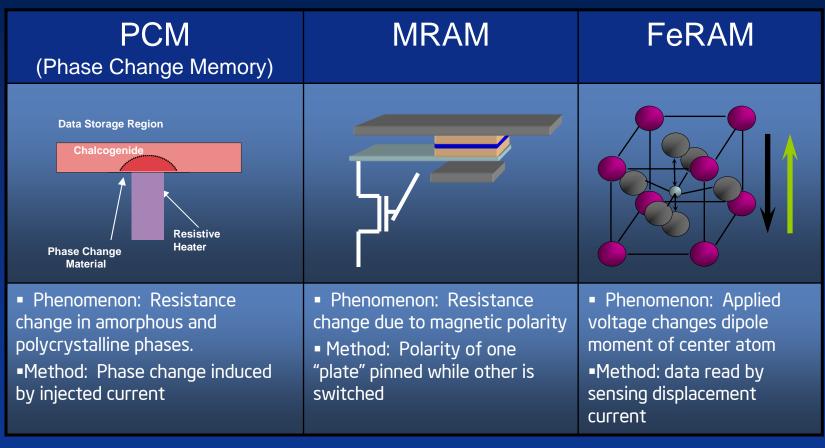
	Today	Тотоггом	Future	
	Evolutionary SRAM	Floating Trap Metal Gate Nano Dot Barrier Engineering	Multi Layer 3D 3D Gate	
	<i>Emerging Alternatives</i>	FeRAM MRAM PCM	Multilayer 3D RRAM Bridging/Ionic Molecular Probe Storage e-Beam	
Focus of Today's Tutorial				



- Overview of Emerging Memory Alternatives
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Key Attributes

- 1C + 1 Transistor
- Cell Area: 25F² shipping
- Cell Area: 12-15F² demonstrated

Advantages

- Fast R/W performance
- Low power operation
- **Bit alterable (no erase)**

Issues

- Scaling path <100 nm
- **Destructive read**
- Read & Write limited ($1e^6 \rightarrow$ $1e^{10}$)

E_{App} E_{Film}

No path to flash/dram level costs

Applied Electric Field Moves Center Atom

> Perovskite Crystal Unit Cell PZT (PbO,ZrO₂, TiO₂) Lead-Zirconate-Titanate

Tetra/Pentavalent Atom

Di/Monovalent Metal Atoms



Non- Linear FRAM Capacitor

Top Electrode

PZT Film Polarized

Bottom Electrode

 $\overrightarrow{\mathsf{E}}_{\mathsf{Net}} = \overrightarrow{\mathsf{E}}_{\mathsf{App}} - \overrightarrow{\mathsf{E}}_{\mathsf{Film}}$





Key Attributes

- 1MTJ + 1 Transistor
- Cell Area: 35F² shipping (Toggle)
- Cell Area: 6F² theoretical (STT)

Advantages

- "Unlimited" R/W endurance
- Fast R/W latency (<35 ns)
- Bit alterable (no erase)

Issues

- Scaling path
- Write disturbs, power
- New materials, CMOS compatibility
- No path to flash/dram level costs





Phase Change Memory (PCM)

Key Attributes

- IR + 1 select
- Cell Area: 5.5-12F2 sampling
- Cell Area: <6F2 demonstrated</p>

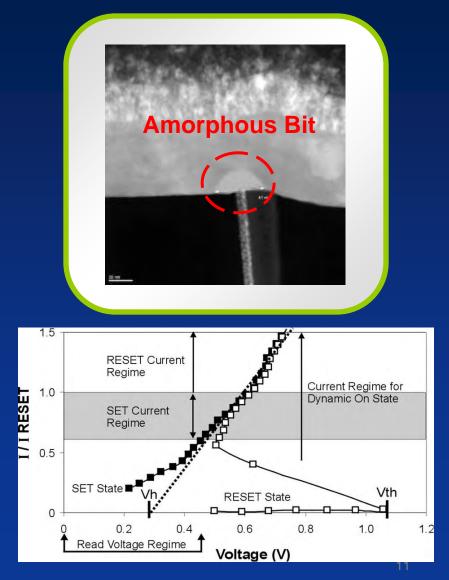
Advantages

- Clear scaling path to <20 nm
- Ease of CMOS integration
- Fast, "unlimited" read
- Bit alterable (no erase)

Issues

- Write endurance limited: 1e6 to 1e12
- Write latency vs. DRAM







Emerging Alternative Memory Attribute Comparison

Key Metrics	РСМ	MRAM	FeRAM
Cell Size	~SBC NOR/NAND (5.5-12F ² → <5F ²)	Larger (35 F² → 6-16F²)	Largest (32F ² → 12-15F ²)
CMOS Integration	Good	Fair to Poor	Fair
Scaling	Excellent	Fair: current, materials	Poor: materials, 3D
Read Latency	Fast, ~NOR	Fastest, ~ xRAM	Fast, ~NOR
Write Speed/Power	~Flash → Higher	Fastest latency, high power	Fast – RAM like
Bit Alterable?	Yes	Yes	Yes
Read Endurance	Unlimited	Unlimited	Limited
Write Endurance	High	Unlimited	Higher
Logic Integration	Easiest	Harder	Easier
Application Reach	Flash + Most RAM + Embedded Memory	Embedded/Cache Memory	Embedded Memory



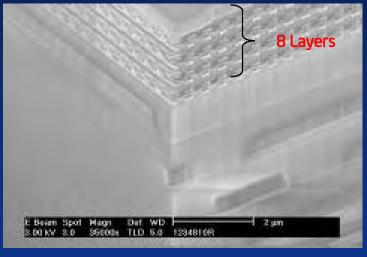
Source: Intel



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Future Research Trend: Extending in Multiple Layers



Source: Intel

R&D Example (circa 2003): Read/Write Eight Layer Memory using Ferroelectric Polymer

- Litho defined memories seeking to extend scaling in vertical dimension
 - Industry work on everything from NAND to polymer
- Ideal Effective Cell Area: Z = 4F² / y Where y = # of layers
- Challenge is manufacturing cost of multiple layers





Other NVM Candidates in the Longer Term Research & Discovery Phase (Part 1 of 2)

Material	Structure	Description	Effect		
RRAM		Resistance change in CMO (usually crosspoint and multilayer)	Resistance change based on an applied field		
Ferroelectric Polymer	Word line Word line Polymer Layer Bit line Polymer Layer Word line	Cross-point, multi- layer capacitive storage in Polymer	Change in capacitance based on an applied field		
Resistive Polymer		Cross-point, multi- layer resistive storage in Polymer	Change in resistance based on an applied field		
Source: Intel					



Intel

Other NVM Candidates in the Longer Term Research & Discovery Phase (Part 2 of 2)

Material	Structure	Description	Effect
Programmable Metallization		Silver Dissolved in Chalcogenide	Field Driven "Electroplating"
Carbon Nanotube		Cross Point Array of Nanotubes Switches	Electrostatic Attraction + Van der Waals Adhesion
	Carbon Nanotube	CNT as Circuit Element	CNTs as replacement structure
Molecular	Image Courtesy of the University of Sydney	Molecules in CrossPoint Array	Voltage Driven Change in electronic states in Redox

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Source: Intel



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Seek & Scan Probe Storage

Cartoon of Nano Dimension Atomic Level Probe contacting single molecule memory

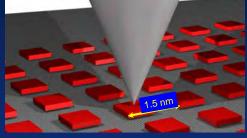


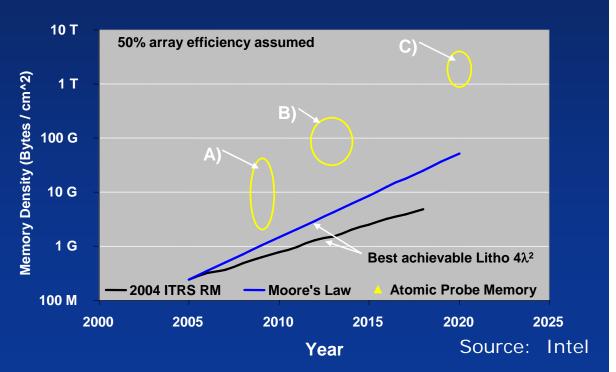
Image Courtesy of the University of Sydney

Best achievable memory density projections over time:

- A) IBM Millipede today
- B) Improved storage media
- C) Full molecular memory storage capability

Seek & Scan Probe (SSP):

- •MEMs device with nanopositioned probe tips
- •Employs alternative storage media
- •Molecular level storage is ultimate goal

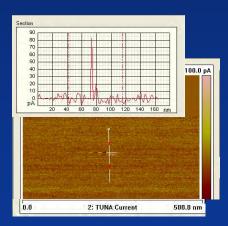


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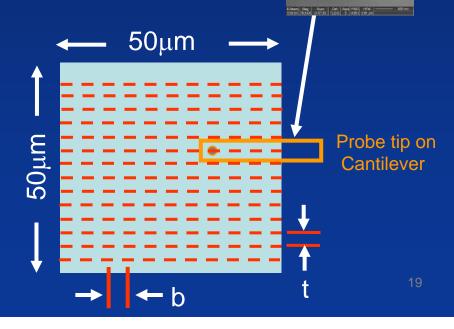
- Bit size: Determined by Media & Tip interactions
- Track Pitch/Position: Determined by Nano-positioning
 - Motor resolution < 1nm resolution reported
- Tip Scaling: Determined by tip field focusing
 - Tip shape & media fields & current distribution

Probe tip





Source: Intel





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- Flash memory technology working to address scaling challenges
- New memory technology is rare
 - Last to break beyond a niche was flash ~20 years ago
- Phase Change Memory is the most promising of near-term candidates
- Multi-level, 3D and MEMS devices hold most promise for the future





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