Flash Memory SUMMIT

NOR to NAND
a Software Perspective

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August 2007

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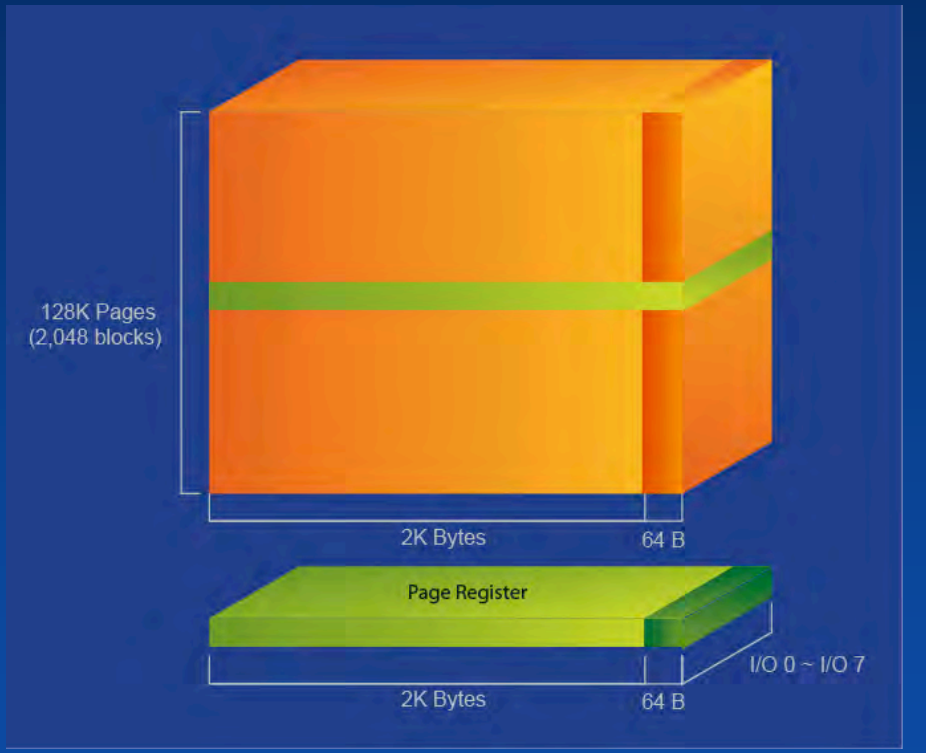
In the Beginning, There Was NOR

- RAM style interface = easy integration
- Entire memory is good – No bad blocks
- Code executes in place (XIP)
- Fast read performance

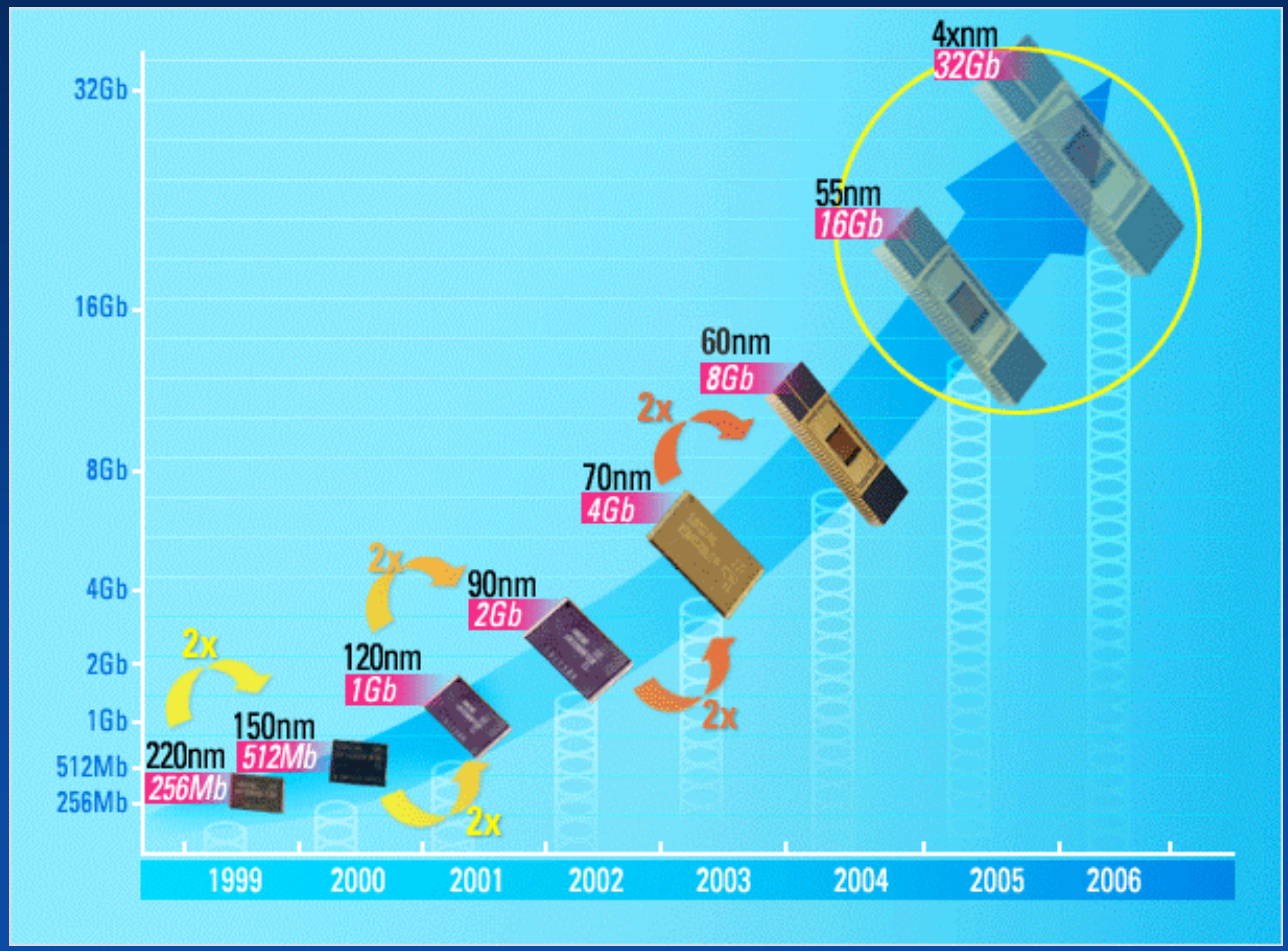
- Slow write & erase performance
- Cost per bit relatively high

Then, along came NAND

- Lower cost per bit
- Densities are much greater
- Non-standard memory Interface: H/W & S/W (Access in pages not bytes)
- Bad blocks exist when new and increase during use

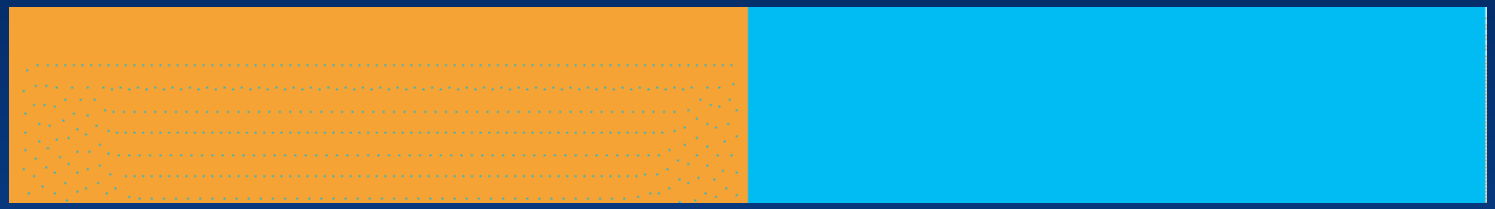


NAND Density Increasing



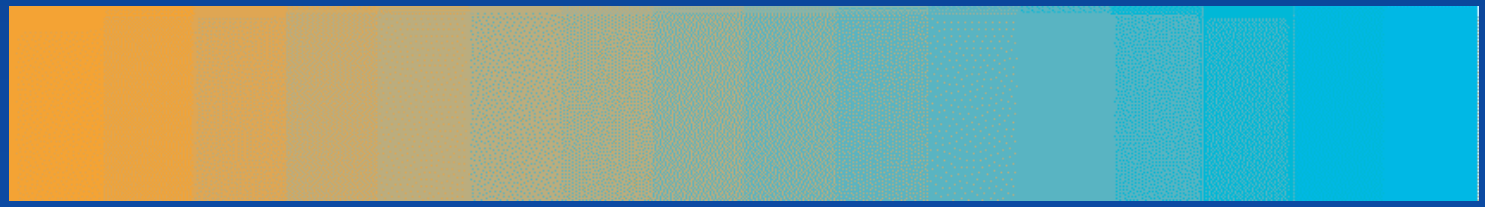
NAND: More Bits = More Complex

SLC
1-Bit/Cell
2 Levels



MLC
2-Bit/Cell
4 Levels

4-B/C
4-Bit/Cell
16 Levels



Read/Write Speed and Endurance vs Cost Per Bit

	SLC	MLC	4-bit/Cell
Read Performance	1x	0.5x	0.4x
Write Performance	16x	6x	1x
Endurance	100,000	10,000	<1,000
Cost/bit	1x	0.6x	.4x

Must Match the ECC (t) to the Application's Target Bit Error Rate (BER)

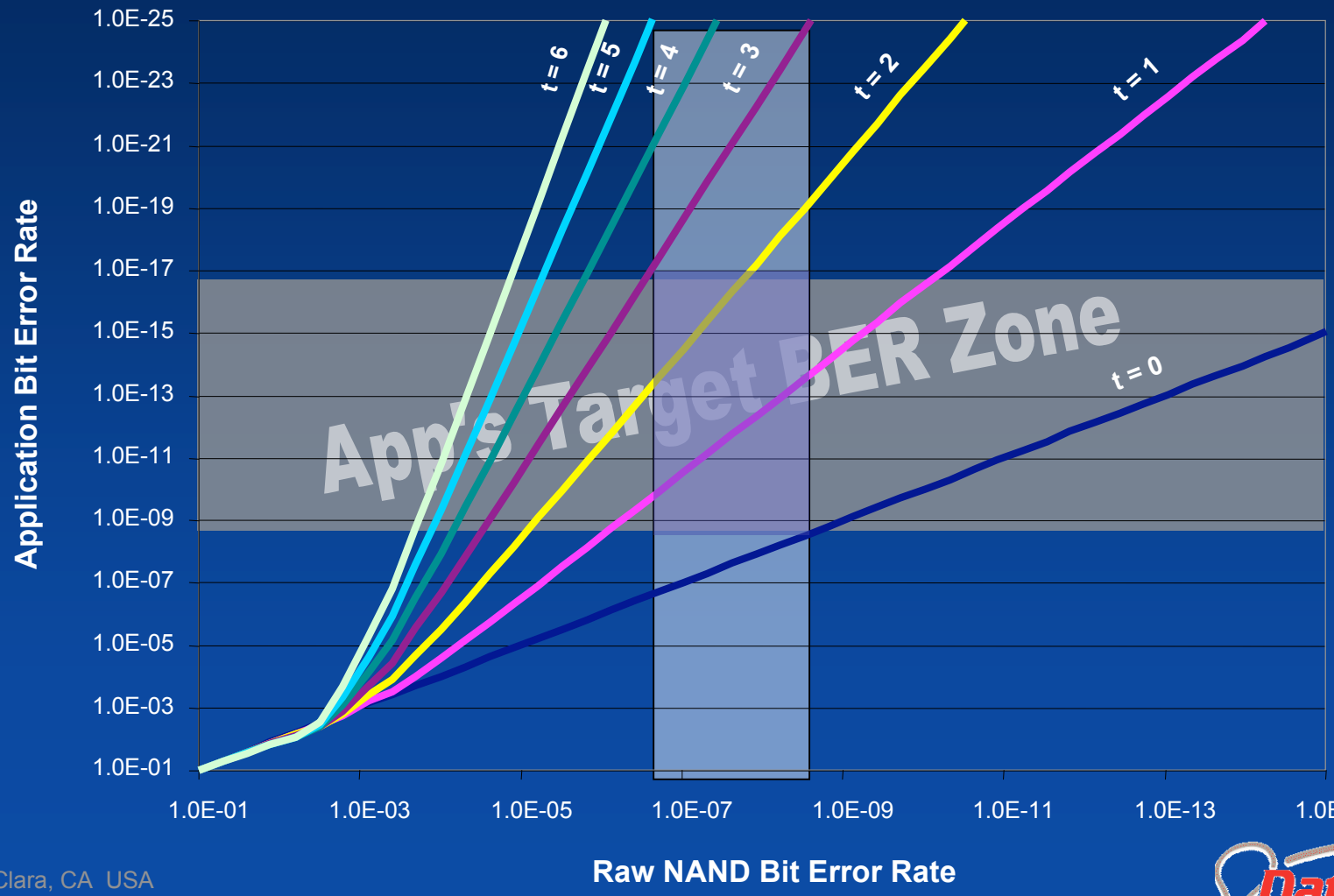
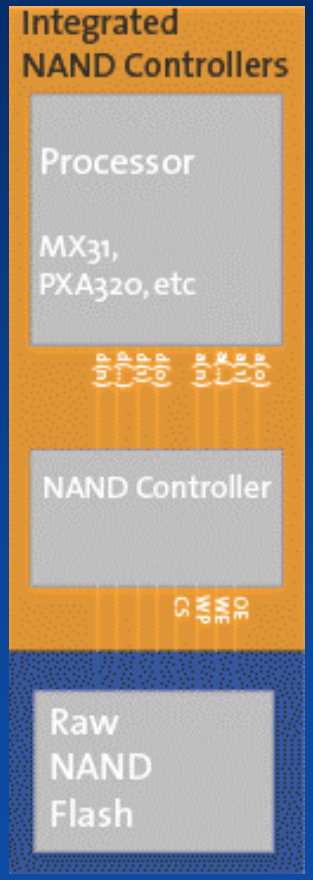
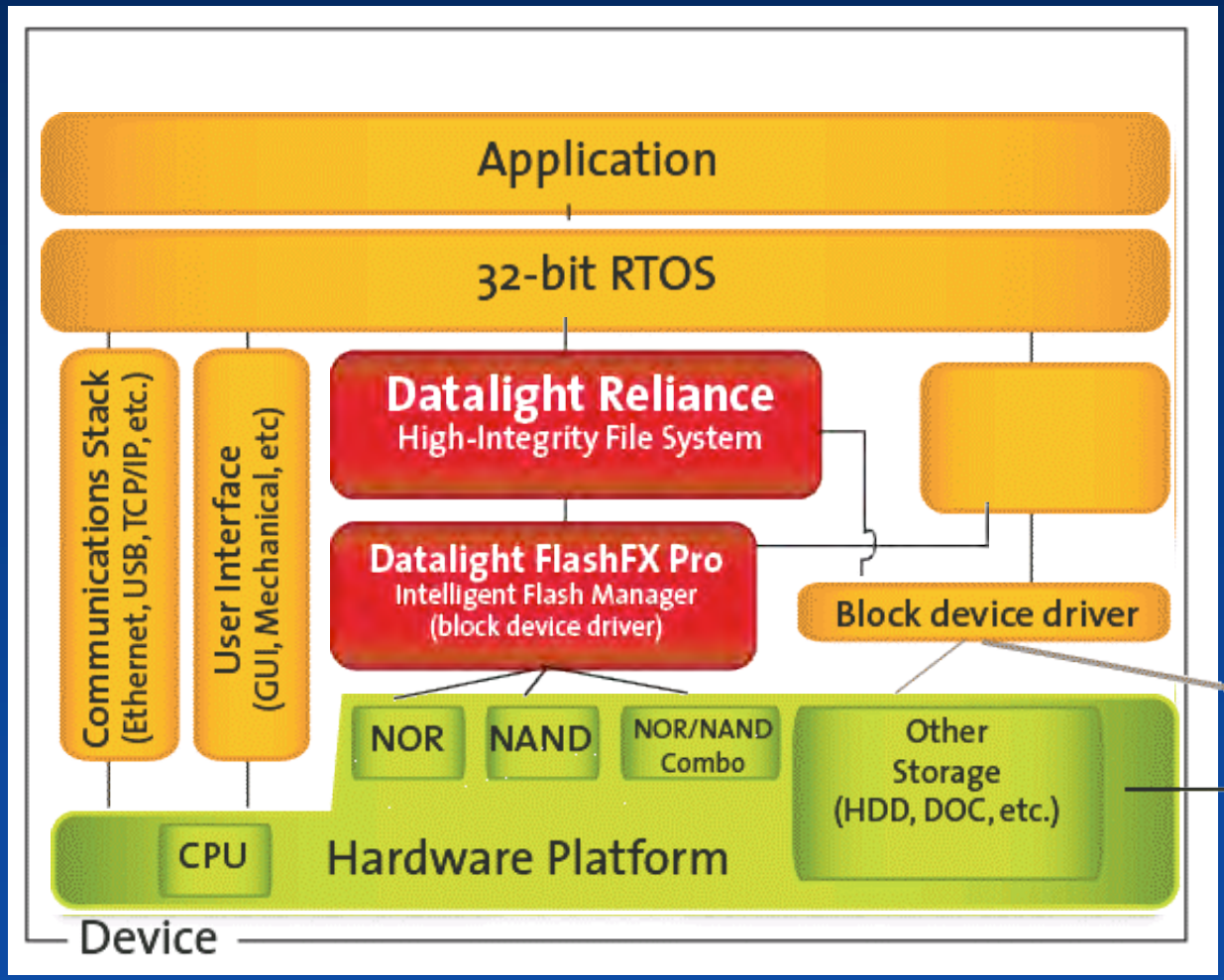


Chart courtesy of Micron Technology. Used with permission

NAND Controllers Simplify Hardware Integration and Handle ECCs

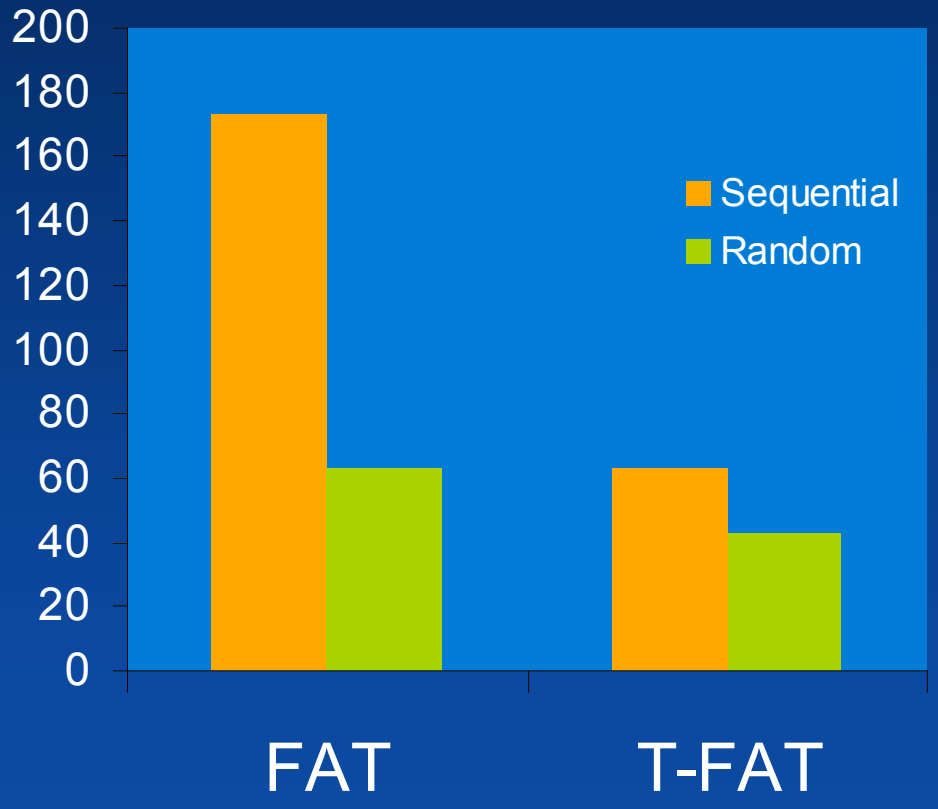


The Role of Software



File System Efficiency Effects NAND Flash Life

- Traditionally, reliability & r/w speeds are a tradeoff
- Extra data written to safeguard reliability may overstress flash
- Performance means fast reads & writes, AND efficient file system operation



Points to Consider

- NOR is best for code, but can store data
- NAND is best for data, but much more complex to integrate and use
- Higher density NAND has lower cost per bit, but lower endurance and performance, too
- NAND controllers built into CPU or NAND simplify hardware integration, but complicate software integration
- Entire software stack impacts reliability, flash life and system performance