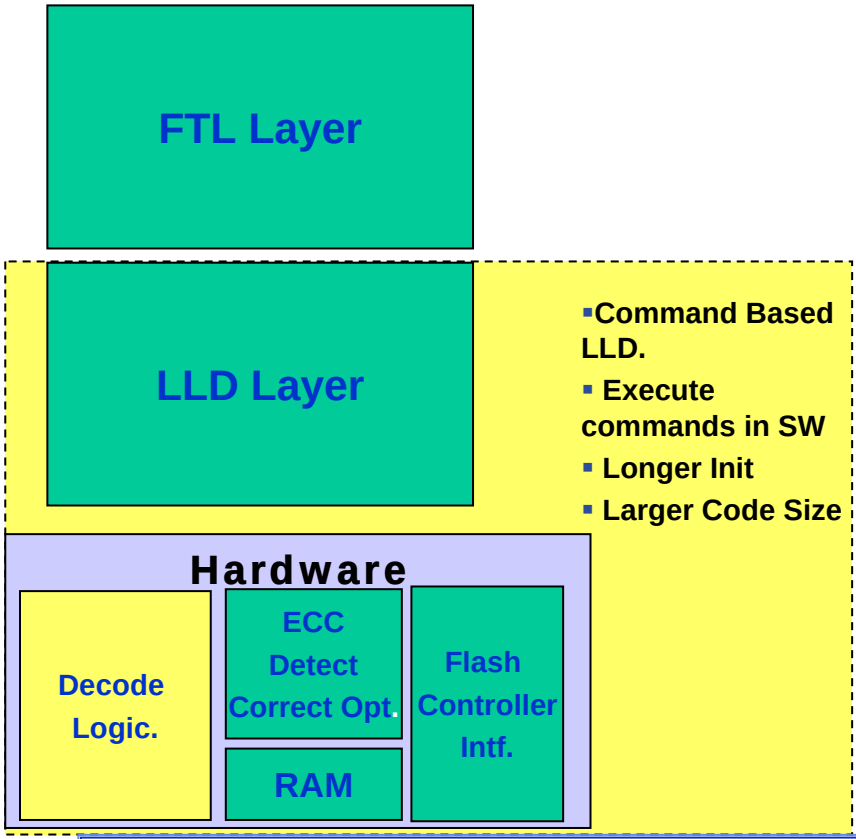
NAND Flash Boot

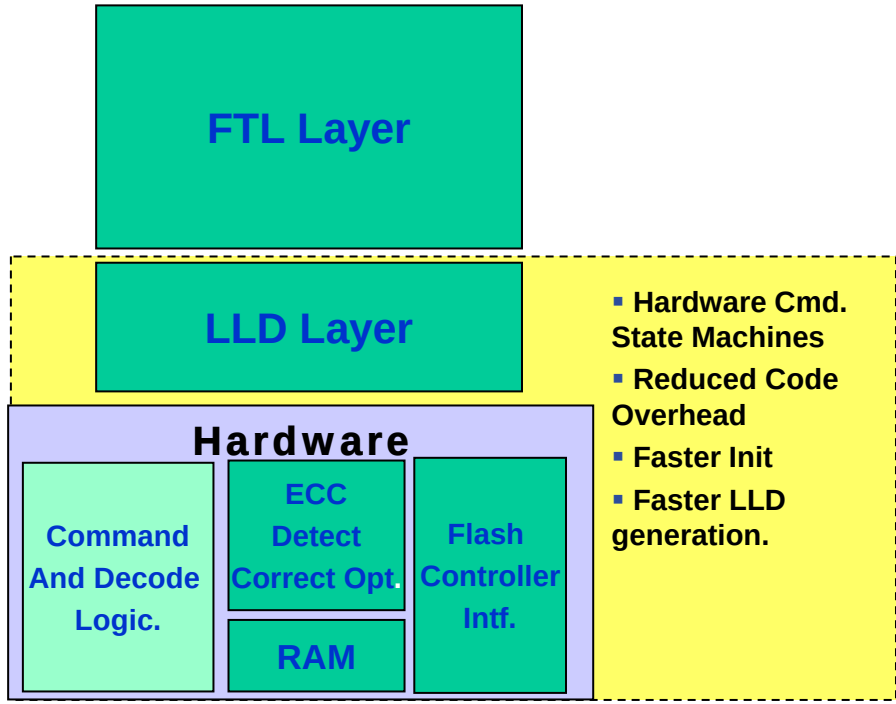
By Bob Pierce
Denali Software

Major Booting Issues

- Reliable Boot Image
- Boot Image transfer time
- Silicon Area
- Known good Boot Block
- Error Correction Latency (BCH)
- Controller initialization
- Multi Images
- Loading multiple stages
- At Speed ECC detect/correct
- Boot loader
- Flash Architecture

Architectures





- Different Architectures have a huge impact on your System
- Hybrid Solutions are very flexible
- Software Solutions Provide the highest Flexibility
- Verification is the Key to either Architecture

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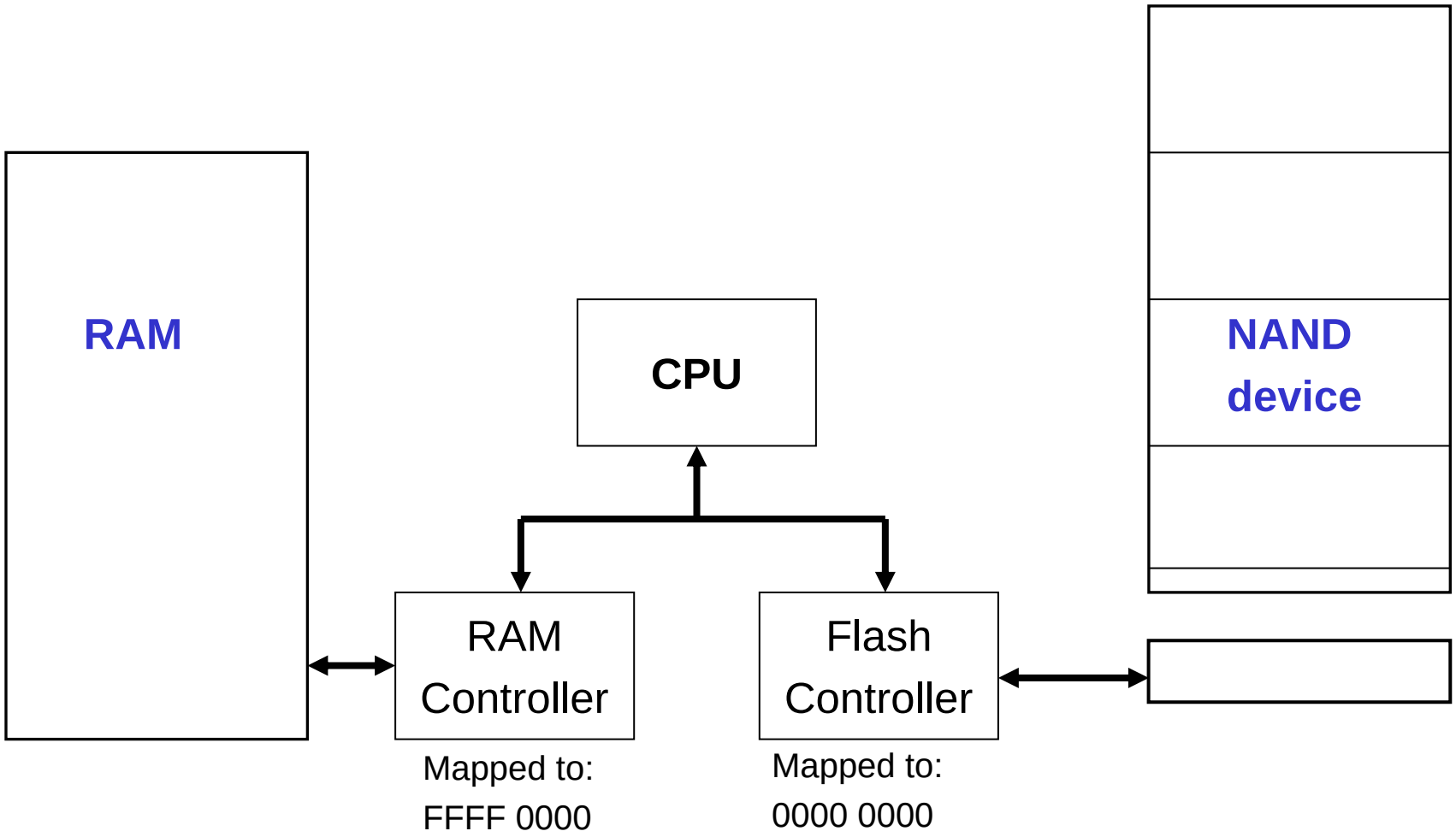
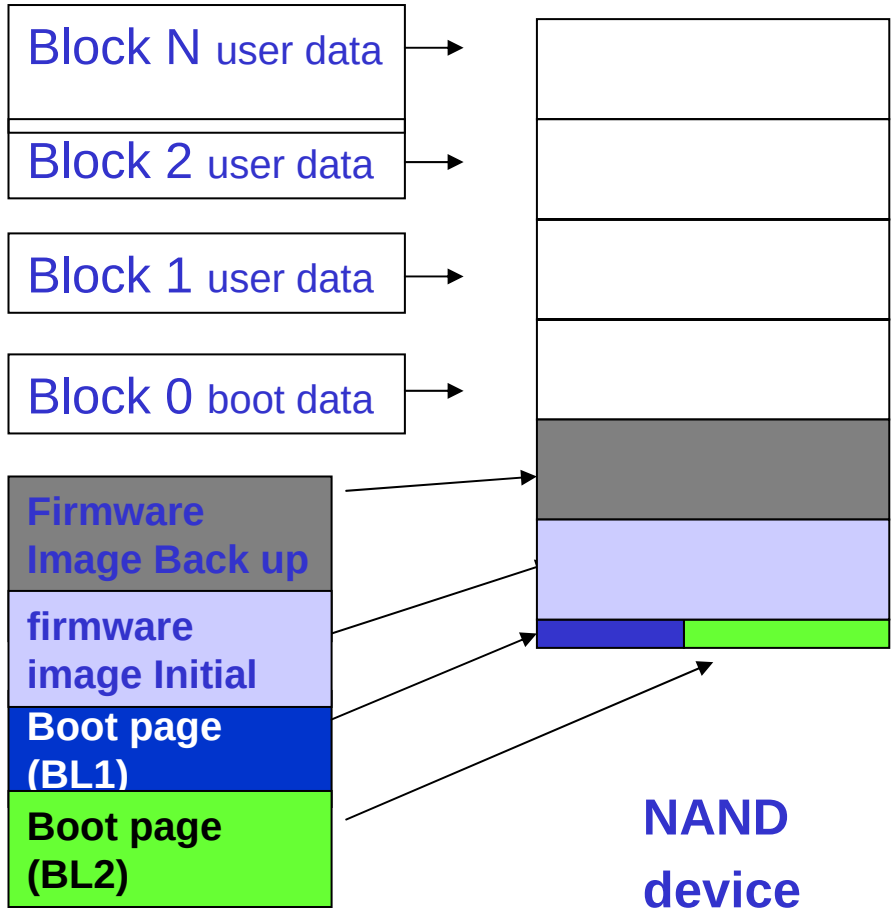
Typical System Architecture

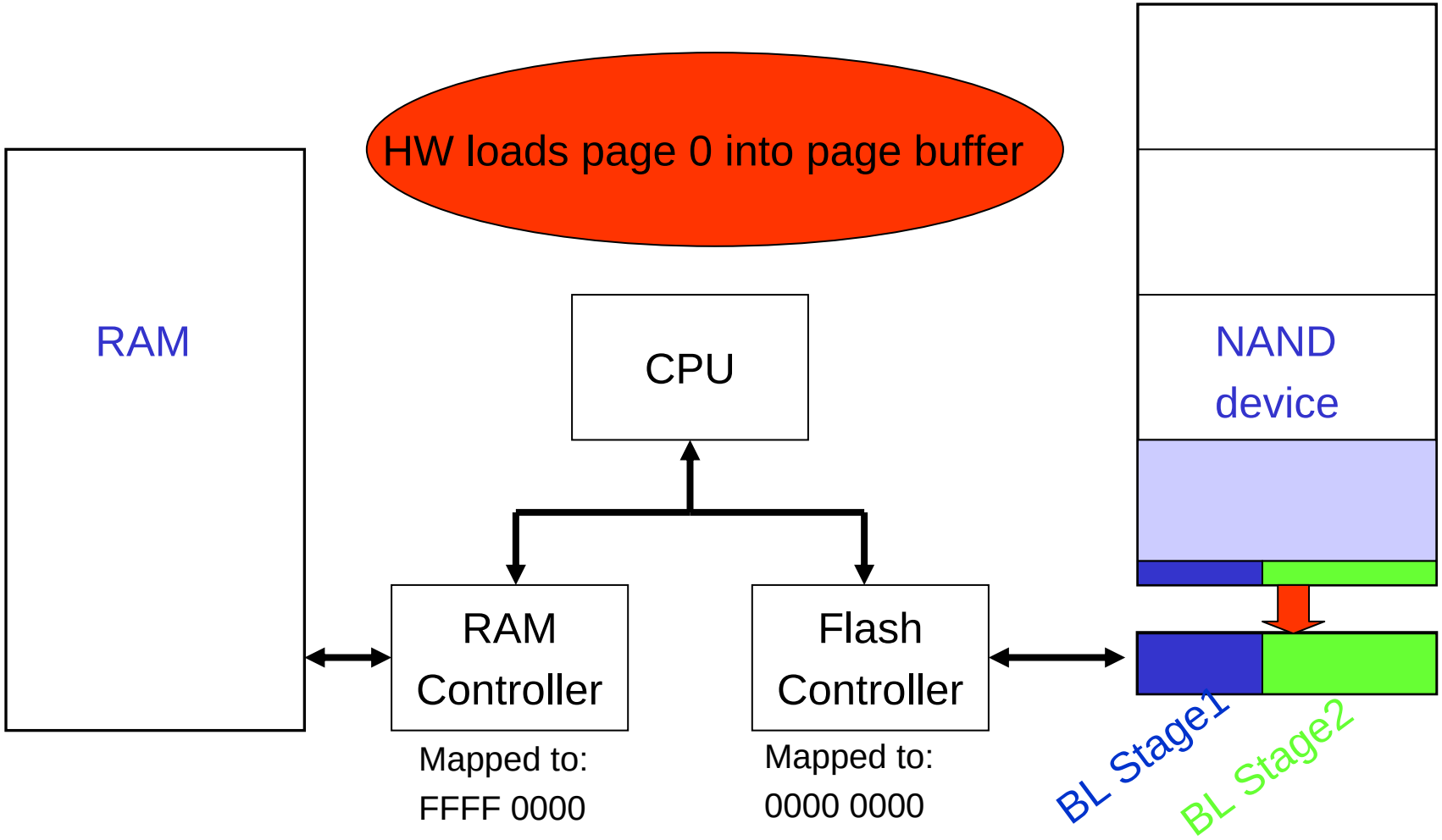


Contents of NAND flash

- Boot from NAND is a typically multi stage.
- Depending on supplier Boot Block (0) might not be guaranteed good.
- Multi Images should be considered.
- Communications to the file system and controller for image updates should be used.
- ECC correction can have a huge effect on how your system boots.



At Reset



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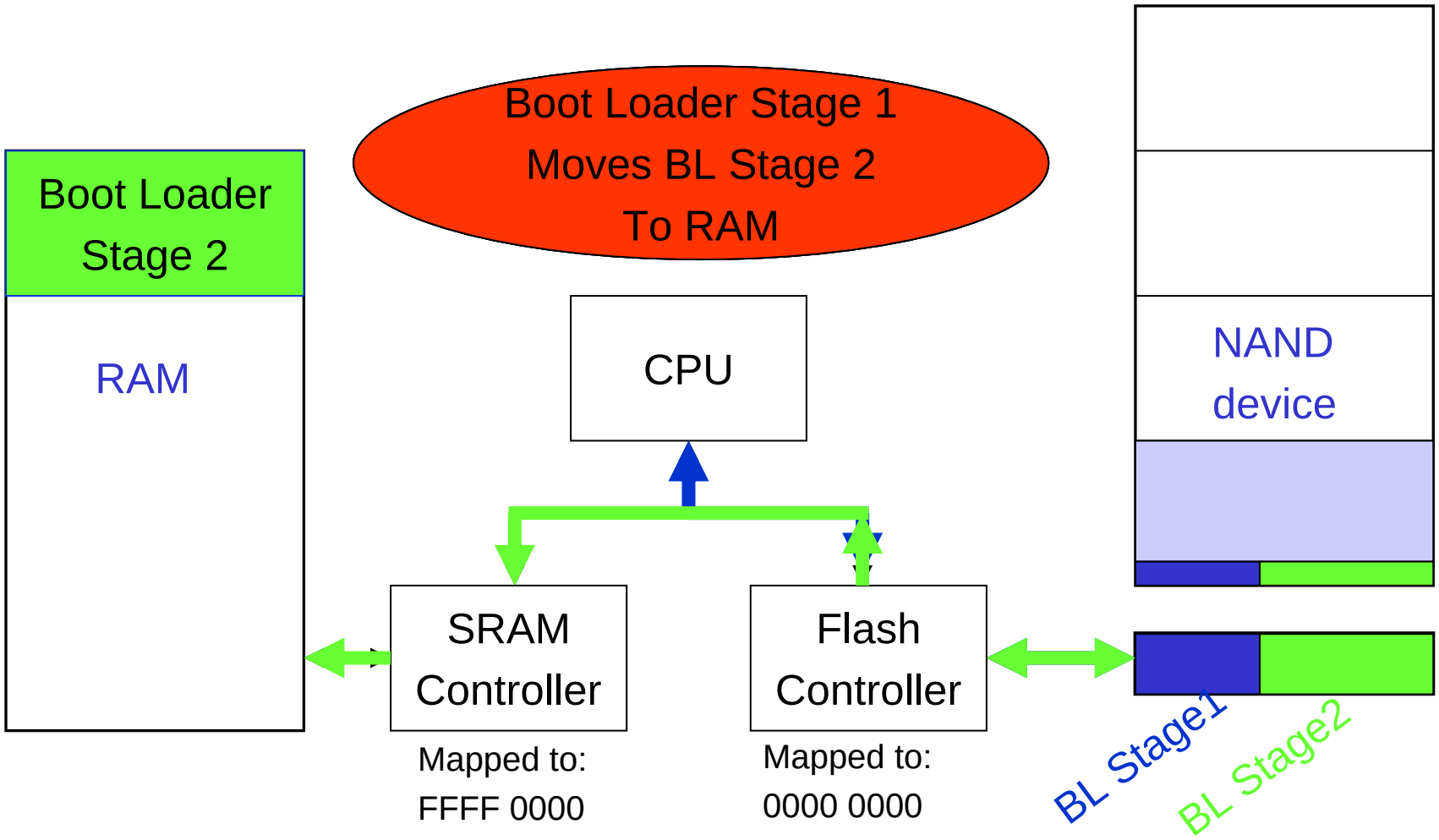
Boot Loader Stage 1



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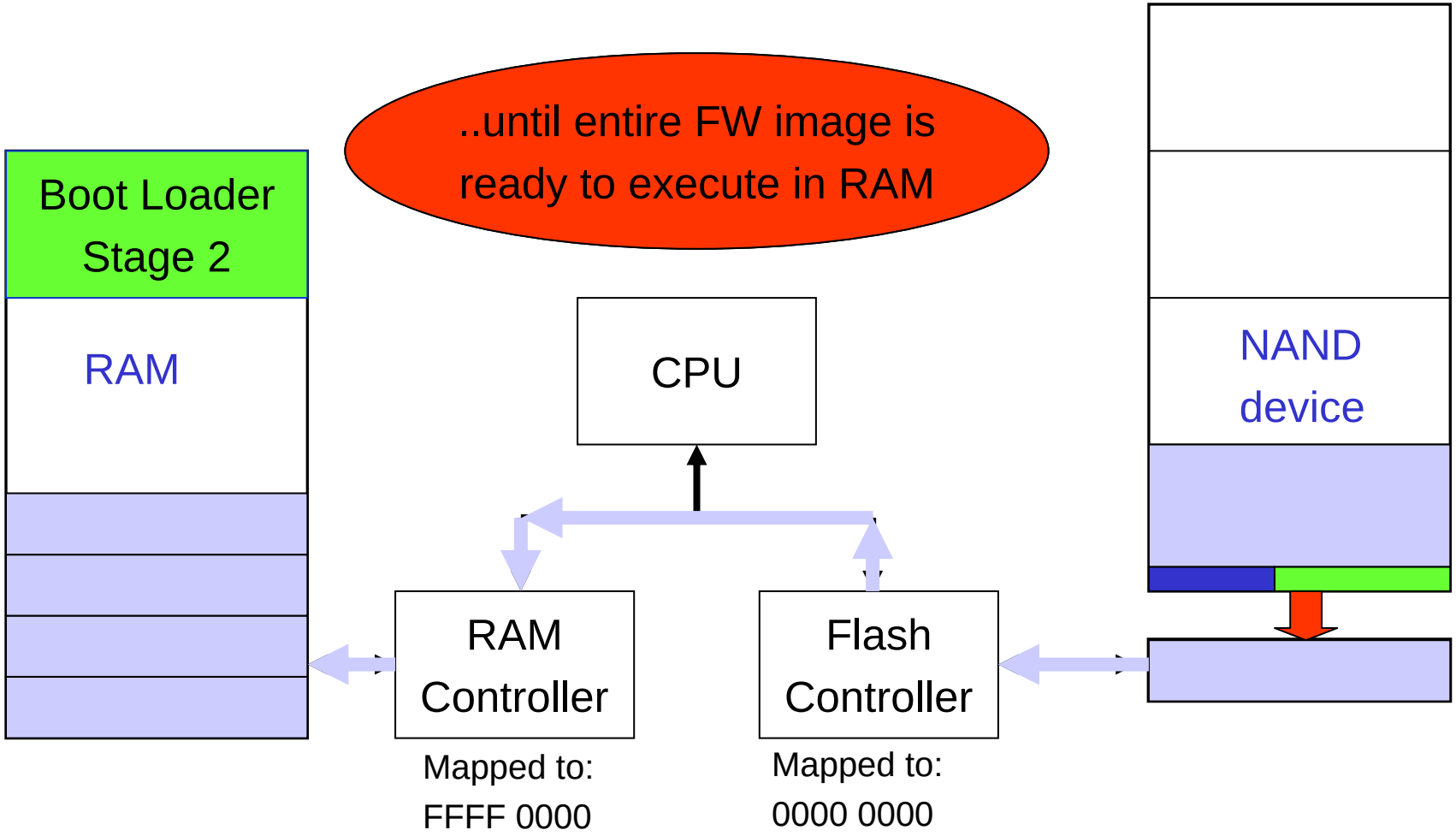
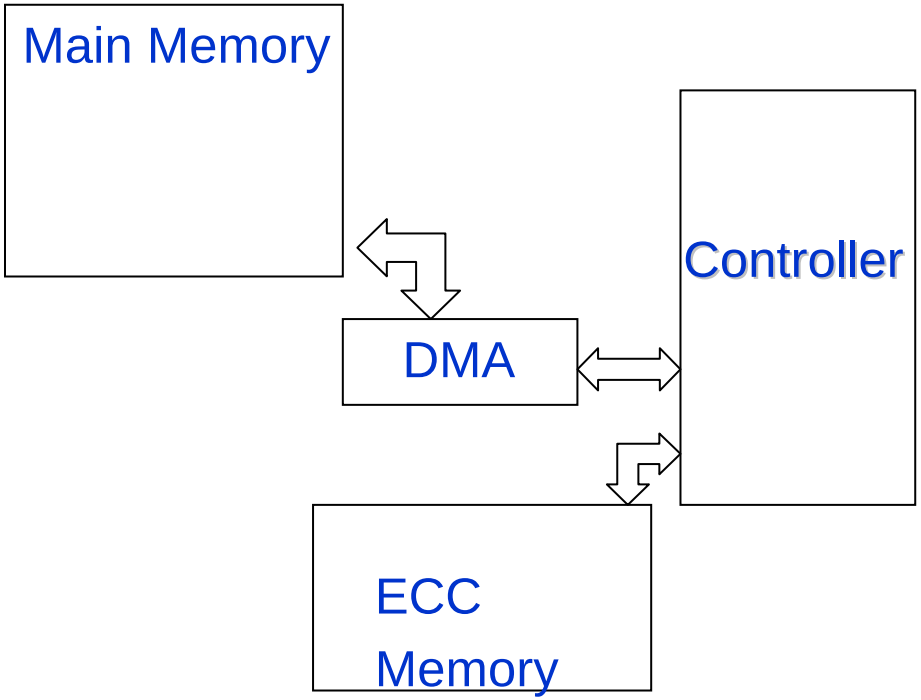
Boot Loader Stage 2



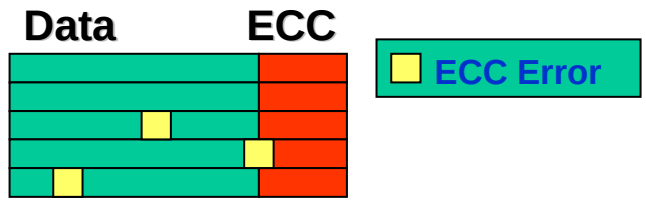
Effects of ECC for NAND Boot



Process for Errors

1) Transfer 2k page 20us
2) Syndrome Calc 104 cycles
3) BCH Code 60 cycles
4) Error finder 8164 cycles

Denali has at Speed Detect and Correct ECC for BCH



- BCH algorithm requires more time to detect errors
- This can require additional Memory.
- Increases code transfer time
- Increases Boot loader complexity.
- Possible additional stage required in Boot loader.
- Accessibility of Data in Main Memory

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Conclusion

- ***Architecture of the Flash controller and software has a huge impact of system components***
  - ***Processor selection, Memory space, Boot performance, Number of Boot stages.***
- ***Geometrical Shrinks of Flash will require even more technology to overcome operational issues.***
  - ***ECC***
  - ***Caching***
  - ***Data, Error logging***
  - ***Boot operation is not trivial, a system solution is required***
- **Denali's System solution provides**
  - ***Small code footprint with excellent NAND operational control.***
  - ***Enhanced Instruction set to reduce processor overhead.***
  - ***Enhanced ECC options for Multi Level Bit Cell devices.***
  - ***Booting from any NAND***