Memory Management: So Complex it's Easy

Amir Fridman

Director, Marketing Strategy, MHV division

SanDisk

amir.fridman@SanDisk.com

Santa Clara, CA USA
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Agenda

- NAND Flash Market Overview
- NAND technology challenges
- What is expected in next generation?
- How to bridge the GAP?
- Summary

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NAND flash market overview

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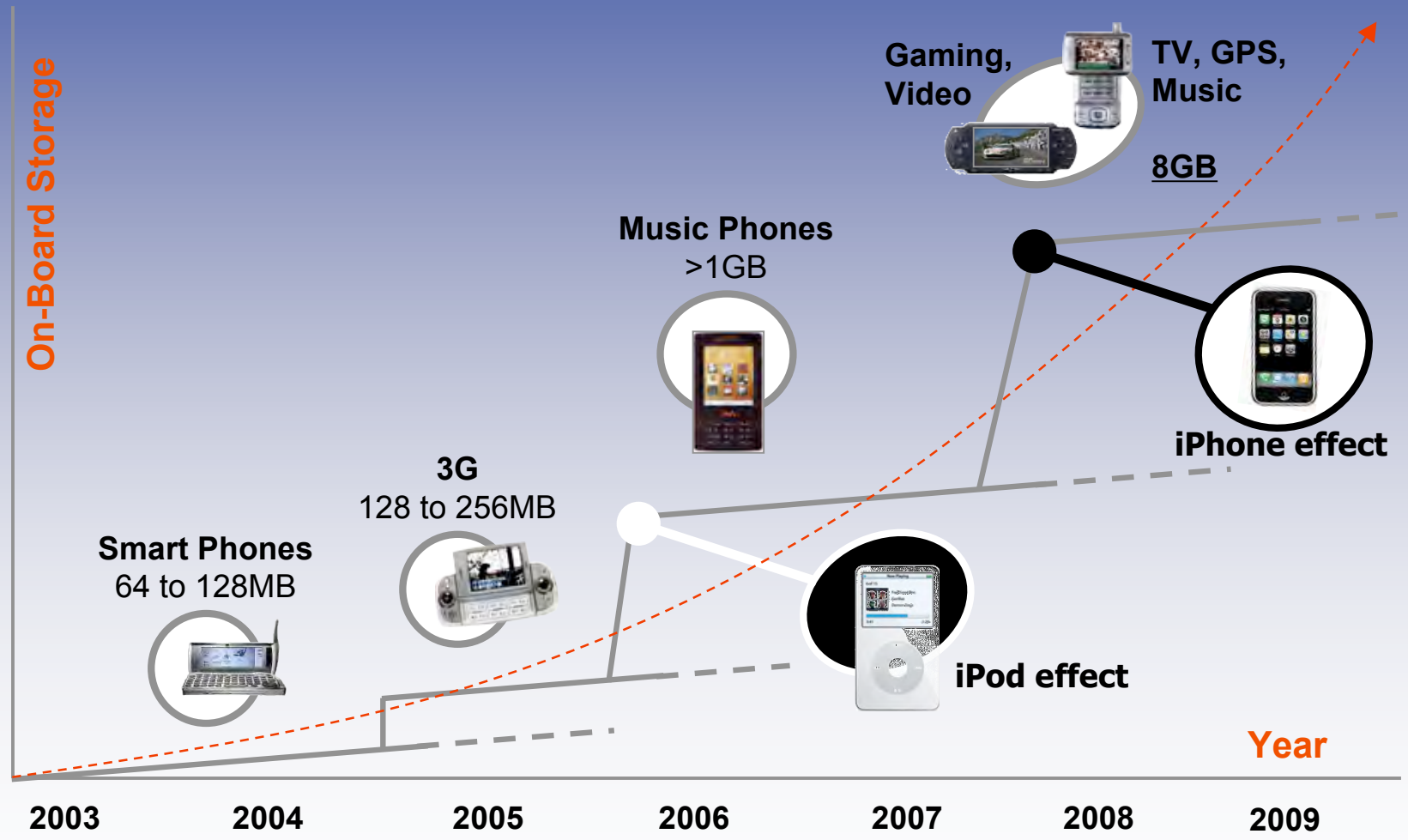
Mobile and CE storage is increasing by leaps



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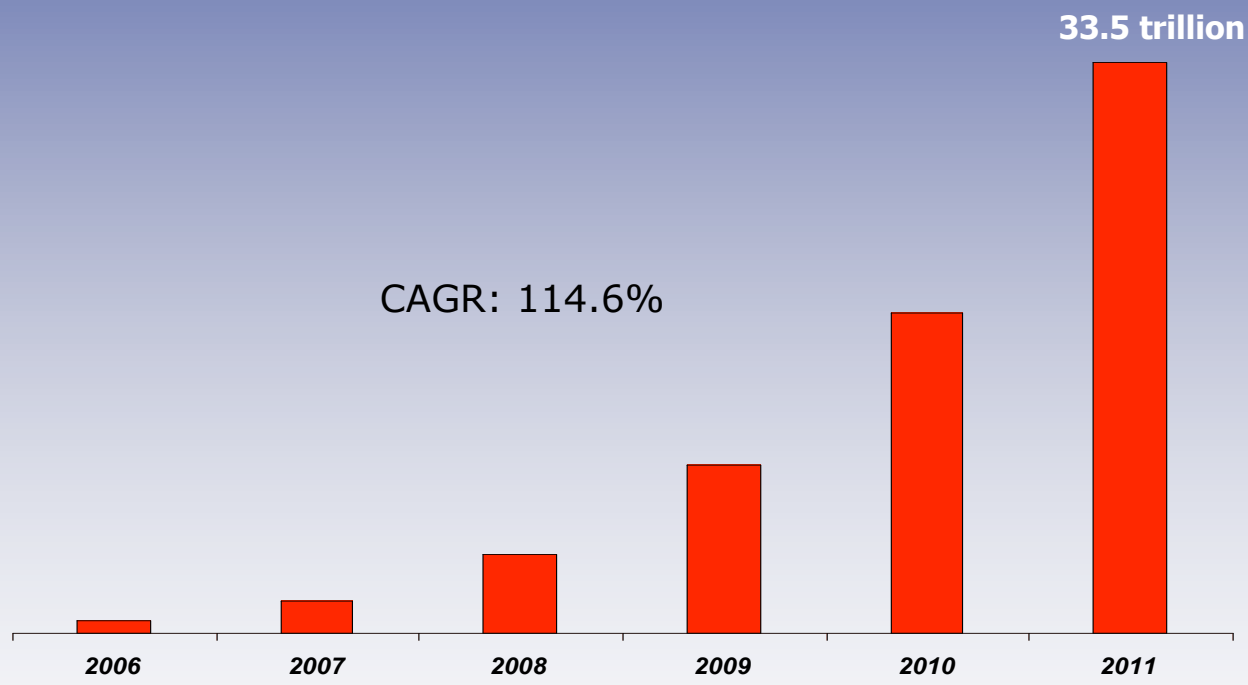
Explosion in NAND based devices

Worldwide NAND Flash Shipments, 2006-2011

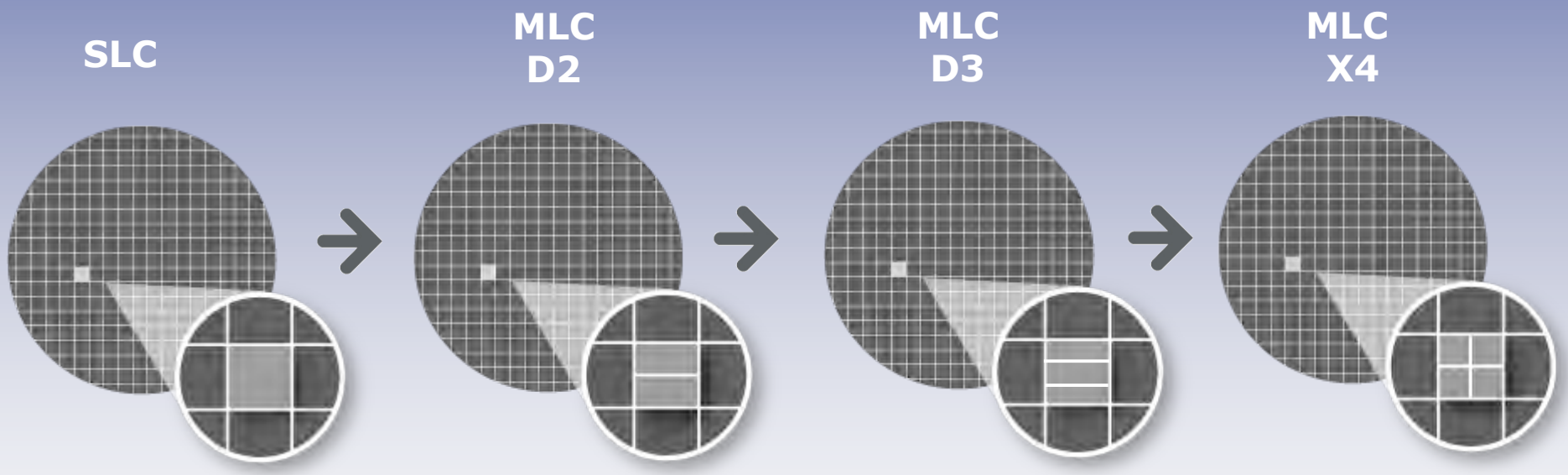
(Millions of Megabytes)



Source – Gartner, Inc., Memory, Worldwide, 2006-2011 (2Q07 Update)
By Richard Gordon, Andrew Norwood, Joseph Unsworth and Clare Hirst

Flash Memory SUMMIT

Moving to advanced technology Enabling high-capacity



X4 technology - enables 4 bits per cell
Higher capacity at lower cost

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NAND technology challenges

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MLC NAND challenges

- MLC NAND industry is characterized by:
  - Incompatibility between vendors
  - Incompatibility between generations
- MLC Flash optimizes cost, but compromises systems' performance and reliability
- Different applications require different performance and reliability of storage

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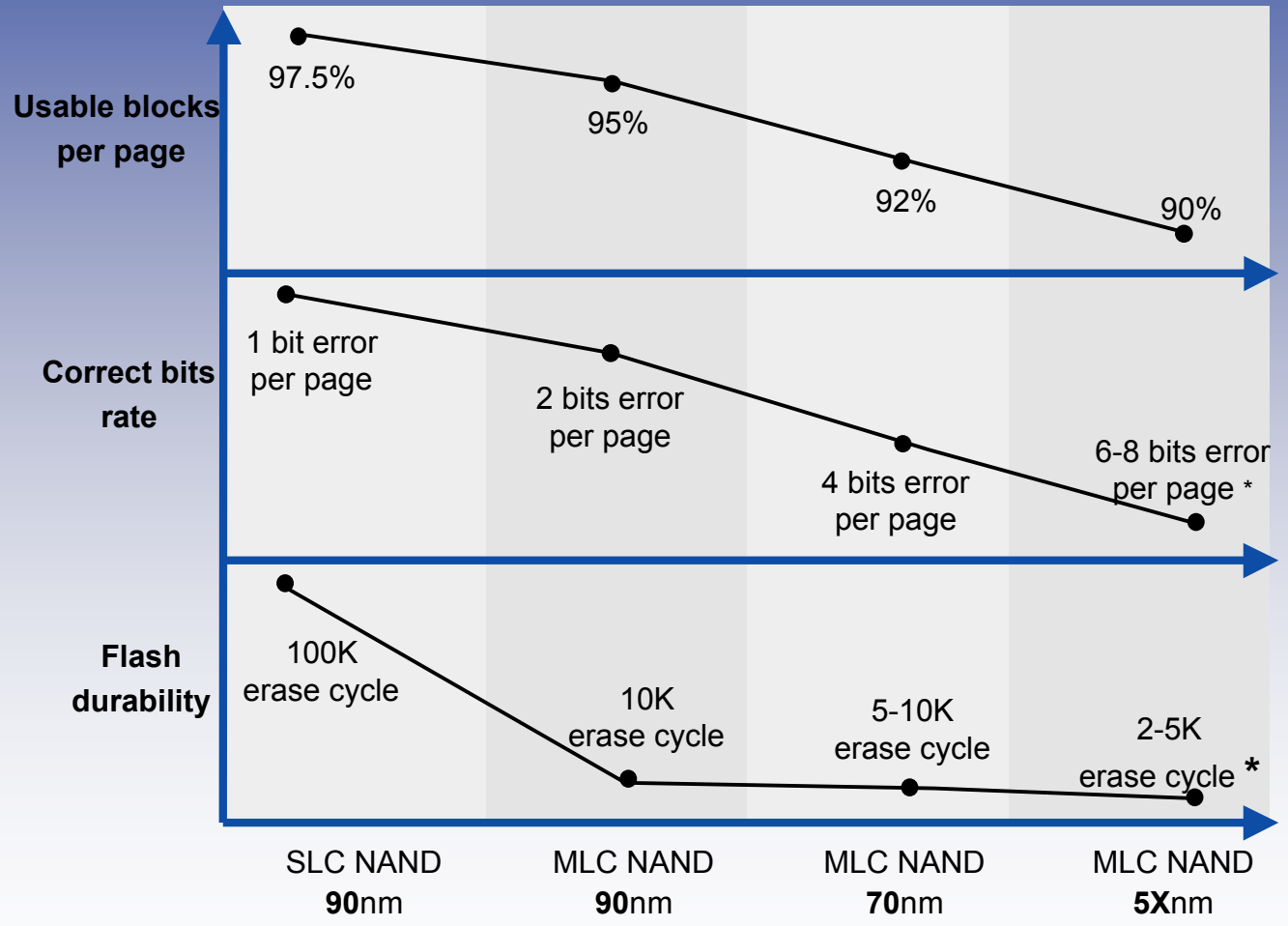
NAND reliability parameters



* Estimations

MLC NAND challenging technology

- NAND is currently the most dense FLASH technology – though it takes its toll by having to deal with:
  - **Bad Block**
  - **Endurance**
  - **Bit Errors**
  - **Data retention**
  - **Bit pairing & Power failures**

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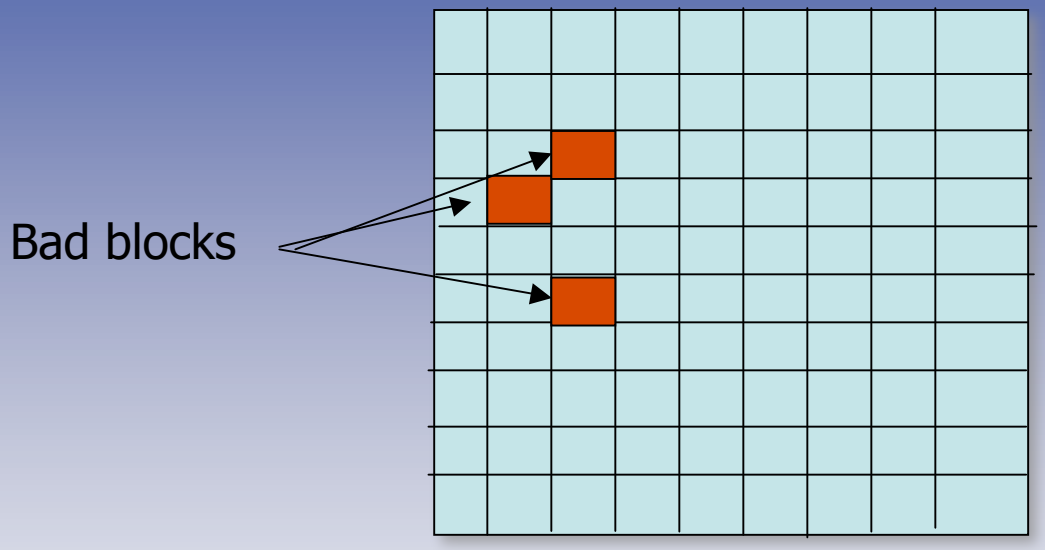
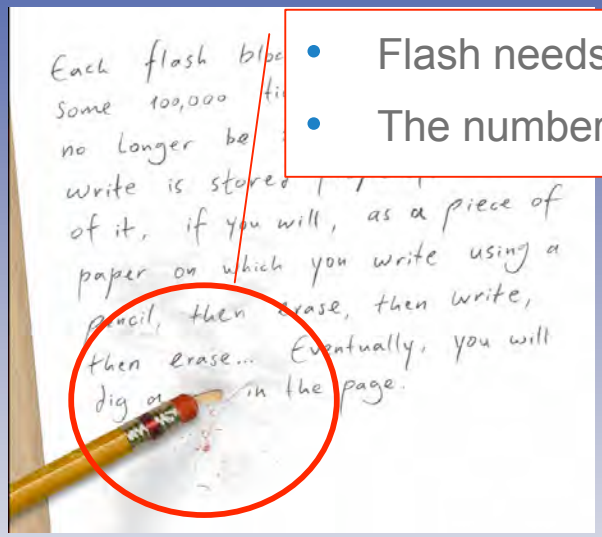
Bad blocks



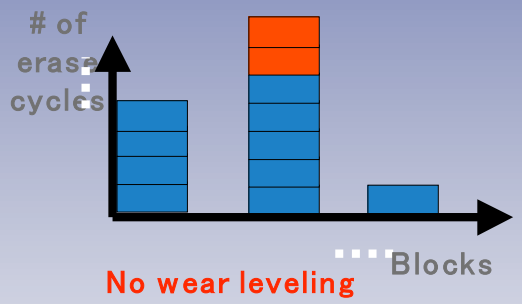
- **2 types of bad blocks:**
  - **Initial BB: devices from fabs are produced including bad blocks**
  - **Dynamic BB: new bad blocks generated during device life**

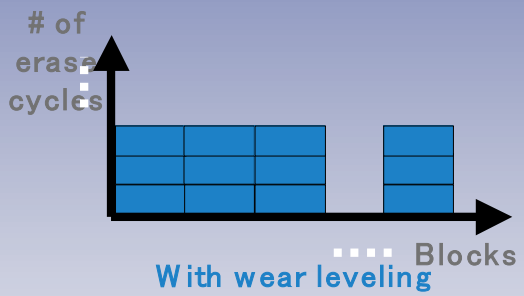
Advanced flash management SW technology detect and isolates initial and dynamic bad blocks

Limited Write / Erase Cycle & Wear Leveling



- Flash needs to be erased before it can be written to
- The number of Write / Erase is limited





Advanced flash management technology provides dynamic and static wear leveling:

- ***Dynamic wear leveling: updated files***
- ***Static wear leveling: updated and static files***

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Bit Errors

- **Basic issues**
  - Read disturb – Many reads causes some of the cells to be programmed deeper (change logical states)
  - Program disturb – The content of the cell is changed due to programming of neighbor cells
  - Data Retention - The charge in the cells leaks causing change of logical state
- **Requirements**
  - **SLC -** single bit ECC shifting to 2 bits
  - **MLC -** 4 bits ECC shifting to 6-8 bits in 50nm and higher in 4Xnm

EDC/ECC beyond current flash needs enables faster migration to future technologies

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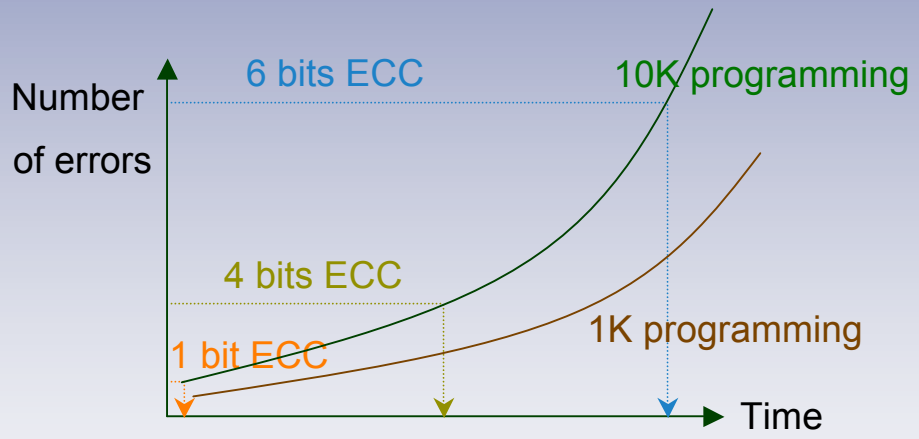
Data retention, endurance & EDC/ECC

- **Data retention** defines how long the data programmed remains valid
- **Endurance** defines how many times data can be programmed
- There is a clear correlation between those 2 parameters:

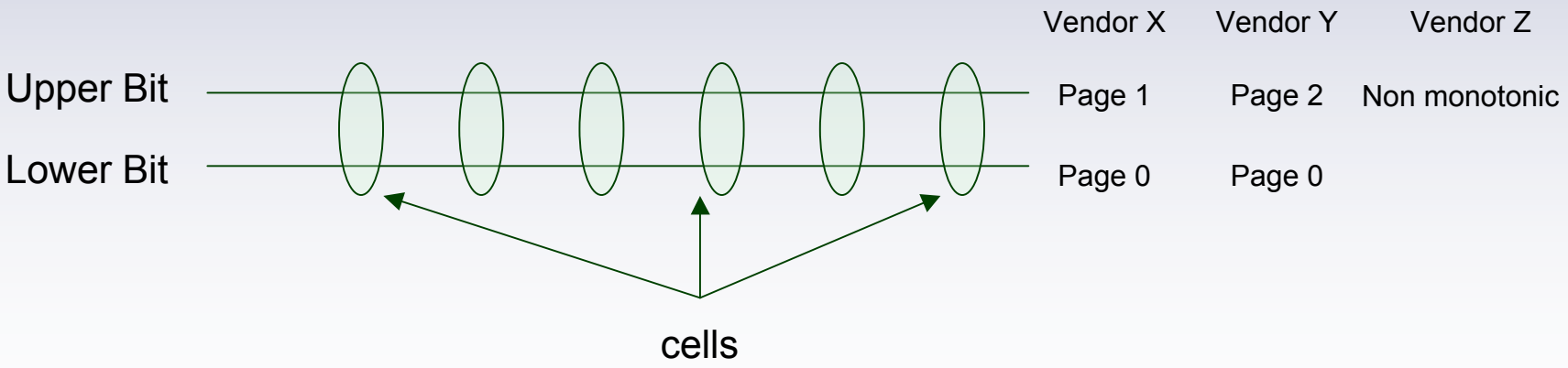


- Data retention:
  number or errors increases with time
- Endurance:
  number or errors also increases with number of programming
- Stronger ECC corrects more errors, improves endurance and data retention

Stronger EDC/ECC beyond required in specifications, can increases device endurance & life span

Bit pairing

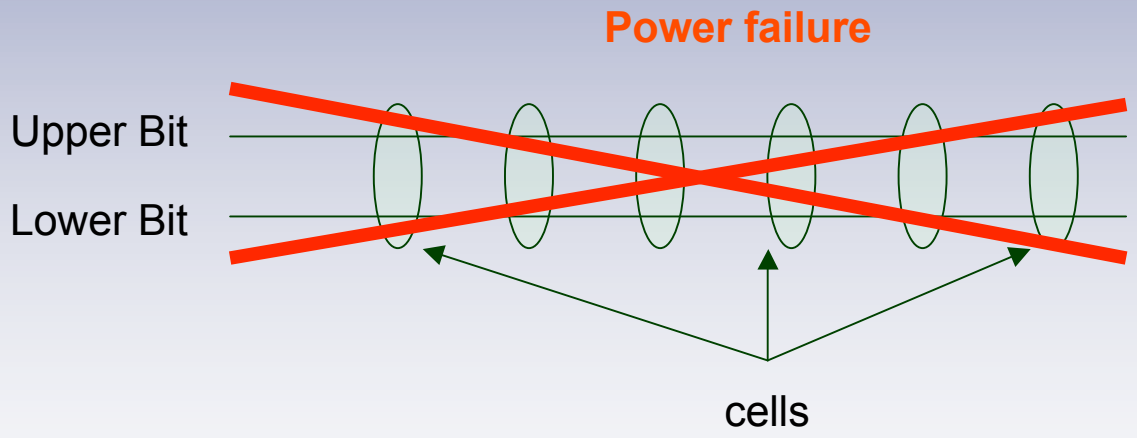
- In MLC product each cell includes 2 bits
- However in most cases each bit belongs to different logical page
  - The arrangement is different from vendor to vendor
  - The arrangement is different from generation to generation
  - The arrangement is usually not documented in data sheets
  - The knowledge of logical to physical is a must in order to handle power failure correctly



Bit pairing impact on power failure

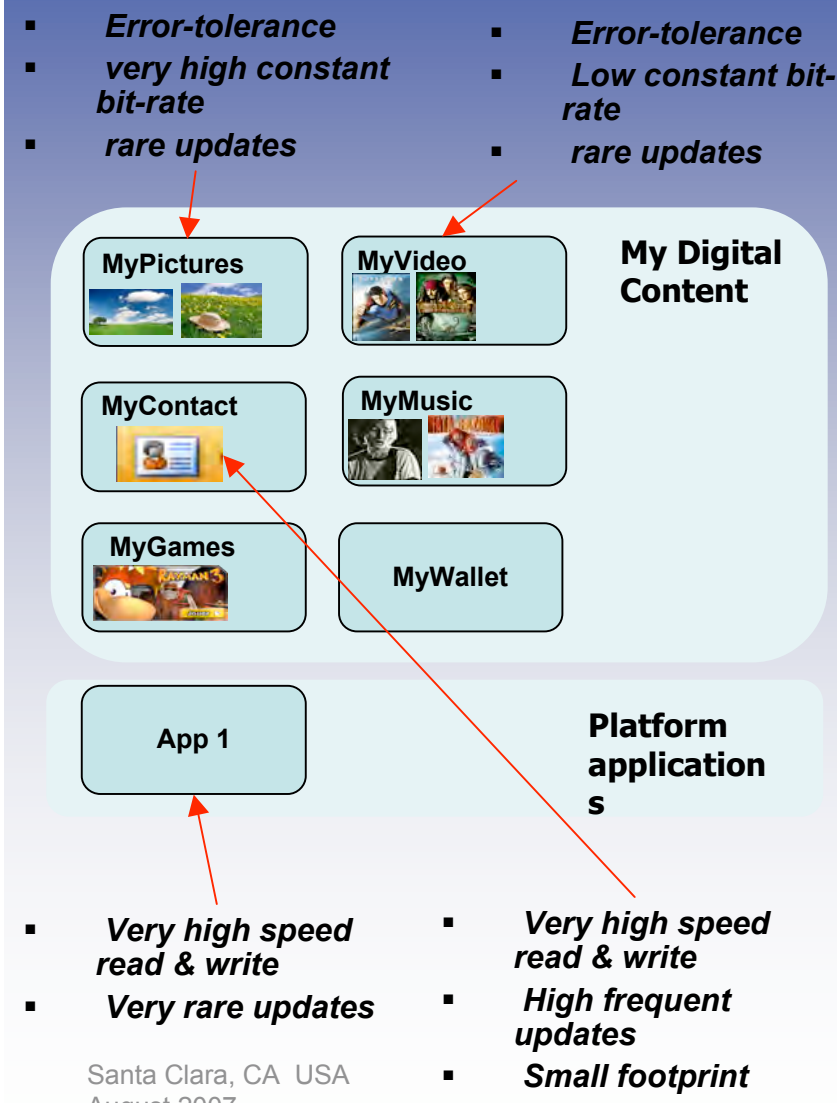
Consider the following case

- Lower page was written
- Later (1 day after for example) – upper page is written
- During upper page program – power failure occurs
- Impact: **Data in lower page, considered safe, is lost.**



Advanced flash management technology has optimized power failure protection, including bit pairing

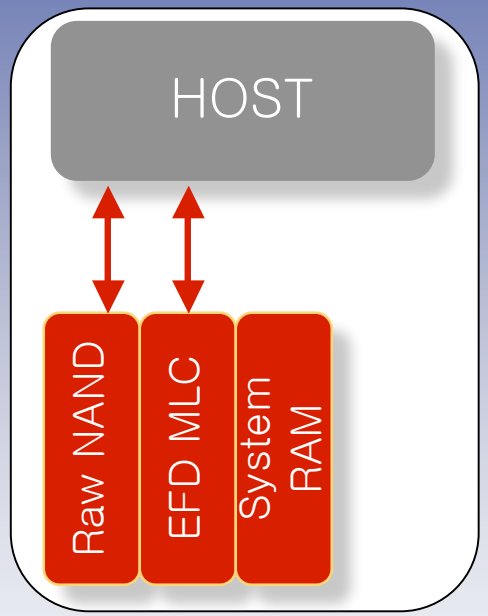
Different Applications = Different requirements



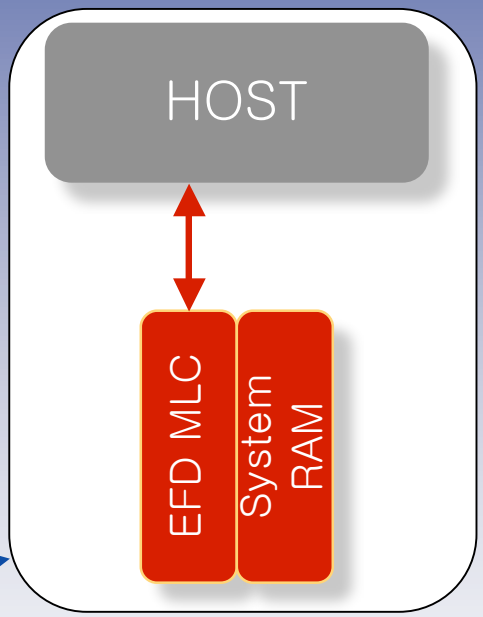
- Content types & applications are treated equally with today's storage technology, regardless of their intrinsic requirements
  - Performance
  - Reliability
  - Security
- Traditional design is challenged with the worst-case of all applications' requirements in terms of performances, data retention, endurance etc..

Booting from MLC Flash Disk

How fast can the market move from this?

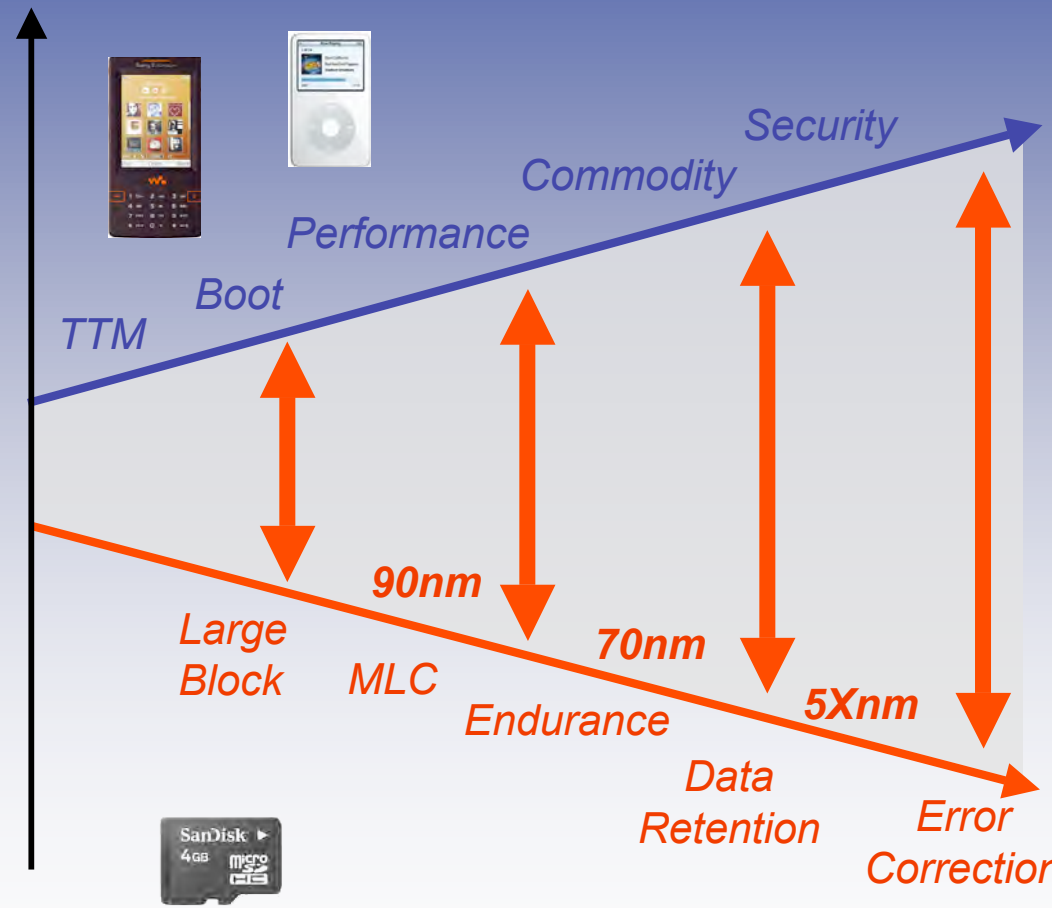


To this!!!



- Reduced $
- Reduced space
- Reduced design complexity
- Reduced height

Flash Storage Conflicting Trends



Market Expectations going UP

NAND management Is challenging!

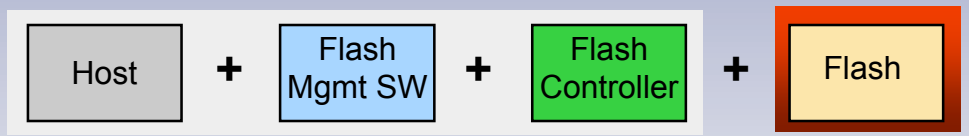
NAND Usability going DOWN

Embedded Flash Drive (EFD) Evolution

Generic Flash Drive Ingredients:

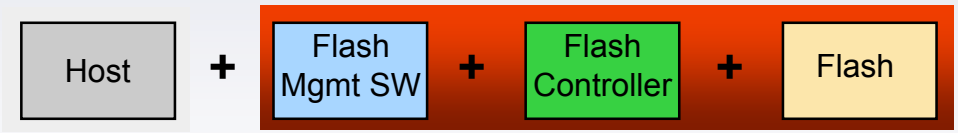
Legacy Solutions – Flash Management on Host

Example: Raw SLC NAND:



Embedded Flash Drive – Flash Management on Drive

Solving software complexity issues



Embedded Flash Drive (EFD)

- Flash manufacturers target is to move to new process & MLC based technologies as fast as possible!
- Embedded Flash Drive with advanced flash management technology solves
  - NAND reliability limitations
  - Power failure protection
  - Fast migration to MLC latest process

EFD enables advanced MLC technology usage for boot and storage

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Summary

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Summary

- NAND flash is the fastest growing memory segment
- Mobile and CE markets leads the flash consumption growth
- NAND market migrating from SLC to MLC technology and future X4
- MLC optimizes cost, but compromises systems' performance and reliability
- Migration to advance NAND technology becomes more difficult and complex, hence puts in risk the introduction of new models
- Mobile handset manufacturers need to design flash storage solutions that overcome evolving NAND technology and challenges and support storage hungry applications

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Thank you

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