



The Evolving Role of Flash in Memory Subsystems

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Overview

- The NVM Market Segment Opportunity
- The Right Solution for the Right Need
- Key Trends – Wireless & Computing
- Future Trends – PCM





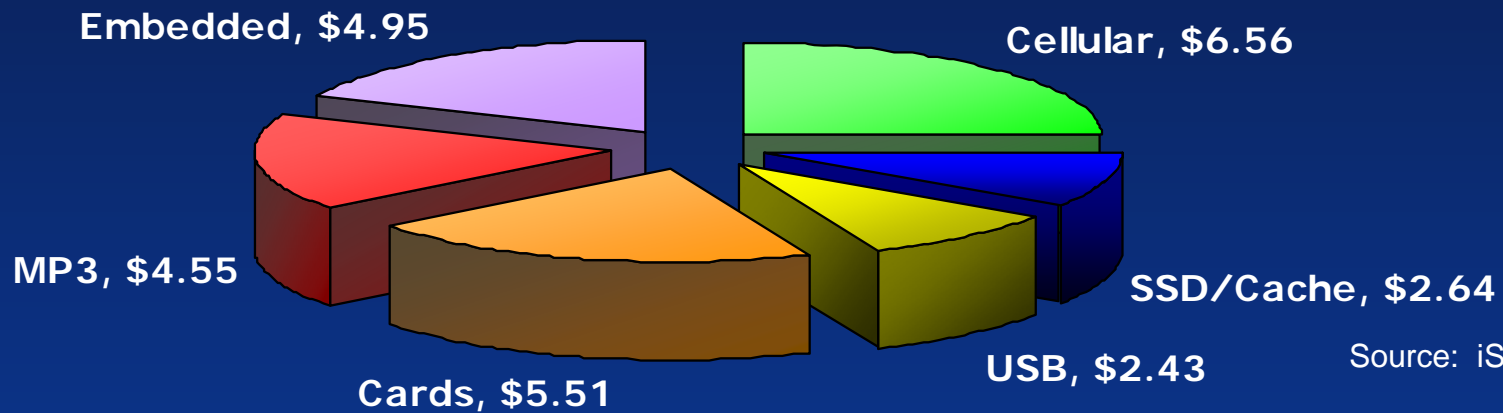
→ The NVM Market Segment Opportunity

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The NVM Market Segment

2009 Flash Market Segment Forecast: \$27.1B



Source: iSuppli 6/2007

NOR

- Continued strength in cellular & embedded

NAND

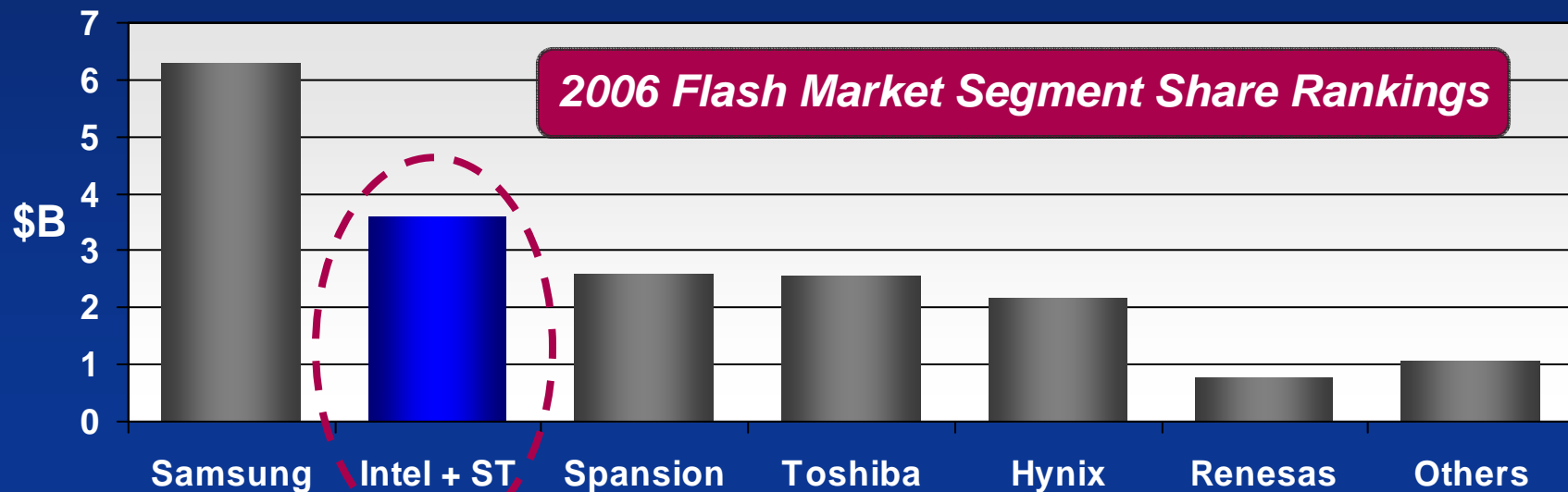
- Computing is major growth opportunity



The Potential New Flash Landscape

May 22nd, 2007: Francisco Partners, Intel and ST announce the formation of the new global company focused on memory solutions

2006 revenue base of ~\$3.6B – World's Largest Pure Play NVM Solutions Supplier





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The Right Solution for the Right Need

Data Storage Spectrum



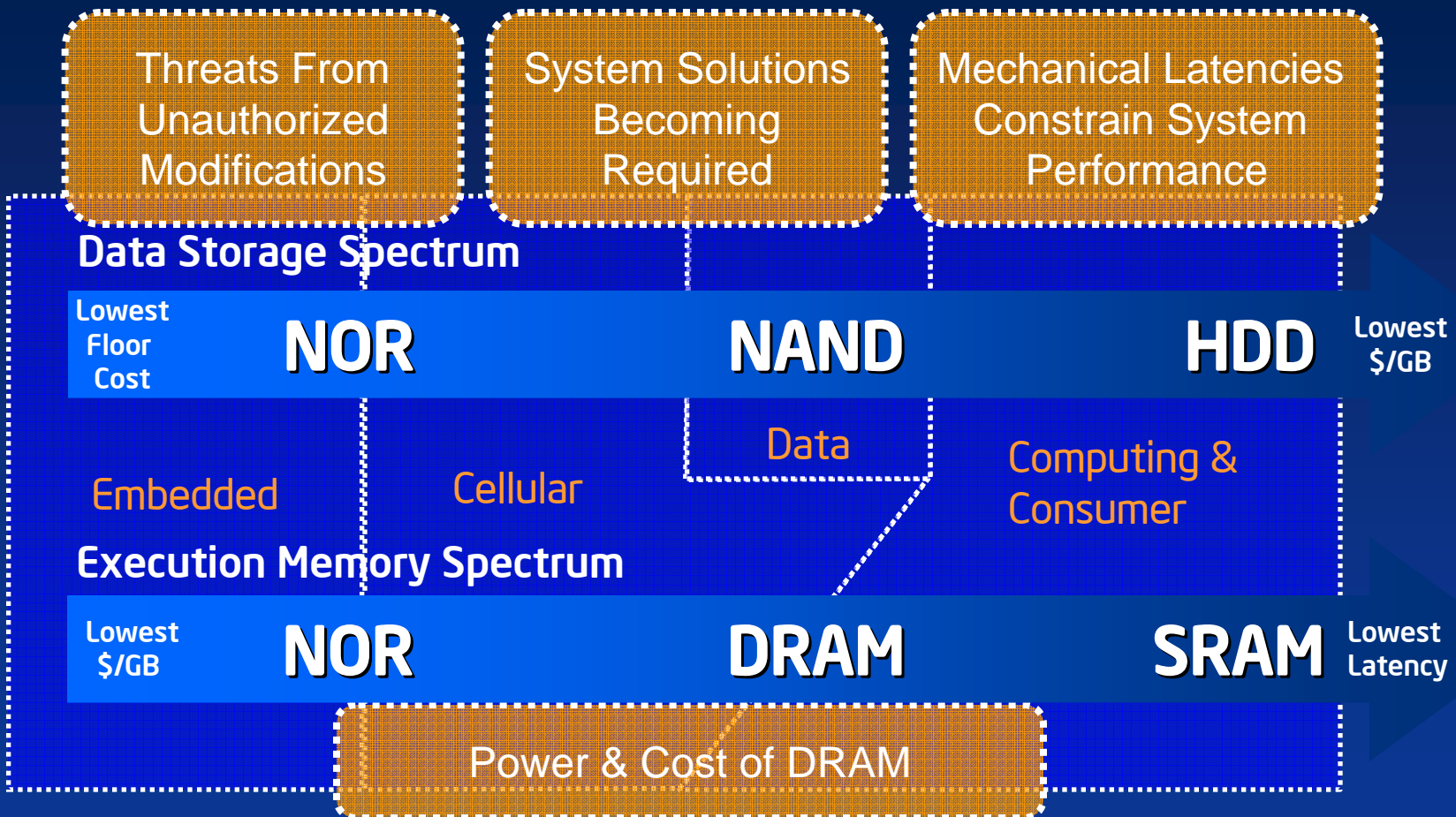
Execution Memory Spectrum



Selection Criteria is Straightforward



Potential Issues in the Memory Spectrum



Key Issues Must be Addressed

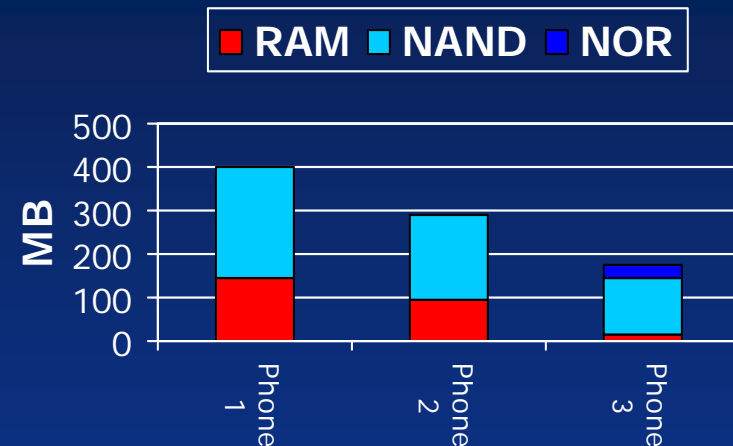
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“Growing” Problem with RAM in Mobile Handsets

- RAM technology trending behind flash
 - Cost, density, litho not keeping pace
- Mobile RAM usage demands increasing
- Apps & data add user value
- Power & cost of Mobile RAM aren't keeping pace

Solution Is Required

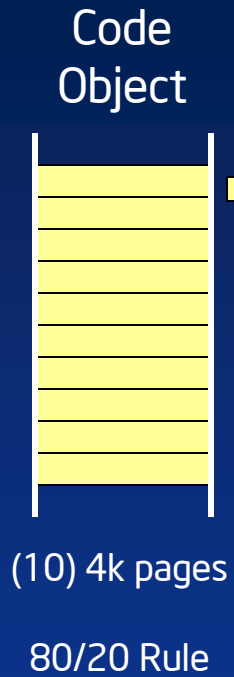
Example Memory Content*



Type	CDMA2K	UMTS	GSM EDGE
Standby	270 hrs	264 hrs	348 hrs
Battery	870mA	1200mA	860mA
Screen	432x240	320x240	240x320
Colors	256K	65K	16.7M
MP3	Yes	Yes	Yes
Camera	3mpxl	1.3mpxl	2mpxl
Data	1X EVDO	HSDPA	EDGE

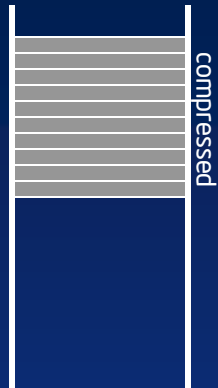
*Source: Portelligent, 2007 Teardowns

Handset Memory Architectures

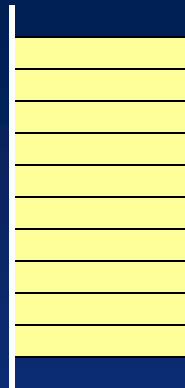


Utilization:

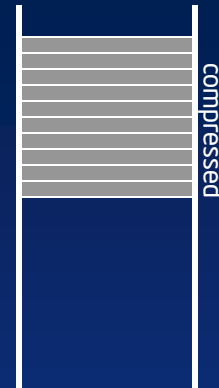
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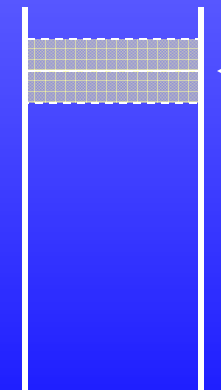
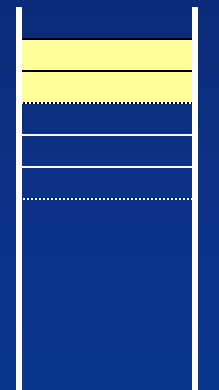
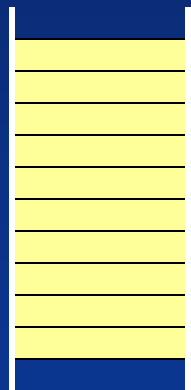
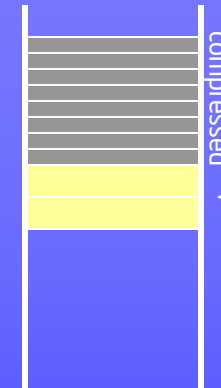
XiP



Demand Paged



New: Blended



Flash

Mobile RAM

5 Flash
10 RAM
15 Total

10 Flash
0 RAM
10 Total

5 Flash
2 RAM
7 Total

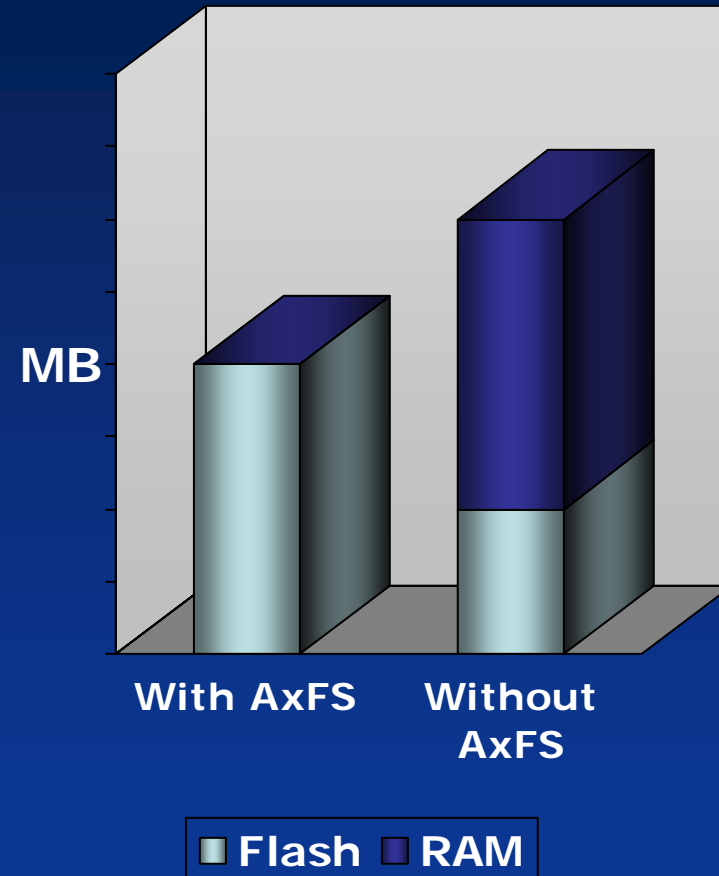
6 Flash
0 RAM
6 Total



XiP & Blended Offer Best RAM Savings

Blended Example: Memory Footprint Reduction Using AxFS

- Linux Based System
- Example: Highly used system library, libsoo.so is 2MB
- Compressed Paged (squashfs):
 - 1 MB of flash + 2 MB of RAM = 3 MB
- Improved With Advanced XIP File System (AxFS):
 - 2 MB of flash + 0 MB of RAM = 2 MB



Reducing the Power & BOM Impacts of RAM

Initial Latency	Read Bandwidth	Pipelining	Write Bandwidth	Erase Latency	RAM contents	
moderate	low	low	low	low	Code	→ Today: M18 / AXFS
moderate /high	moderate /high	moderate	moderate	low	Read-Only Data	→ Next: LPDDR / AXFS+ + Pipelining + Higher Read BW
high	high	high	high	high	Read-Write Data	→ Future: PCM / Next Gen SW + Lower Initial Latency + Higher Write BW + Zero Erase Latency
unknown	unknown	unknown	unknown	unknown	Static Allocations	

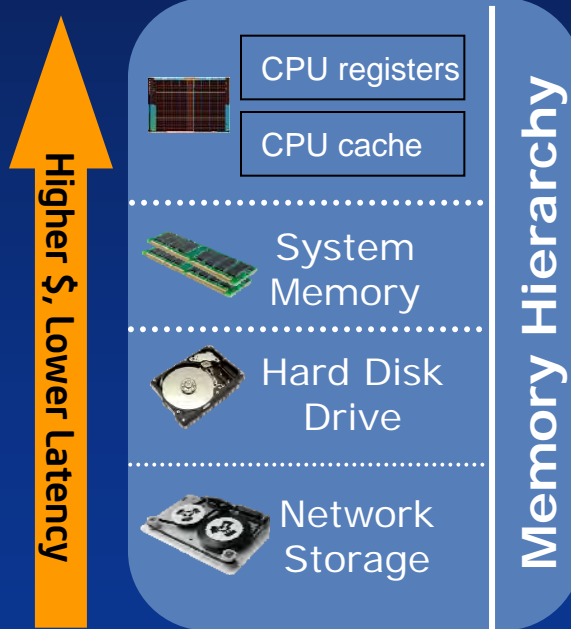


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Memory Hierarchy Evolving in Computing Platforms

Traditional Hierarchy

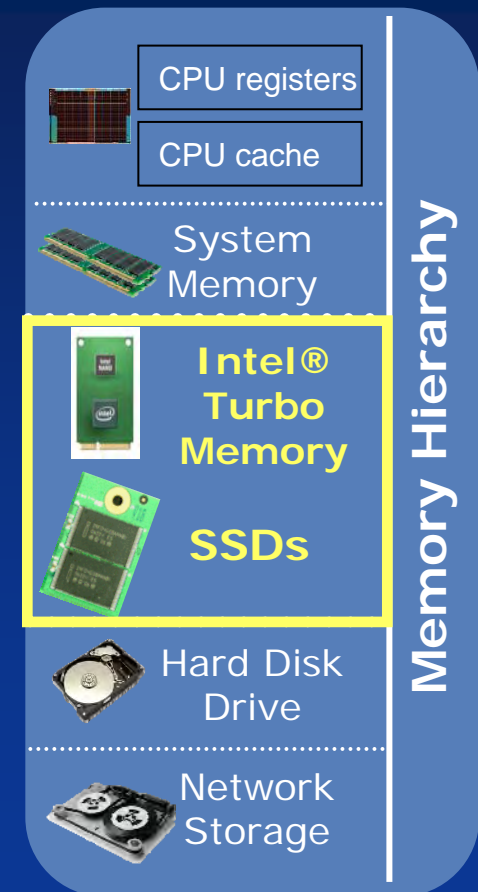


Key Issues

Cost vs. NAND
Power

Latency Plateau
Cost per IOPS

New Hierarchy



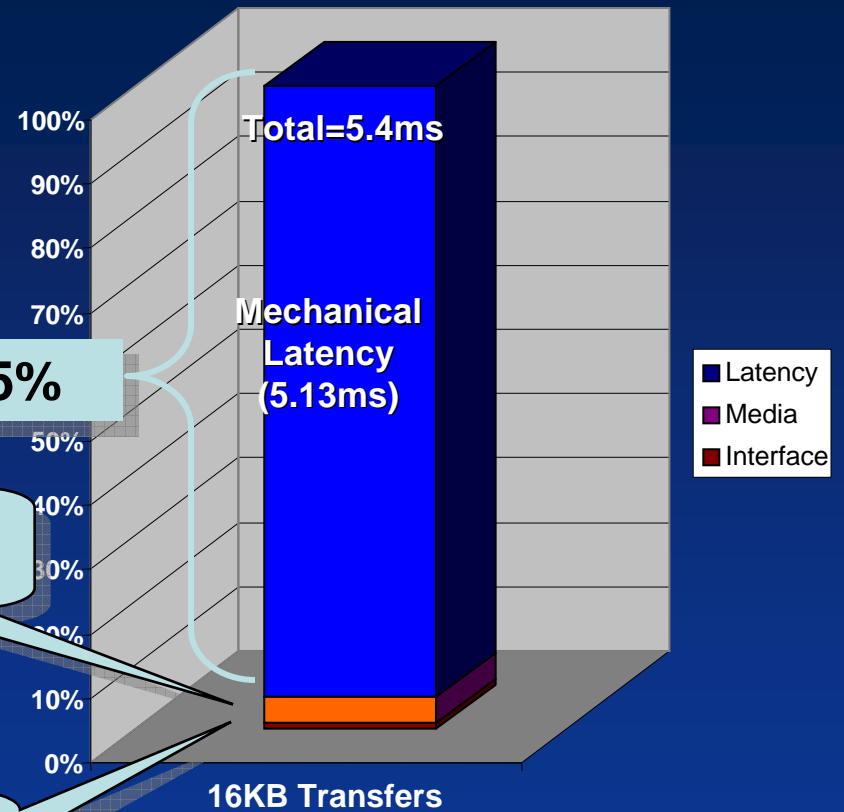
**New NVM Solutions
Address Key Issues**

Typical Disk Transfers Dominated by Latency

Transfer time accounts for insignificant fraction of actual disk service times

Total Value SSD (USB)
Latency = 690us
7.8X improvement
(vs. 5.4ms for HDD)

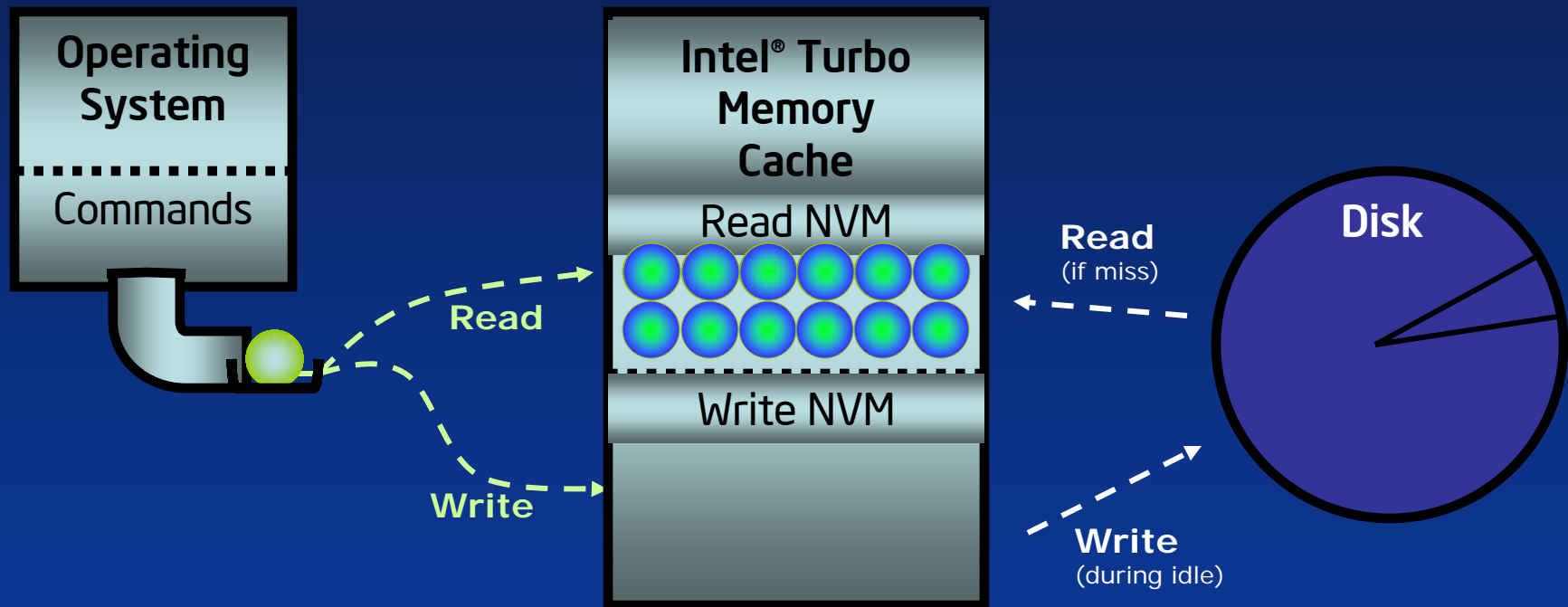
*IOPS performance breakdown for HDD running sample workload (75MB/s, 3Gbps)



Seek and Rotational Latency are What Matters for Typical Workloads

Intel® Turbo Memory – Performance and Battery Life Benefits

Intel® Turbo Memory supports read and write caching through Microsoft ReadyBoost* and ReadyDrive* technologies



Intel® Turbo Memory reduces disk access events, saving power and improving system performance up to 20%

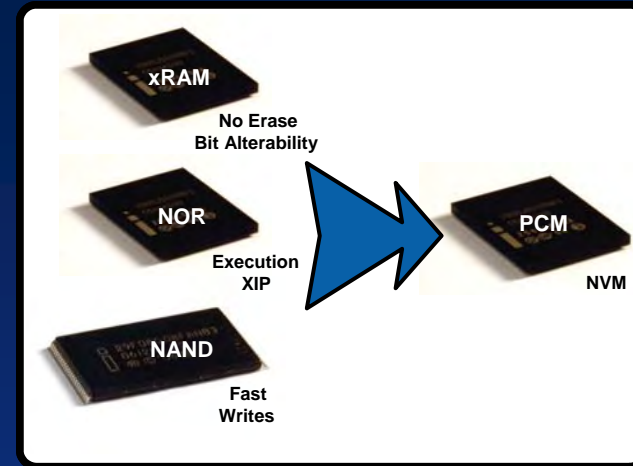


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Phase Change Memory (PCM)

- PCM combines best attributes of RAM, NOR & NAND
 - No Erase – Bit Alterable
 - Fast Writes
 - Execution in Place
 - Nonvolatile
- Excellent scaling path to the future



Attributes	PCM	NOR	NAND	DRAM
Non-Volatile	Yes	Yes	Yes	No
Bit-Alterable	Yes	No	No	Yes
Power	~Flash	~Flash	~Flash	Higher
Write/Erase	Medium → Fast	Medium Write	Medium	Fast
Read Speed	Fast	Fast	Slow	Fast
Error Rate*	Best	Good	Fair	Fair
Endurance	Flash < PCM < DRAM	~Flash	~Flash	Unlimited

PCM Capability Demonstration

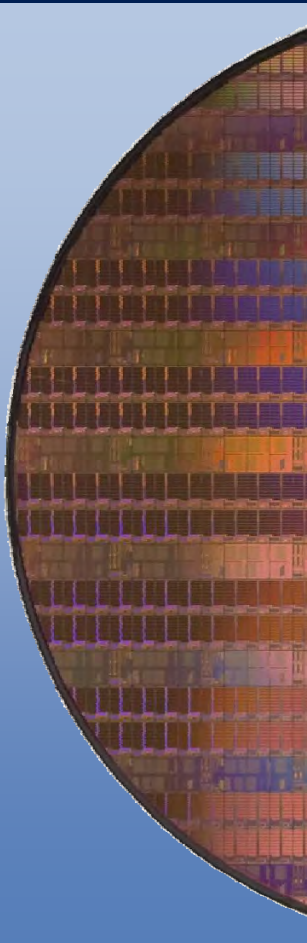
- R&D with ST in PCM since 2003
 - Intel working with Ovonyx Since '00
- 90 nm test results encouraging
 - Data matches early expectations
 - Yield & reliability learning ongoing on 128 Mb arrays
- Demo:
 - NOR and 90 nm PCM
 - Graphic display tracks status of chip re-write



Demo Available

Flash: Constantly Evolving

Technology Innovation



- Technology capability may force changes in future memory usage
- NOR flash offers a solution to the RAM issue in wireless
- NAND flash altering the storage *and* memory landscape in computing
- PCM offers new usages



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