Custom Design Automation

Steve Ferguson
Technical Director

steve.ferguson@pulsic.com

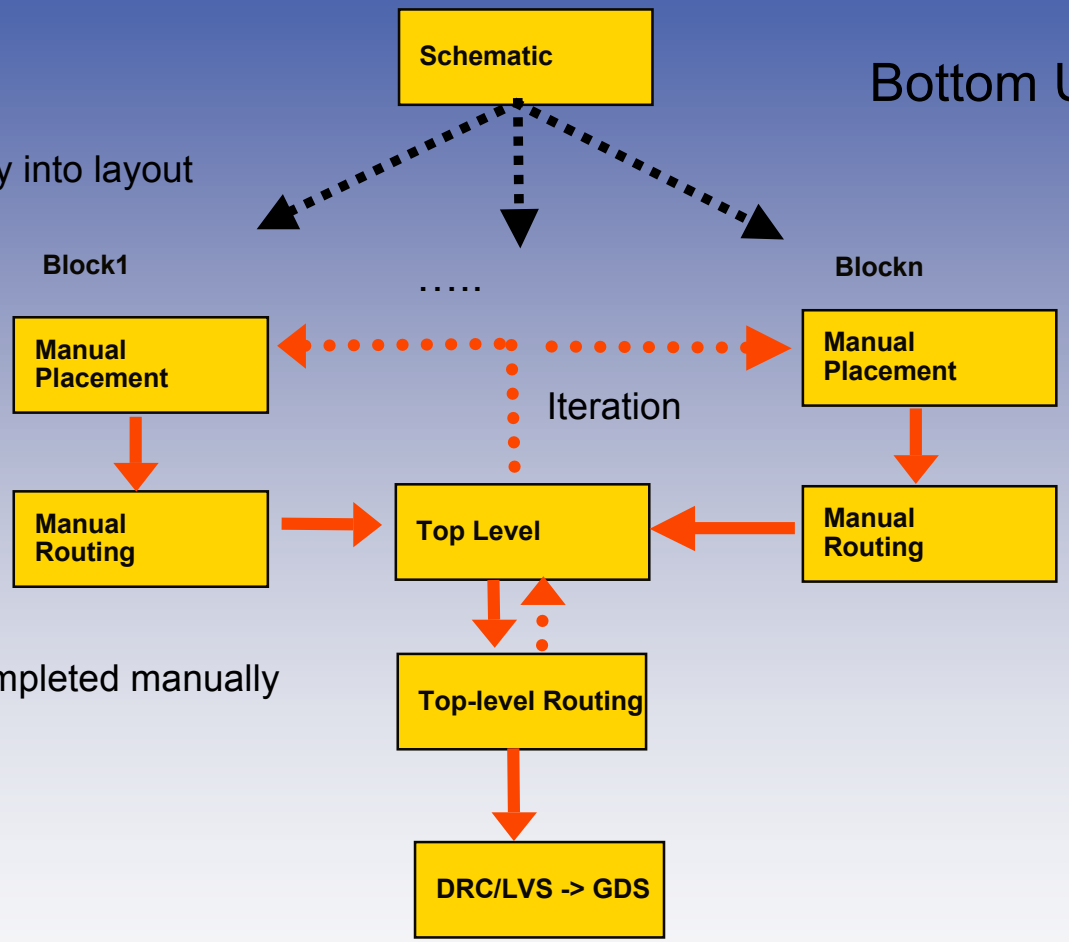
Characteristics of current FLASH designs

- **Pressure on design teams to increase capacity and performance of Flash devices is becoming more intense with each design iteration**
  - **More components placed on Flash devices with reduced size = larger die size and power issues**
  - **Arrays becoming larger as capacity requirements increase leaves less room for logic**
  - **Less real estate for control and peripheral logic means performance is compromised**
- **Not enough structured planning at beginning of design**
  - **Re-spin of previous design is considered enough 'to get started'**
- **Physical design tools are either not integrated or not used**
  - **Floorplan is often 'drawn' manually**
- **Consequently designs miss time, size and financial targets for both design and die costs**
- **How can these problems be circumvented and the risks be managed?**

FLASH Memory Physical Design - Existing Flows

Bottom Up Design

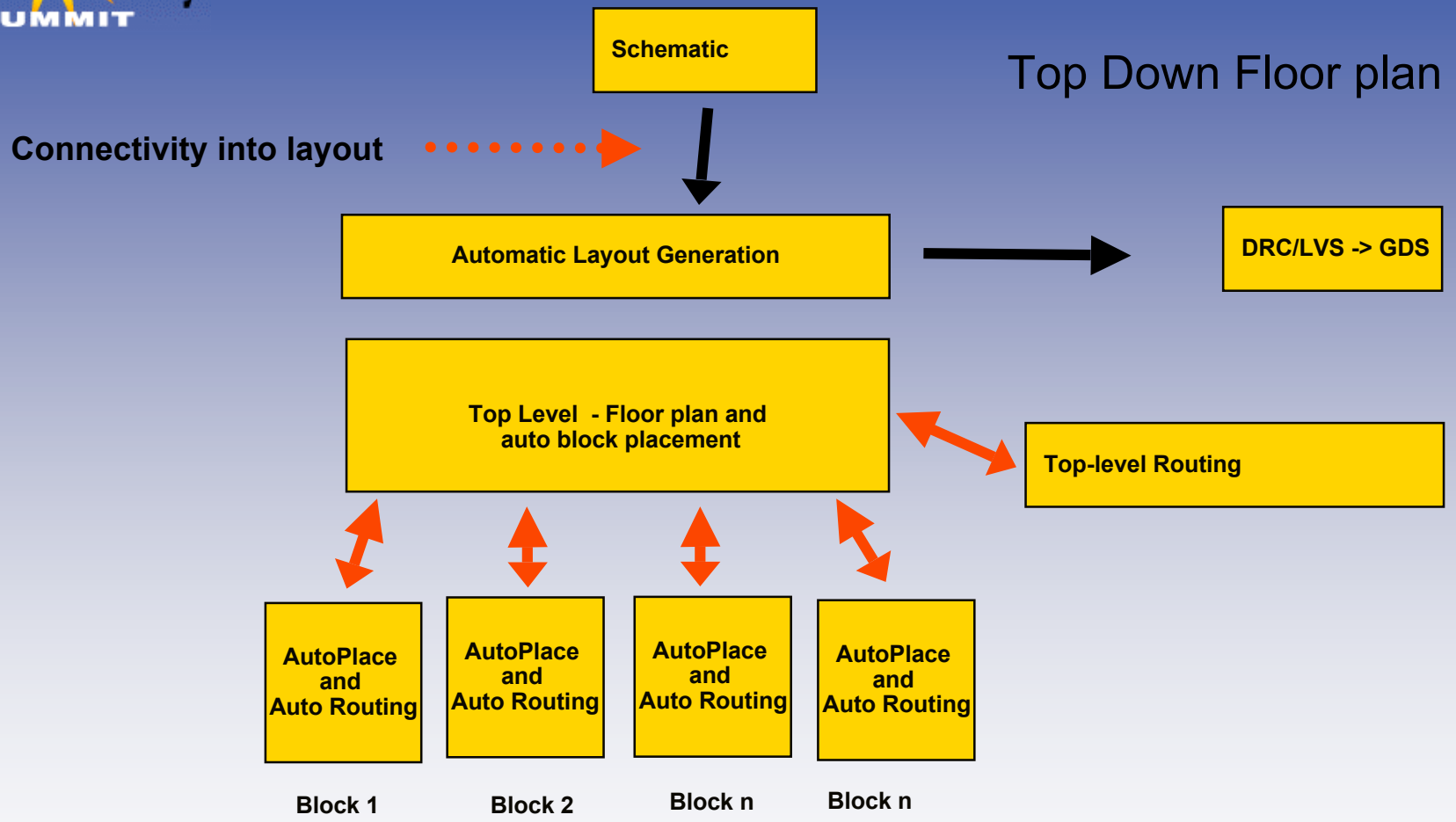
Often No connectivity into layout



Layout typically completed manually

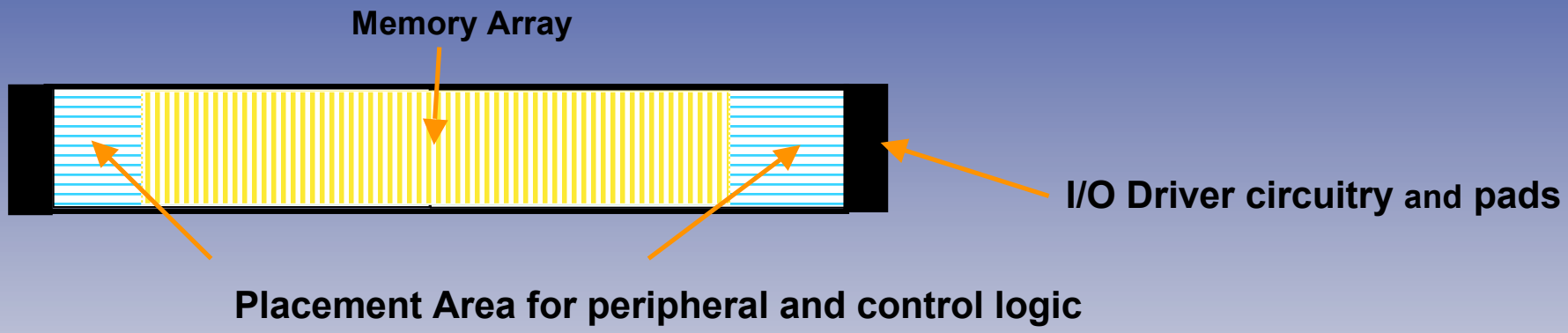
Conclusion: Top Down Integrated and automated solution required

FLASH Memory Physical Design – Desired Flow



A 'top down', integrated and automated solution is required

Key Issues for layout of peripheral logic for FLASH

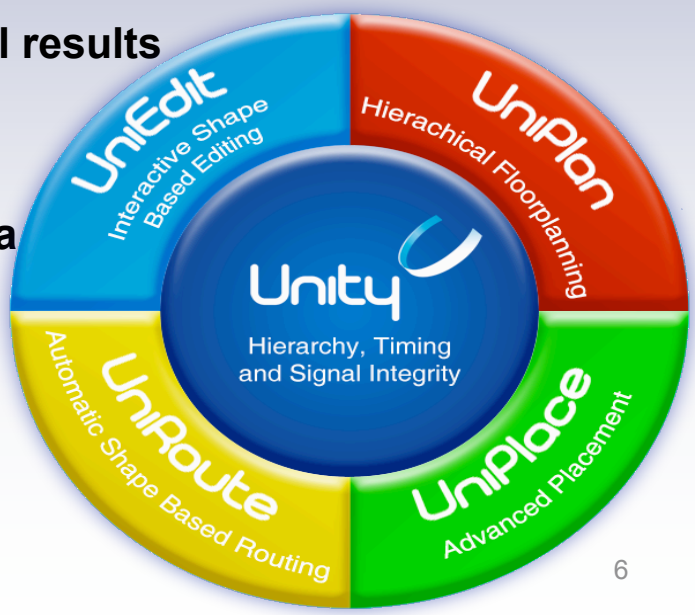


- **Characteristics and requirements for peripheral logic layout for FLASH**
  - **Long and narrow aspect ratios of layout regions.**
  - **Need for control of specific layers (e.g. highly resistive layers)**
  - **Automation for low number of routing layers (e.g. 1-2 layer)**
  - **Specific placement and routing methodology required to meet area target and yield**
  - **nm process nodes are driving requirement for increased automation for productivity.**

- **Standard ASIC technology inappropriate and difficult to control to achieve required results.**

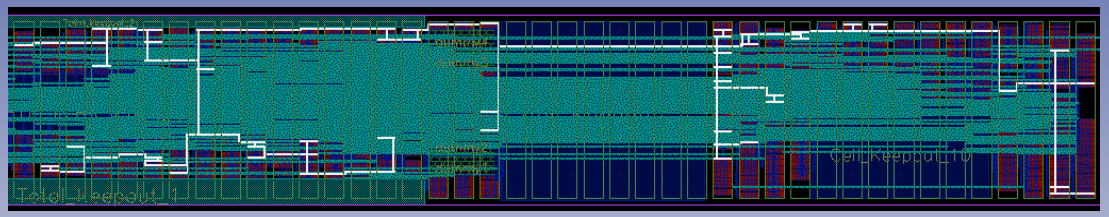
Automating Custom Design with an Integrated Tool

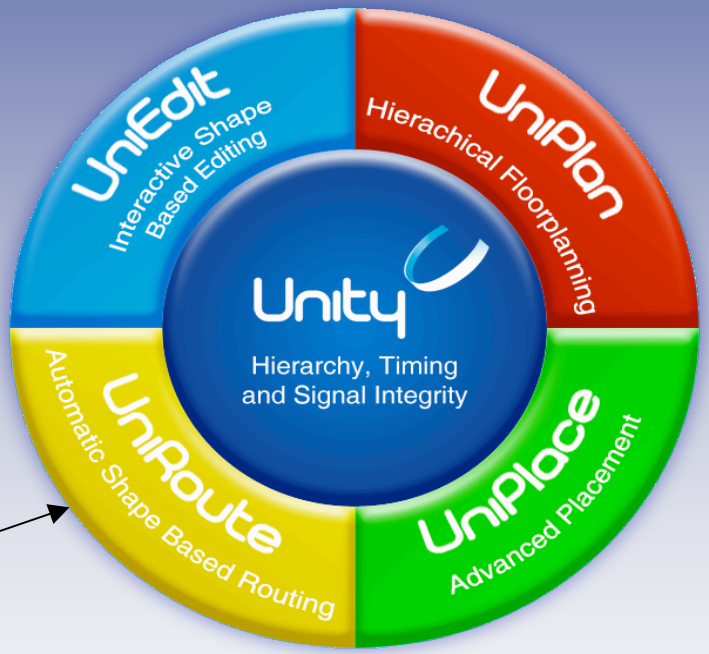
- **Automation of the layout of peripheral logic is possible with an integrated custom tool specializing in memory designs**
  - **Integration of floorplanning, placement and routing is mandatory**
- **Top down full chip floorplanning methodology has proven advantages versus manual effort or using tools not developed for floorplanning custom designs**
  - **Resources estimates more accurate**
  - **Reduced iterations at the Layout and Extraction phases**
  - **Easier and quicker to close timing**
  - **Management of hierarchy**
  - **Quicker Time to Market**
- **Dedicated placement strategies required for optimal results**
  - **Cluster placement**
  - **Routing aware placement**
- **Specialised routing techniques deliver smallest area highest yield and best performance**
  - **Shape based routing**
  - **Spine and Stitch routing**
  - **DFM aware routing**



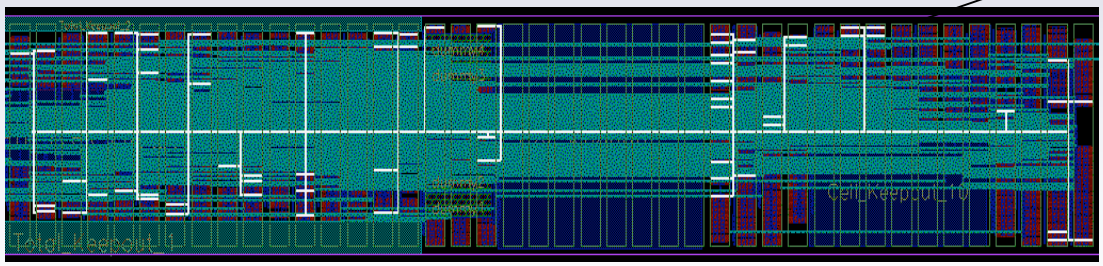
Example of Routing Results

Without Spine and Stitch Router





With Spine and Stitch Router



Summary

- Automation facilitates quick ‘prototype’ floor plan development in early stage of design process to calculate and verify full chip floor plan and area
- Provides opportunity to do power planning at top level and ‘push down’ to other levels of hierarchy at the beginning of the design process
- Allows die size to be estimated more accurately at an early stage of the design
- Provides designers with the ability to partition designs for parallel completion
- Accurate early stage planning, coupled with an integrated custom tool for floorplanning, placement and routing, provides a ‘real time’ view of floorplan, parasitics and power and allows design team to complete ICs earlier and within target metrics for time, size and budget

Custom Design Automation

Steve Ferguson
Technical Director

steve.ferguson@pulsic.com