NAND Interleaving & Performance

What You Need to Know

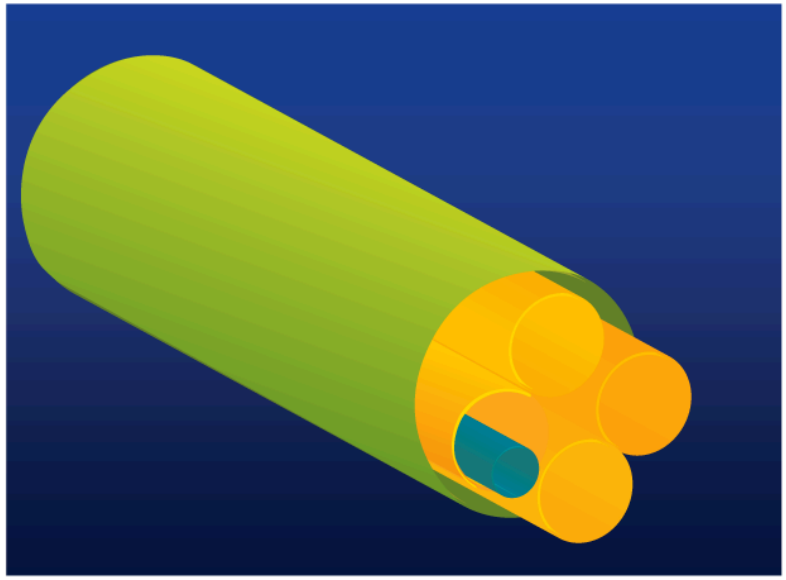
Presented by: Keith Garvin
Product Architect, Datalight

Overview

- What is interleaving, why do it?
- Bus Level Interleaving
- Interleaving Between Flash Planes
- Conclusions

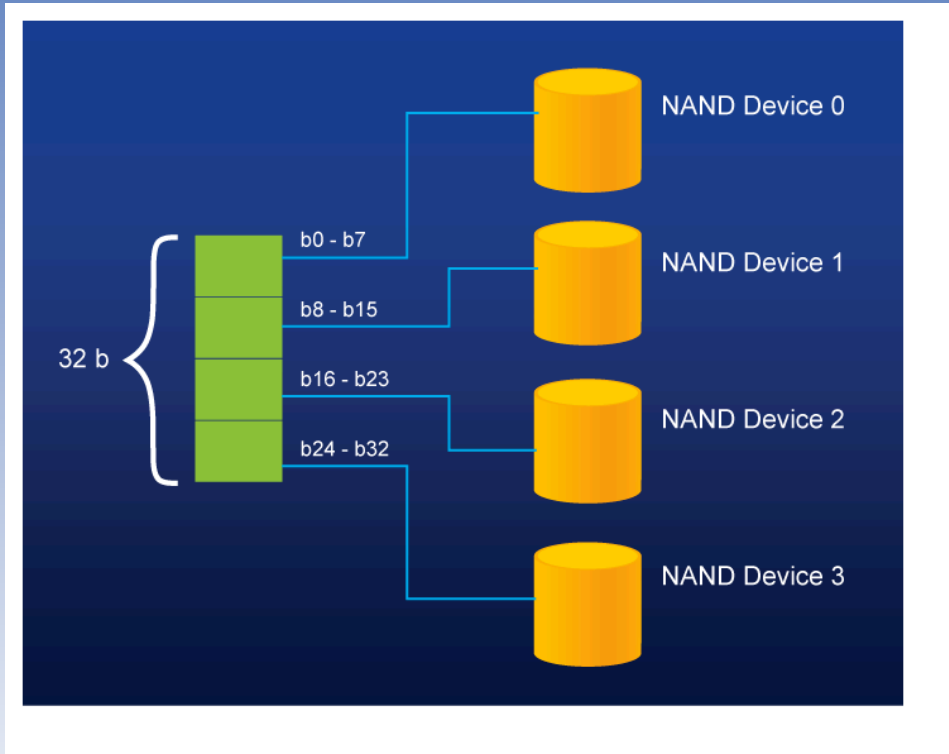
What & Why of Interleaving?

- What is Interleaving
  - Device bus interleaving
  - Flash Plane Interleaving
  - IO Interleaving (concurrency)



Device Bus Level Interleaving

- Hardware Simplicity
- Potential Return: Two devices = 2X the performance (per IO cycle)
- Additional overhead is minimal



Device Bus Level Interleaving

- Flash Characteristics
  - Minimum programmable size will increase
  - Error rates increase with added devices
  - Increased Power Consumption

Device Bus Level Interleaving

- Challenges of Bus Level Interleaving
  - Large page size may necessitate double buffering
  - 2X Error rates require interleaved EDC or more powerful correcting codes
  - Increased bad block counts require more complex mapping of bad flash erase blocks

Device Bus Level Interleaving

- Increased Power Consumption
  - Achieving large disks (100's of GB to TB) will require unique heat dissipation strategies.
  - Large SSDs will need to carefully consider device placement and airflow.

Flash Plane Interleaving

- Interleaving Between Flash Planes
  - No special system hardware design is needed
  - Flash hardware & software must support planes
- Potential Return
  - 2X on paper, implementation range: 30% to 80%
  - Flexible implementation in software

Flash Plane Interleaving

- Challenges with Flash Plane Interleaving
  - Access must be restricted to matching page address ranges across device planes
  - Bad blocks may prevent multi-plane operations where present
  - Managing bad blocks across planes requires unique solutions

More interleaving…

- What does all this add up to???
  - Bus level interleaving is good – match the native width to maximize throughput.
  - Interleaving across device planes achieves even more performance improvements.
  - One more to consider…

IO Concurrency

- Take advantage of multi-die packages
  - Separated R/B# pins allow for concurrency
  - RAID0 style interleave without the penalty of altered geometries
  - Make certain your design has DMA to handle moving all this data.

Interleaving Challenges

- Flash Page Size Increases
  - Devices **may not** support partial page writes.
  - May require double buffering.
  - File systems or legacy applications may not accommodate larger write sizes.
  - Know the application, use case, and hardware capabilities.

Interleaving Challenges

- Bad Block Management
  - Bus level interleaving increases bad block counts.
  - Bad blocks will negate some performance gains.
    - Plane interleaving may not be realized.
  - Software solutions will have more flexibility
  - If rolling your own, investigate the IP rights.

Interleaving Challenges

- Error Detection & Correction
  - Interleaving effectively increases error rate.
  - Errors may now exist within the same logical page or block.
  - Use a fast HW based ECC

Conclusions

- Ensure the hardware & software supports
  - Your flash hardware, interleaving requirements, and performance requirements.
- Establish an interleaving balance
  - Consider the burst rate, latency, and sustained
- Use the performance features provided by the flash (multi-planes, cache mode, …)

Further Reading

- Micron – Increasing NAND Flash Performance
  http://www.micron.com/products/nand/technotes

- Datalight – Blog
  http://www.datalight.com