ONFI 2.0 – The Compatible NAND Flash Interface

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Abstract

- ONFI 1.0 standardized the asynchronous NAND Flash interface with significant industry acceptance. It greatly simplified the protocol, command set, and NAND signals providing a stable, consistent interface on which to design controllers and reduce compatibility testing.

- ONFI 2.0 maintains backwards compatibility to ONFI 1.0 and adds a faster, synchronous I/O interface to meet today's demanding high-performance needs. No alternative NAND interface supports backwards protocol- and signaling-level compatibility; it makes for an easy migration and upgrade path for today's high-performance controllers to support both source synchronous and asynchronous NAND Flash. ONFI 2.0 is publicly published (http://www.onfi.org/) and has the industry support of over 80 member companies.

The NAND Interface Today

- ## ONFI 1.0 standardized today's NAND interface
  - Consistent and easier for controller designers to identify and use NAND features through use of the parameter page

- ## ONFI 1.0 introduced timing mode 5 for faster I/O throughput
  - New standard for NAND interface performance
  - tRC / tWC = 20ns

Read Performance

4 Gb Plane

330MB/s

Page Buffer (4KB)

Page Buffer (4KB)

4 Gb Plane
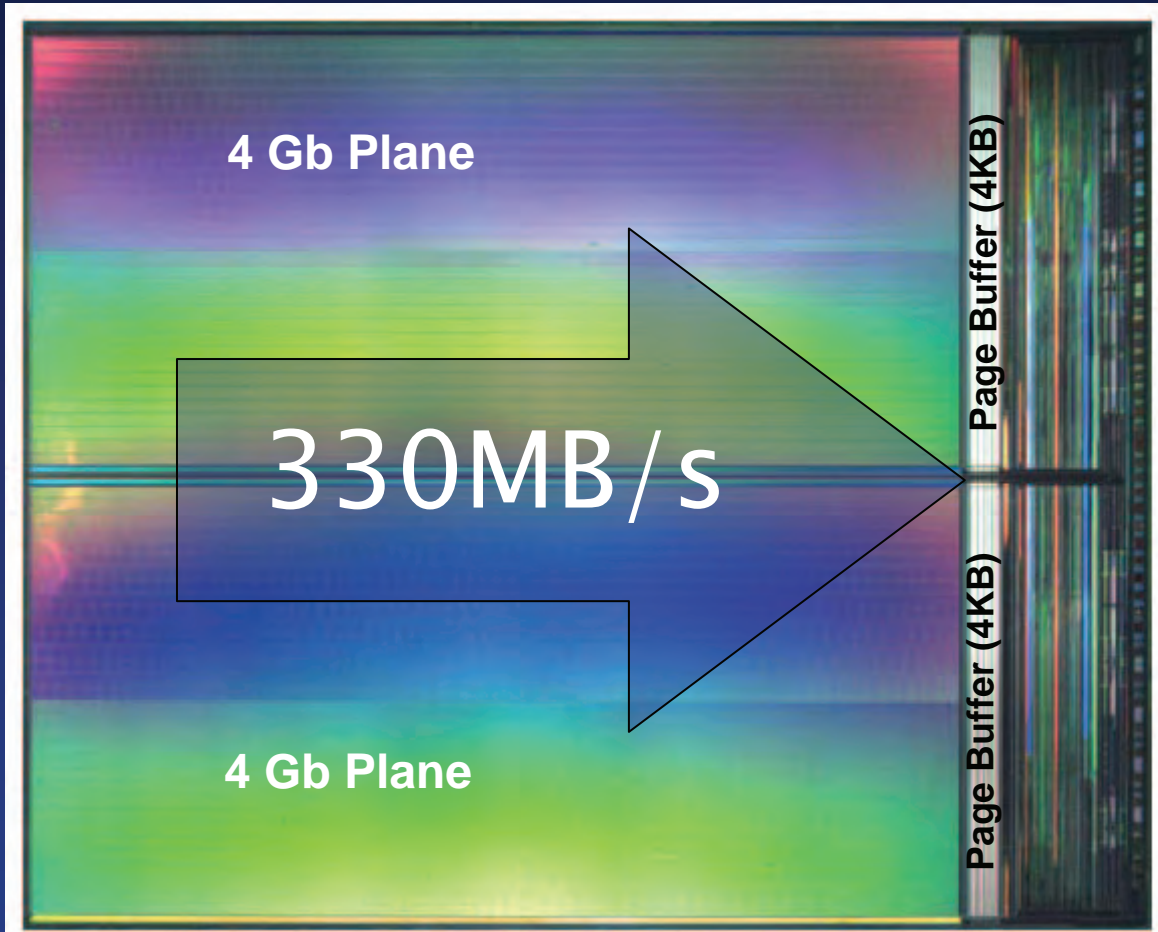
40MB/s

NAND array reads are parallel and very fast

- Read array bandwidth is greater than 330MB/s (8KB read in 25us)

Interface speed is the limiting factor

- Read bus bandwidth is 40MB/s (25ns clock)

Total throughput after array read and I/O transfer is 34MB/s

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Single Channel I/O Bottleneck

Device	Planes	Data Size	Array Read (tR)	Data Output (tRC * Data Cycles)	Total Read Performance
SLC 4KB page	2	8KB	25µs	211µs	34MB/s
MLC 4KB page	2	8KB	50µs	211µs	30MB/s

- Read performance is I/O limited because $tIO \gg tR$.

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I/O Throughput Cannot Scale

- NAND Flash Interface is asynchronous
- NAND timing parameters cannot scale indefinitely to faster speeds
- As tRC decreases, it becomes difficult for controllers to latch data output from the NAND
- As tWC for data input decreases, time to process command and address cycles does not decrease

40% faster	17% faster	25% faster

| 50ns I/O | → | 30ns I/O | → | 25ns I/O | → | 20ns I/O |

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Goals of the ONFI 2.0 Source Synchronous NAND Interface

- Keep transition to high-speed interface simple
  - Keep and/or redefine original NAND signals to provide high-speed signaling without disrupting the NAND protocol and command set
  - Provide backwards compatibility to asynchronous NAND interface to make device identification simple

- Increase I/O throughput with room to grow
  - Remove tRC latching limitation by adding a bi-directional source synchronous strobe (DQS)
  - Remove tWC command and address cycle limitation by decoupling command and address processing from the data input rate

- Insure a graceful transition from the standard, asynchronous NAND Flash interface to the source synchronous interface

Scalable I/O Performance

- A scalable interface is needed for more than read I/O throughput

- As more NAND devices are added to the bus even slower MLC devices will max the I/O bus bandwidth

  - A fast NAND Flash interface is possible by:
    - Adding bi-directional source synchronous DQS
    - Providing scalable DDR data I/O interface
    - Optimizing the signaling to allow enough time to process command and address cycles
    - Minimizing NAND pin capacitance

ONFI 2.0 Source Sync Read Performance

4 Gb Plane

330MB/s → **200MB/s**

4 Gb Plane
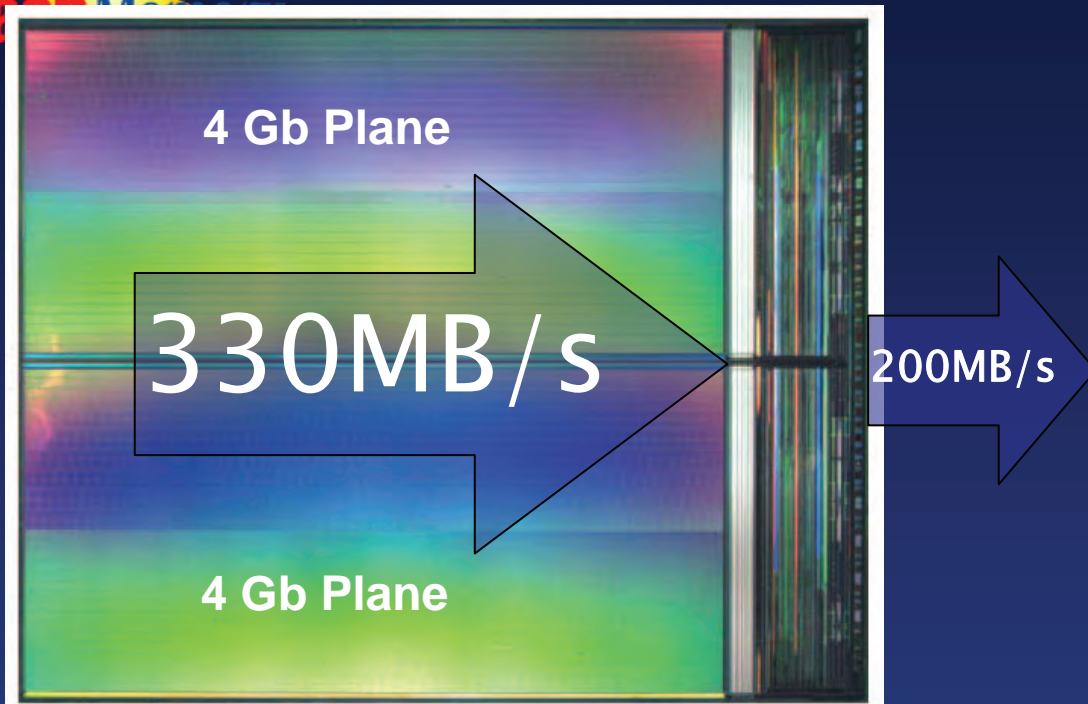
Shows significant improvement for single–die performance.

Shows significant gains for multiple die on the same channel.

Device	Planes	Data Size	Array Read (tR)	Data Output (tCK/2 * Data Cycles)	Total Read Performance
SLC 4KB page	2	8KB	25µs	43µs	120MB/s
MLC 4KB page	2	8KB	50µs	43µs	88MB/s

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NAND ⇨ Source Sync NAND Interface

Asynchronous NAND Interface

NAND

CE#
ALE
CLE
RE#
WE#
R/B#
WP#
I/O[7:0]

Source Synchronous NAND Interface

DQS

NAND

CE#
ALE
CLE
W/R#
CLK
R/B#
WP#
DQ[7:0]
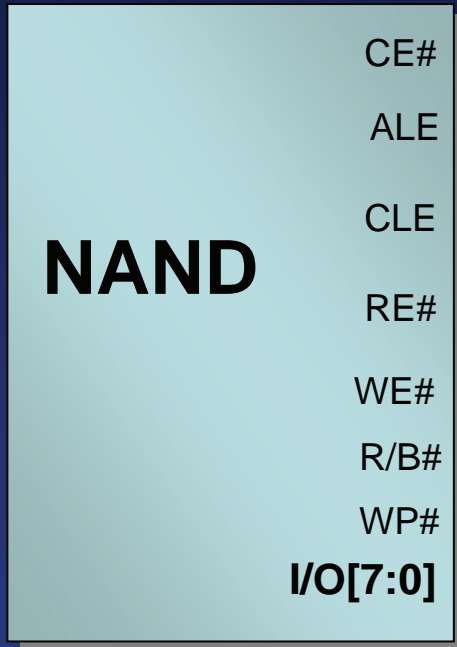
- High-speed-capable NAND Flash devices power on using the asynchronous interface for backwards compatibility

- Set Features enables source synchronous interface

- WE# becomes a fast CLK

- RE# handles data direction by becoming W/R# (Write/Read#)

- I/O[7:0] renamed to DQ[7:0] (name change only, functionally identical)

- DQS, a new bi-directional signal, is enabled

Source Synchronous Signal Description

Signals		Description
Async	**Sync**	
WE#	CLK	▪ Free-running and used to latch command and address cycles ▪ During idle CLK may be stopped to save power

RE#	W/R#	▪ Controls direction of DQ bus and DQS
		  • W/R# = "1": Data input
		  • W/R# = "0": Data output

—	DQS	▪ During data phase, each DQS rising and falling edge corresponds to a data byte
		  • DQS is center-aligned for data input
		  • DQS is edge-aligned for data output

ALE / CLE	ALE / CLE	▪ For source synchronous mode:
		  • ALE / CLE = "11": Data transfer
		  • ALE / CLE = "00": Bus idle
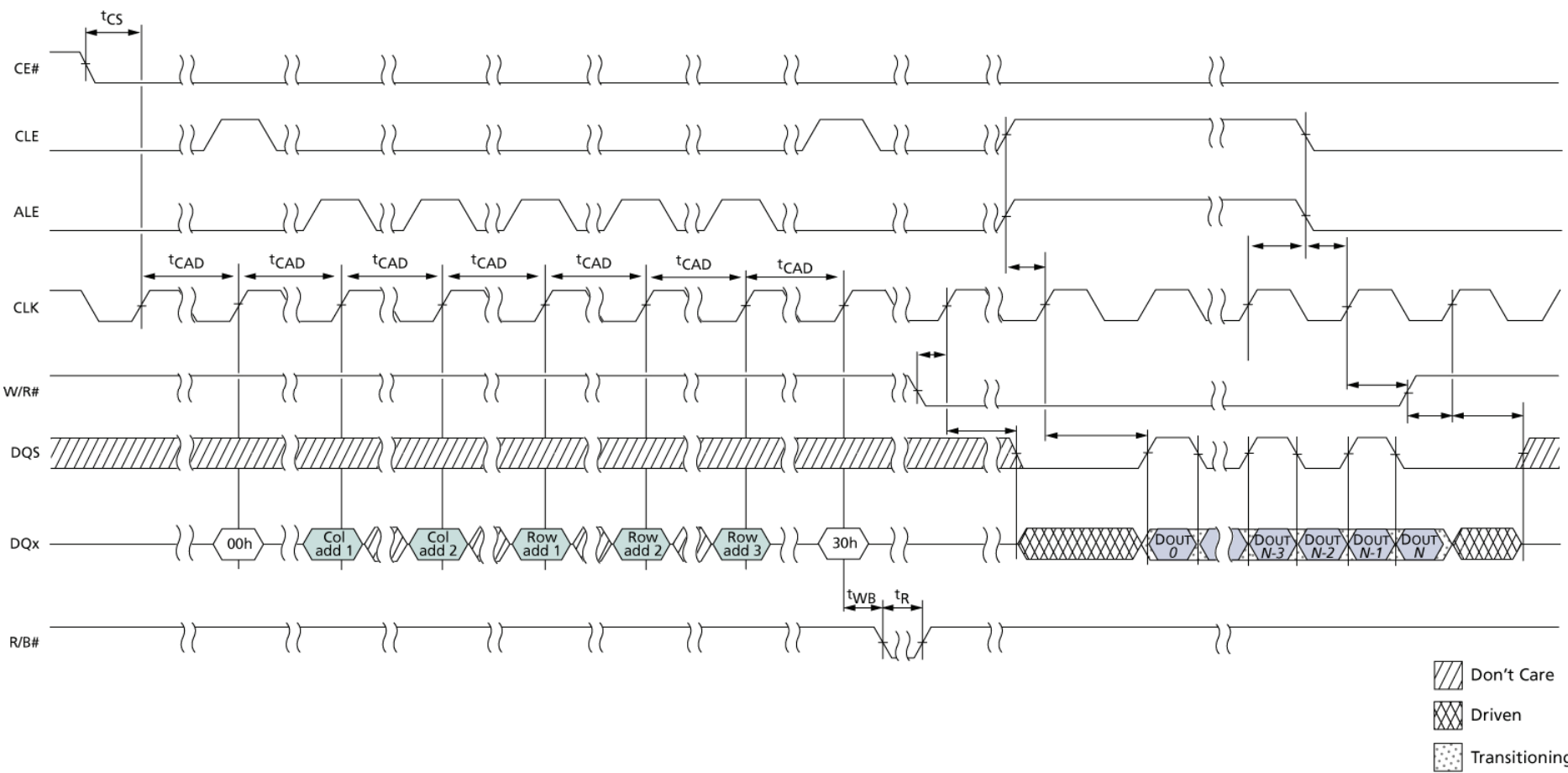
Low Power Signaling

- As process geometry shrinks it becomes more difficult for controllers to stay with 3.3V I/O
  - Many applications today use 1.8V signaling
  - Many high-speed interfaces today use smaller voltage swings so signals can transition faster

- NAND Flash today requires the array and I/O to operate at the same voltage
  - V_{cc} = 2.7-3.6V, or
  - V_{cc} = 1.7-1.95V

- NAND Flash array operations perform best when V_{cc} > 1.8V providing faster Program, Read, and Erase times

- By splitting the array voltage (V_{cc}) from the I/O voltage (V_{ccQ}) it is possible to get fast array operations *and* faster, lower power I/O signaling

- Potential high-speed voltage configurations
  - V_{cc} = 2.7-3.6V, V_{ccQ} = 2.7-3.6V
  - V_{cc} = 2.7-3.6V, V_{ccQ} = 1.7-1.95V

High-Density Scalability

- By providing multiple output drive strength settings many NAND devices can share the I/O bus while maintaining I/O throughput.

- Example: 133MT/s data throughput

- Net result: Higher performance for fewer I/O channels

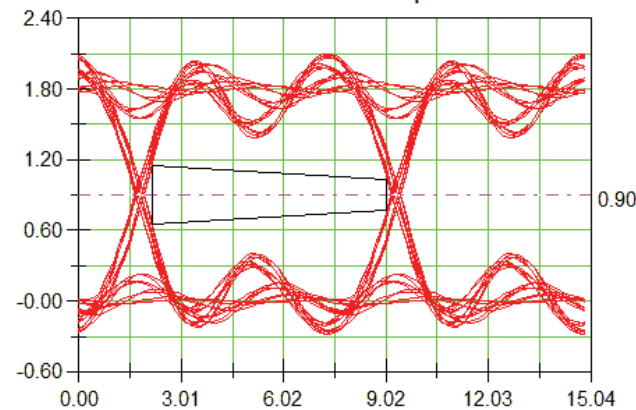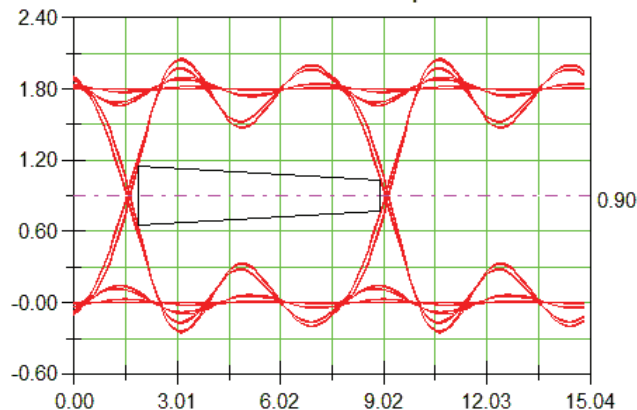35-ohm driver, 4 NAND die   25-ohm driver, 8 NAND die   18-ohm driver, 16 NAND die
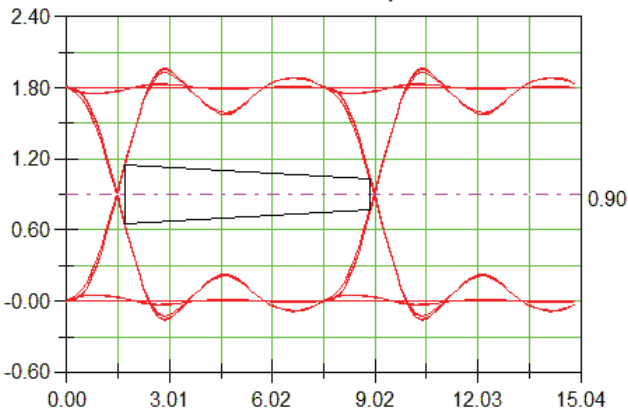
Packaging

- Source-synchronous-capable packages receive
  - DQS signal
  - Some Vcc change to VccQ
  - Some Vss change to VssQ

- The following packages have been transitioned
  - 48-pin TSOP
  - 63-ball BGA

Introducing a New BGA Package

- ONFI 2.0 introduced a new 100-ball BGA package

  - Accommodates source synchronous *and* asynchronous-only NAND Flash devices

  - Dual x8 interface

  - More power/ground balls for lower noise

  - Signals arranged for excellent signal integrity

  - 1mm ball spacing for low-cost PCB assembly

  - Accommodates ever-increasing NAND densities with two package outline options

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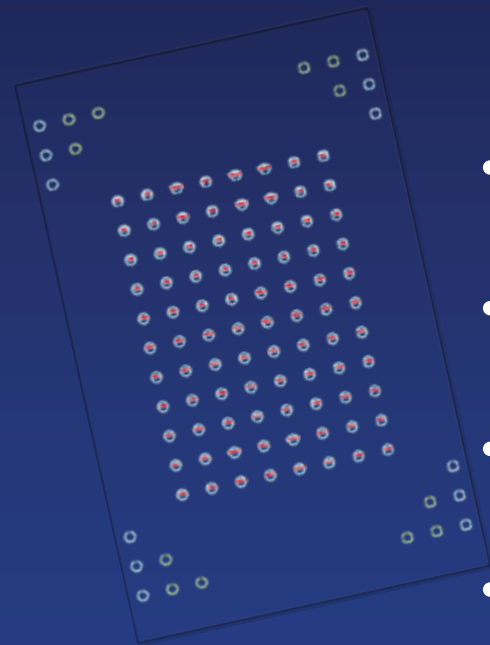
ONFI 2.0 Summary

- The source synchronous interface defined in ONFI 2.0 increases the bandwidth of each I/O channel while adding only one pin, DQS.

- The interface can scale up to 200MT/s in the first generation.

- Designed for up to 16 die per I/O channel through use of output impedance control

- The protocol is backwards compatible to asynchronous NAND reducing or eliminating firmware changes for command set and device behavior

- No DLL required in the NAND Flash devices

- May necessitate a new high-speed PHY in controllers, but was designed to be similar to mobile DRAM controller interface → evolutionary *not* revolutionary

- Because ONFI 2.0 devices are backwards compatible with the asynchronous NAND interface, controllers that only support the asynchronous interface can still use these devices

ONFI Connectors

- ONFI defined a connector for NAND modules

- Form factors for small and larger form factors

- Modules support both asynchronous-only and source synchronous NAND Flash devices

Small Form Factor Module & Connector

ONFi
OPEN NAND
FLASH INTERFACE

SONY (intel) **hynix** **SPANSION**

N numonyx

Micron **PHISON** Knows What You Need

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Super Talent Electronics	Synopsys	Tandon
Tanisys	Telechips	Teradyne, Inc.
Testmetrix	Transcend Information	Tyco
UCA Technology	University of York	Virident Systems
WinBond		

ONFI Membership

- Participation in ONFI provides opportunity to review each draft of the specification

- Membership open to all NAND vendors, enablers, and OEMs

- There are currently no dues

- Download application at http://www.onfi.org

For more information…

- Open NAND Flash Interface
  - ONFI 2.0 specification: http://www.onfi.org/
  - ONFI 2.0 webinar: http://www.nand.com/

- Micron High Speed NAND
  - Product details: http://www.micron.com/highspeednand
  - Marketing Brief:
    http://download.micron.com/pdf/datasheets/flash/nand/8gb_nand_mktg_brief_m51h.pdf
  - The full product data sheet is also available (NDA required)

- Micron's NAND Webinars:
  http://www.micron.com/products/nand/nand_webinars

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About Michael Abraham

- Manager of Micron's NAND Flash Applications Engineering group

- B.S. in Computer Engineering from Brigham Young University

- Micron's technical representative in ONFI and JEDEC for NAND Flash

- Key role in defining and standardizing the new high-speed NAND interface within Micron and at ONFI

Santa Clara, CA USA
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