Addressing System Challenges for Next Generation SSD SoCs

Ian Ferguson

Director, Enterprise Solutions

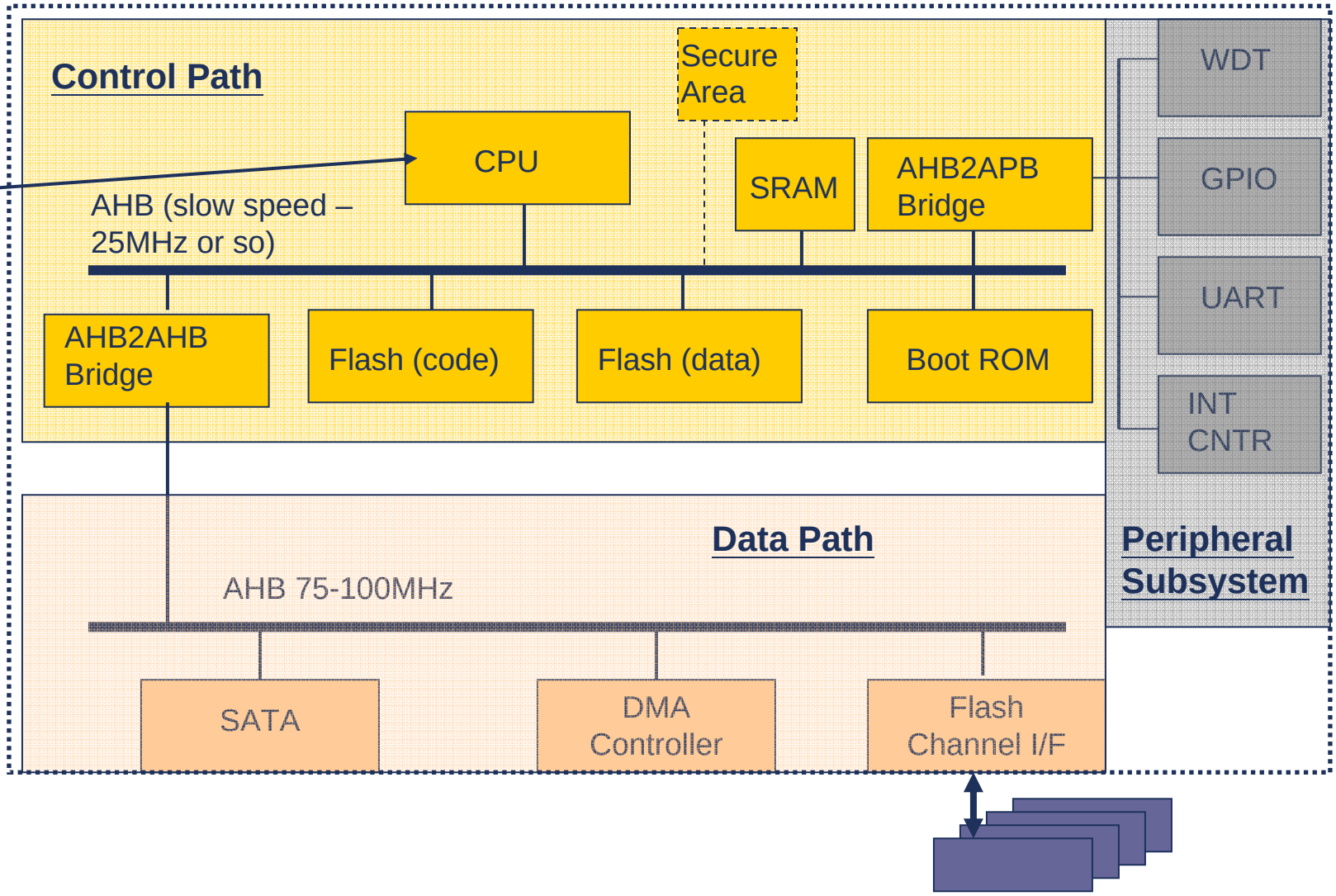
Email: ian.ferguson@arm.com

Drivers on Flash Controller CPU Performance

- Increasing complexity of wear leveling algorithm
  - Higher densities increase number of blocks to be managed
  - Reduced number of write accesses supported by MLC technology
- Write performance
  - DRAM buffers helps, but introduce other issues
- Host interface data rate

Inside a Current SSD……

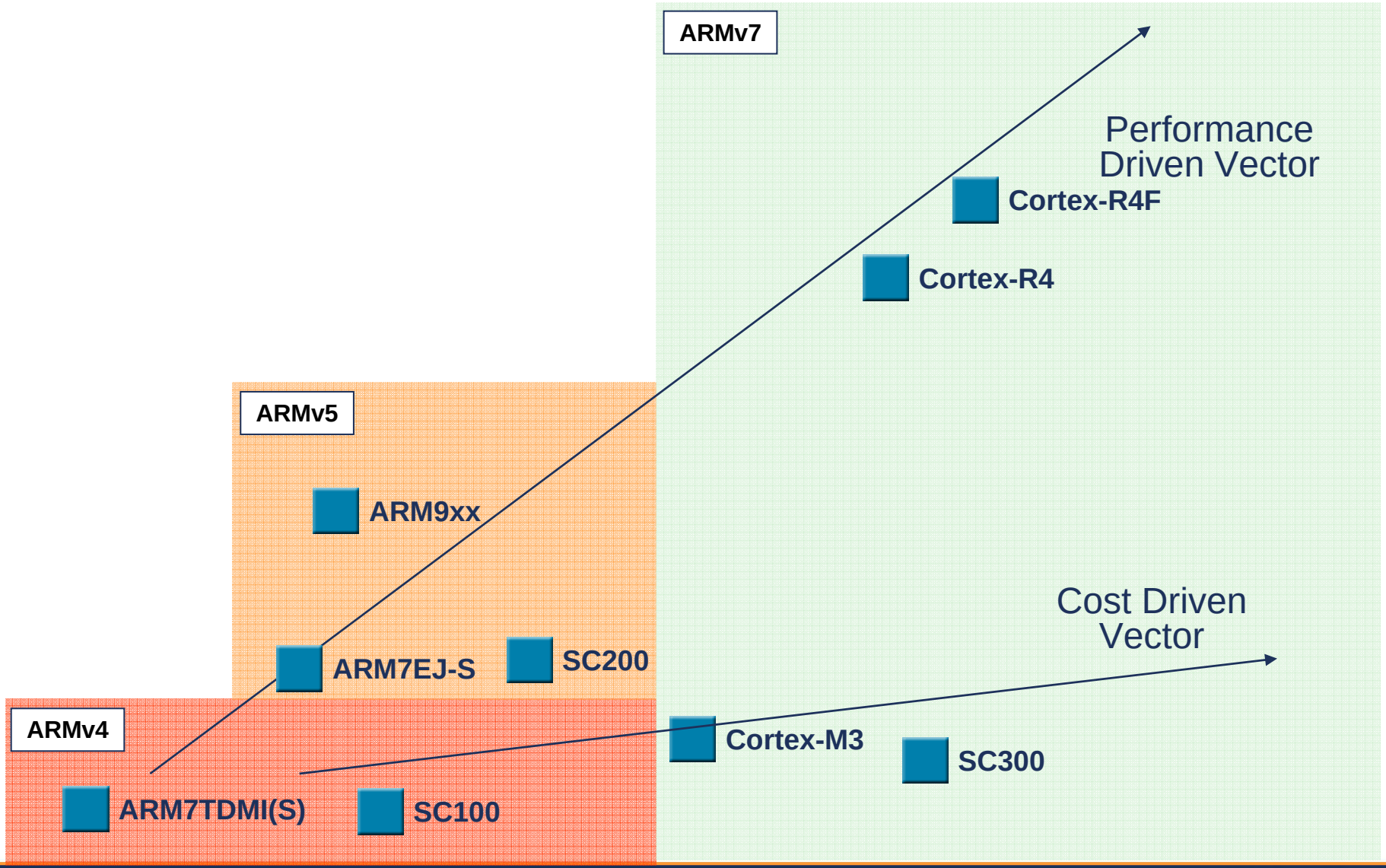
CPU establishes DMA transfers, implements wear leveling algorithms



No One Size Fits All

- Performance driven applications (Enterprise…)
  - Migration to asymmetric multiprocessing architecture
  - Single core to manage host interface
  - CPU core per 4-8 channels of flash for local wear leveling etc
- Mainstream SSD (Notebook, ULPC…)
  - Single CPU architecture with frequency pushing toward 500MHz
- NAND Flash card (SD-Card, USB…)
  - Migration from 8-bit to 32-bit CPU technology

Breadth of Code Compatible Offerings



Additional Challenges

- Sophisticated system debug vs. data security conundrum
- Power
- Minutia differences between electrical interfaces of different flash technology
- Cost to drive mainstream adoption of SSD
  - LCPC Retail $399
  - BOM $199
  - Storage ~20% of BOM

Summary

- We think SSD market predictions will be revised upwards
  - Momentum from Computex and entrants like Intel
- No standard core or SoC architecture during this early adopter cycle
- The keys
  - 32-bit CPU technology
  - Breadth of code compatible options to leverage software investment
  - Multi-core and (ultimately) secure debug
  - Die size minimization