

Integrating Solid State Storage and DRAM onto Standard Memory Module Form Factor (SSDDR)

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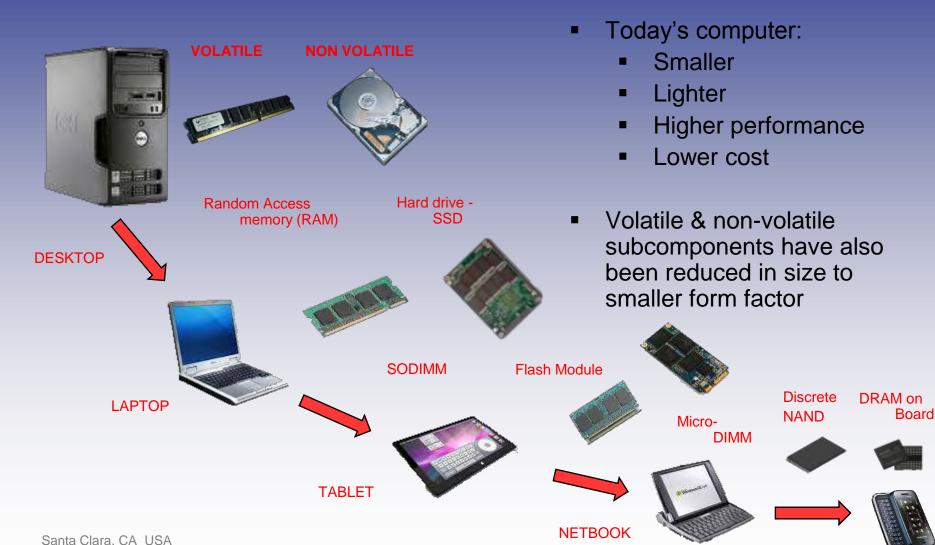
Agenda

- The Need to Integrate SSD & DRAM onto a Module
- Today's Technologies make SSDDR Possible
- A Bright Future for SSDDR
- The Road Ahead for SSDDR Applications



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The Need to Integrate SSD & DRAM onto a Module





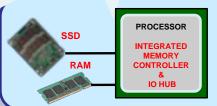
The Need to Integrate SSD & DRAM onto a Module

- Future potential: single chip, single package – a complete processor integrating memory controller and I/O controller
- A need to scale volatile & non-volatile subcomponents (SSD & DRAM) onto a single, small form factor

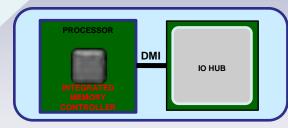
Increase overall system performance

Lower power

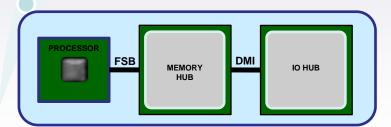
1-CHIP INTEGRATION



2-CHIP INTEGRATION

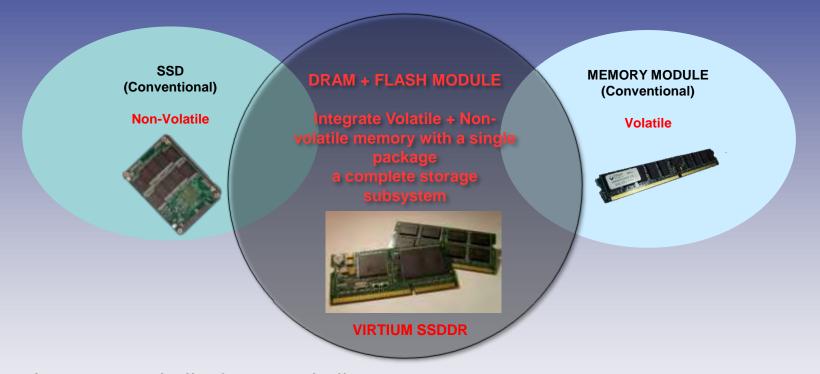


3-CHIP TRADITIONAL DESIGN





The Need to Integrate SSD & DRAM onto a Module



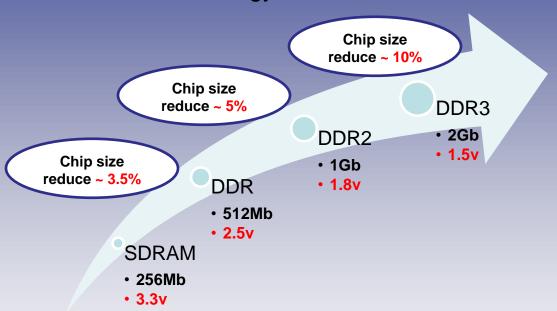
Integrate volatile & non-volatile to:

- Save cost
- Increase overall system performance, lower the power consumption
- Scale to smaller form factor and lighter weight

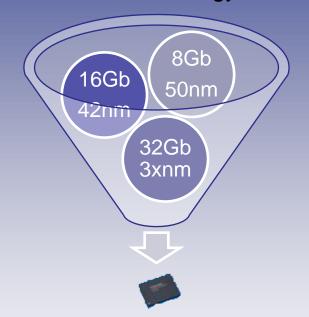


Today's technologies make SSDDR Possible - Components

DRAM technology trends:



NAND flash technology trends



- Smaller DRAM & Flash components make the integration possible in a small form factor i.e. SODIMM
- Low power consumption components help to reduce design complexity i.e. reduce number of power supply input pins and consolidate two different voltage technologies into a single voltage supply

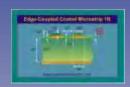


Today's technologies make SSDDR Possible – PCB Technology



Memory Module stack-up & Impedance requirement

SSD stack-up & Impedance requirement



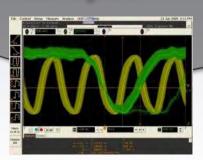
8 layers stack-up (SODIMM)

- Single end 0.1mm width
 - Outer layer 60 ohms +/- 40%
 - Inner layer 55 ohms +/- 10%
- Differential 0.1mm width
 - 88 ohms +/- 1/0%

Mixed signal PCB technology enables the integration of these two technologies

Combine onto a 40 mil thick – 10 layers PCB

Maintain signal integrity and crosstalk between mix and match signals



4 layers stack-up

- Single end 0.1mm width
- 50 ohms +/- 10%
- Differential 0.1mm width
 - \100 ohms +/- 5%

	Violate	Cutor	Layer Harris	Type	Usage	mile, co	10	mile	atter:
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2	122		9 (28)	PARKE	Rand		Allegen	28	52.6
1	100			Dielectric	ELECTRICAL SECTION 1	2.6	3.6		
4	12		1.2 GHD PLANET	RASE OF	Hand	9.5	454din	1	83
E	1000		-	Develope	To do til mine		38		
18.	F		17-DA7A_600	Make at	(Signol-	10.6		9.	117
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15.	1000			DREADIN	Subspirate.		2.9		
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21	10000			Deliverate	Table Wash	0.2	. 54		

				1 Dierance	MILITARIA	MIGKERITORIE
Substrate 1 Height	H1	5,0000	+/-	0.0000	5.0000	5.0000
Substrate 1 Dielectric	Er1	4.2000	+/-	0.0000	4.2000	4.2000
Lower Trace Width	W1	8.0000	+/-	0.0000	8.0000	8.0000
Upper Trace Width	W2	7.5000	+/-	0.0000	7.5000	7.5000
Trace Separation	S1	14.0000	+/-	0.0000	14.0000	14.0000
Trace Thickness	T1	1.3000	+/-	0.0000	1.3000	1.3000
Coating Above Substrate	C1	0.4000	+/-	0.0000	0.4000	0.4000
Coating Above Trace	C2	0.4000	+/-	0.0000	0.4000	0.4000
Coating Between Traces	C3	0.4000	+/-	0.0000	0.4000	0.4000
Coating Dielectric	CEr	4.2000	+/-	0.0000	4.2000	4.2000



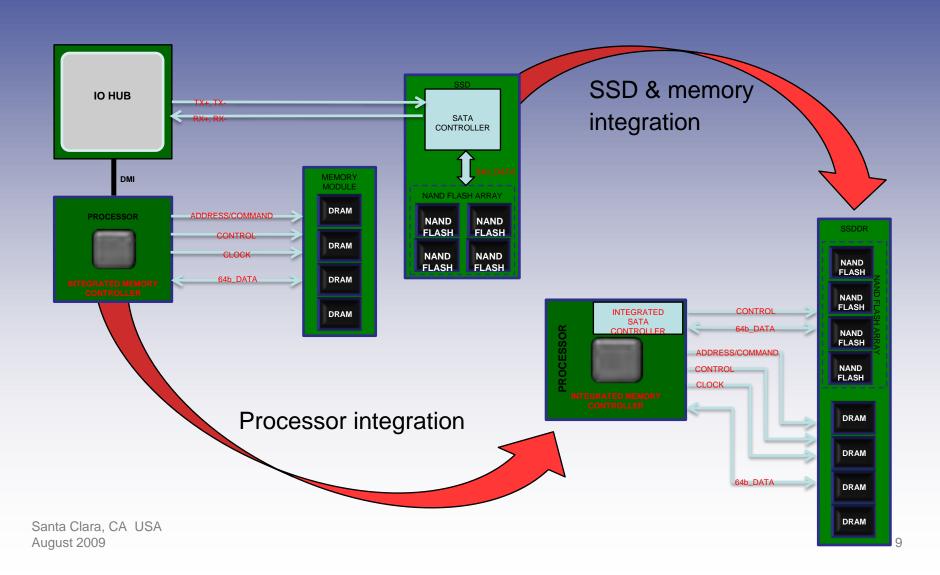
Today's technologies make SSDDR Possible

SSDDR Video





A Bright Future for SSDDR





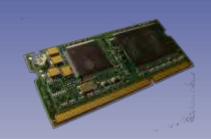
The Road Ahead for SSDDR Applications

SSDDR in use



Product Image Courtesy of PTi





Benefits of integrating Solid State Storage and DRAM onto Standard Memory Module Form Factor:

- Smaller
- Lighter
- Higher performance
- Lower cost



Q&A