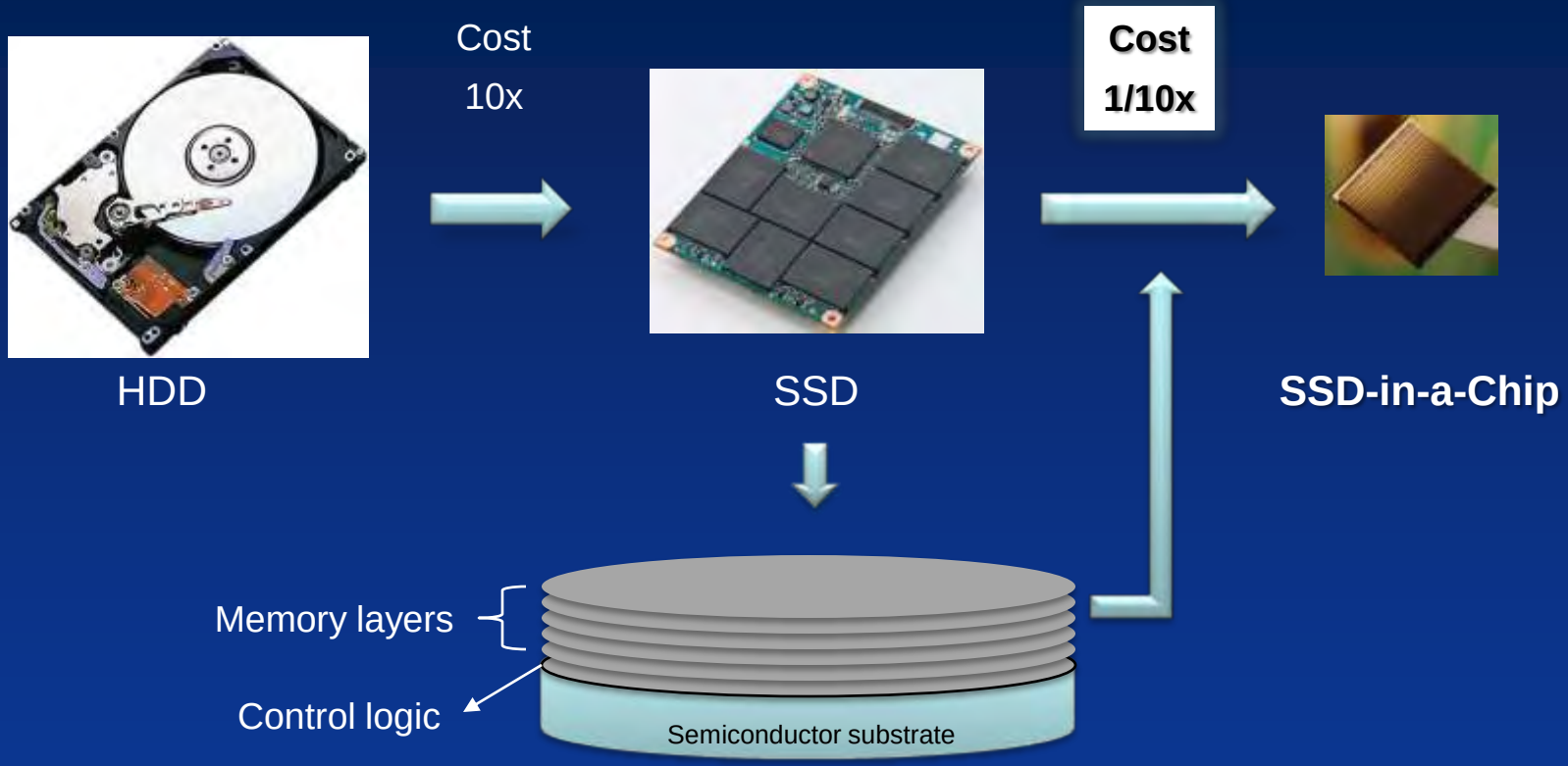
3D IC Architecture for SSD-in-a-Chip

Sang-Yun Lee

CEO of BeSang Inc.

SSD-in-a-Chip

Ultra Low Cost SSD Solution



High Density & Low Cost

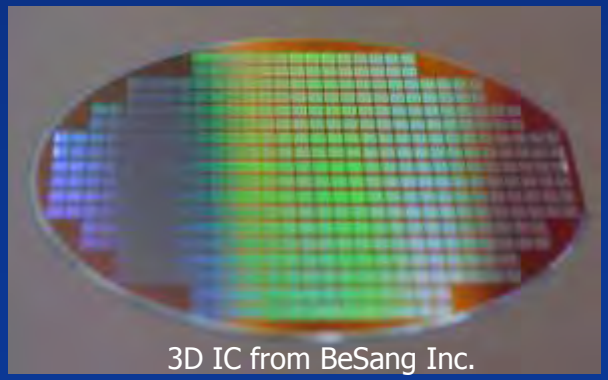
3D IC

Flash Memory for SSD-in-a-Chip

3D IC Architecture

For SSD-in-a-Chip

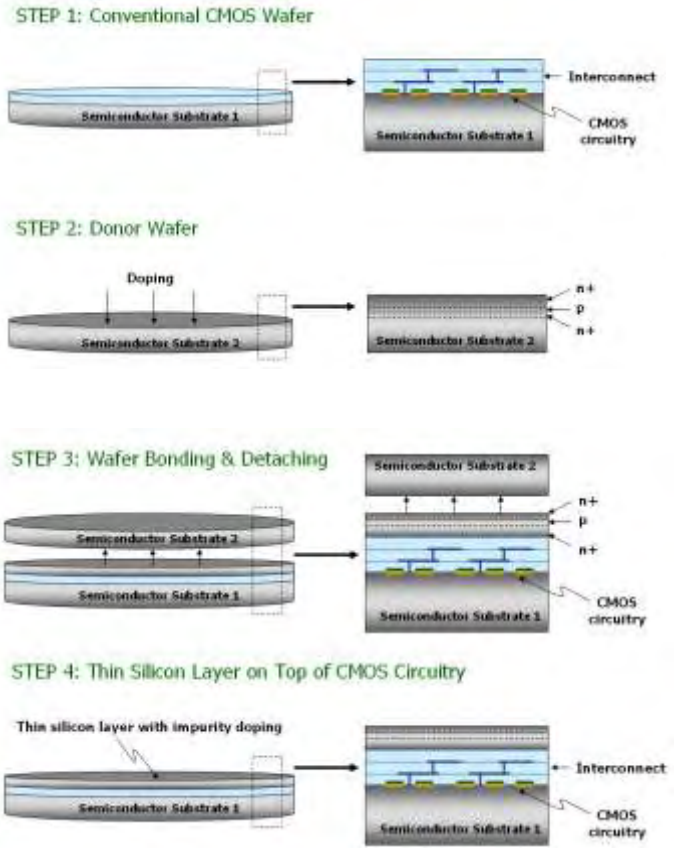
- Material: **Single crystalline silicon**
- Process temperature: **400 ºC** or below
- Flash cell structure: **Vertical transistor**
- No. of staking memory layers: **5**
- Stacked memory Layer Thickness: **< 500 nm**
- Overall effective flash memory cell size : **0.1 F^2**

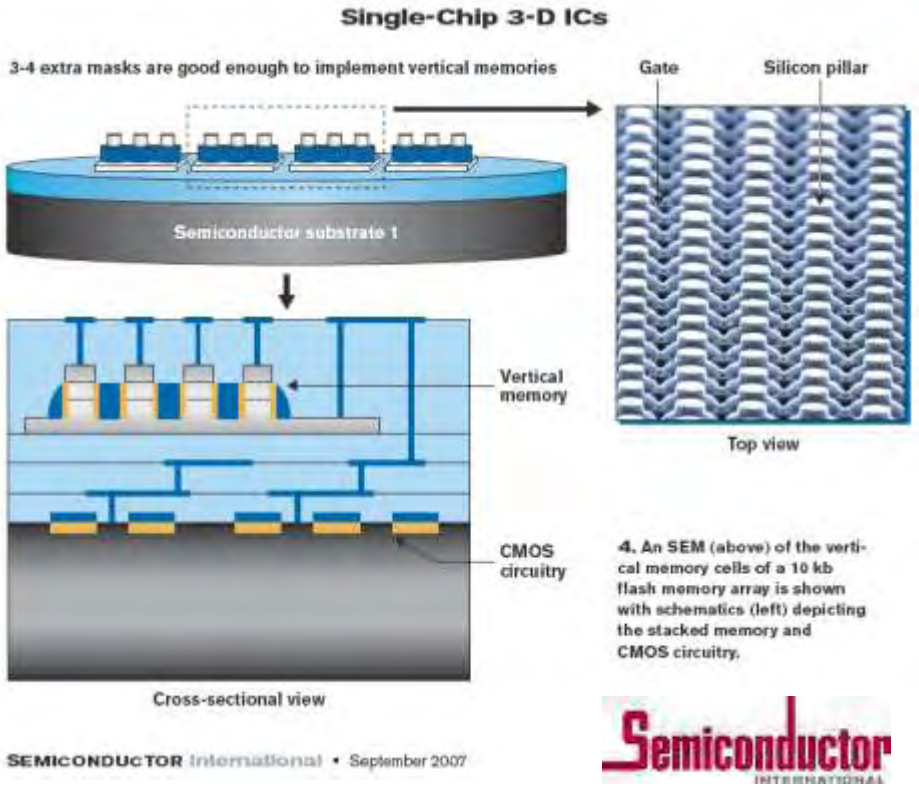


3D IC from BeSang Inc.

3D IC Process Flow

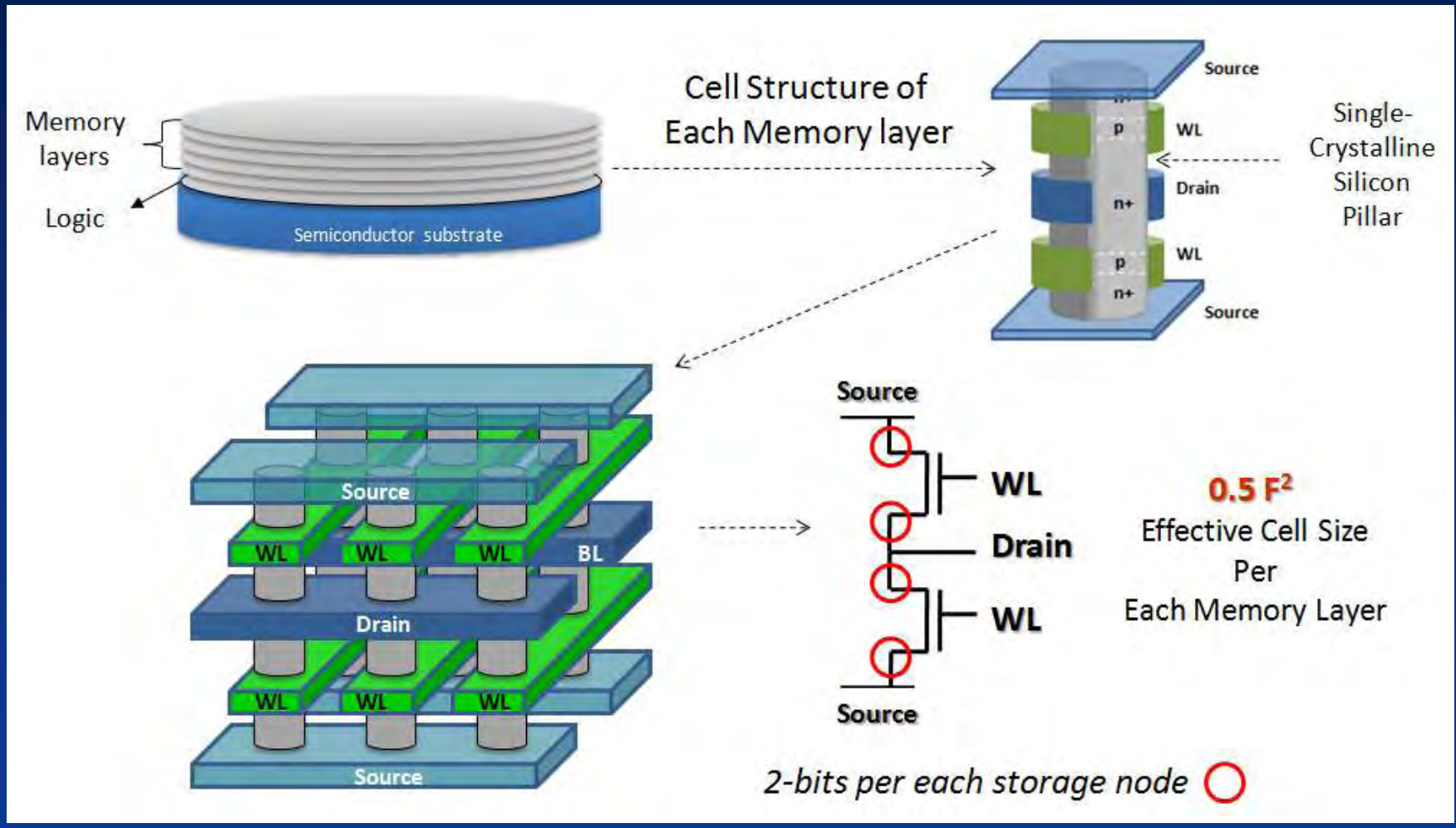
Overview



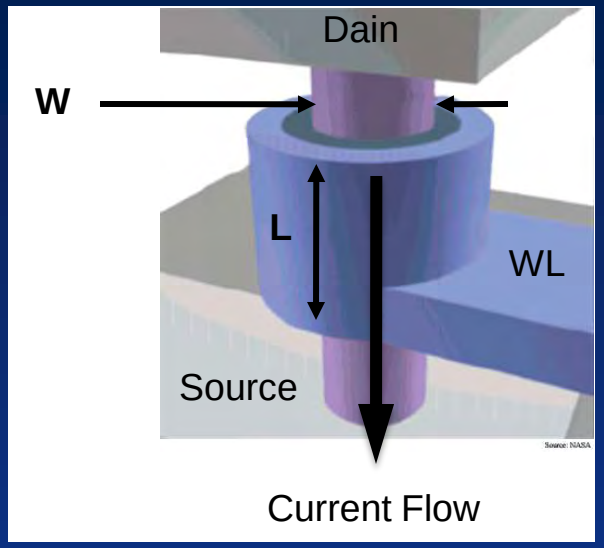


High Density Vertical Flash

Memory Cell Structure

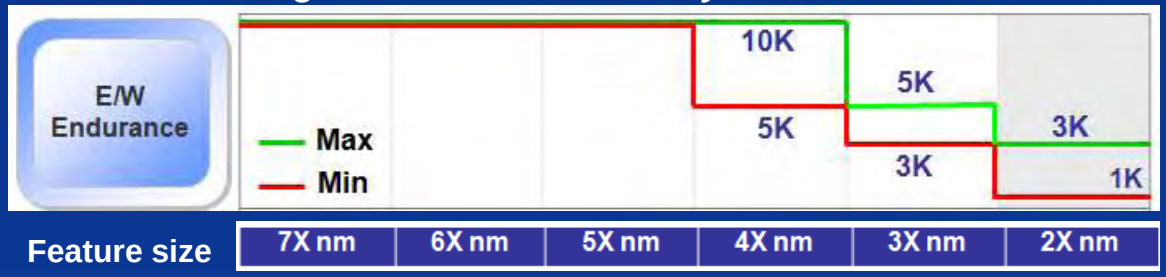


Vertical Transistor



- Channel length is independent to litho
- Low standby leakage current
- Large driving current
- Low SER (Soft Error Rate)
- **Better E/W for non-volatile memory**

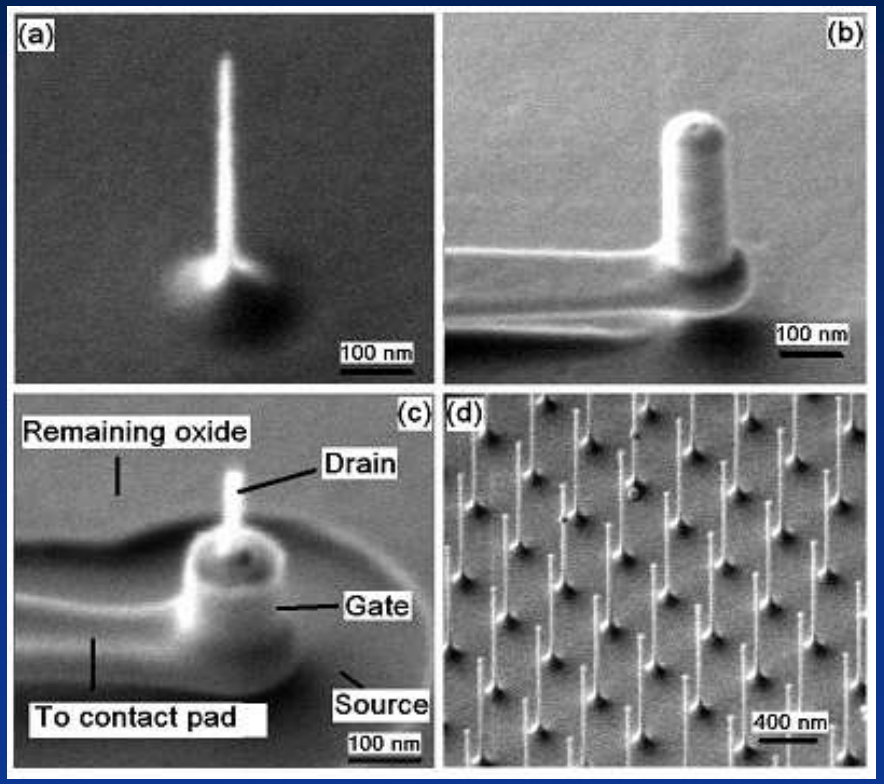
Degradation of Reliability of Flash Cell



Source: Hynix

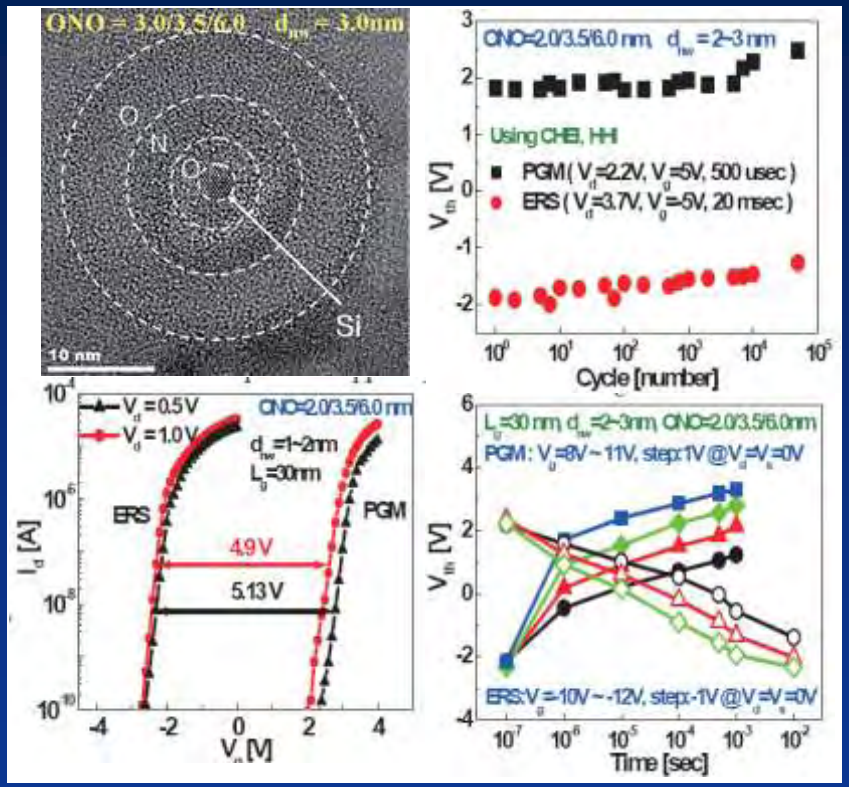
How Small Silicon Pillar Can Be?

It will work down to 3 nm.



Source: IME

20 nm silicon vertical transistor



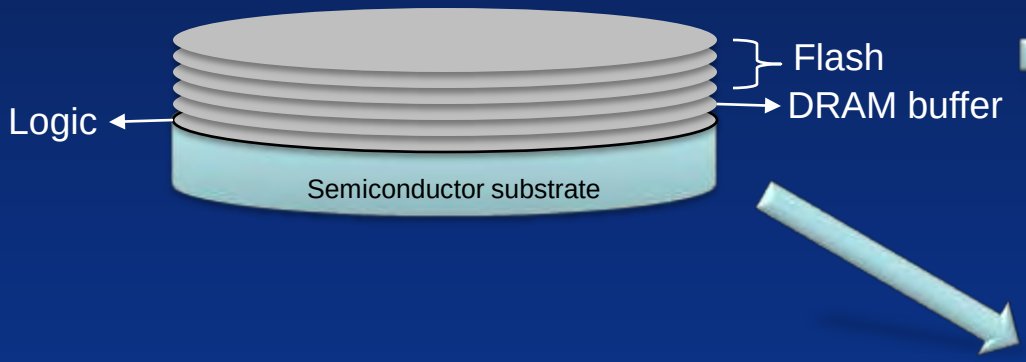
Source: Samsung

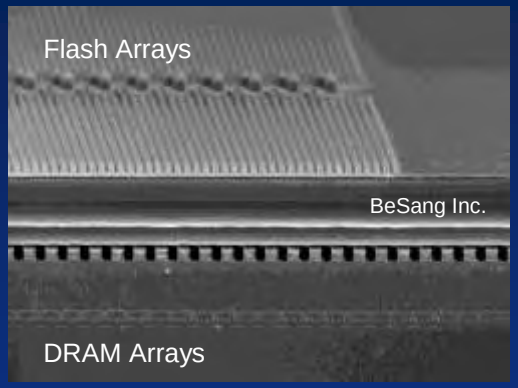
3 nm silicon nano-wire flash memory

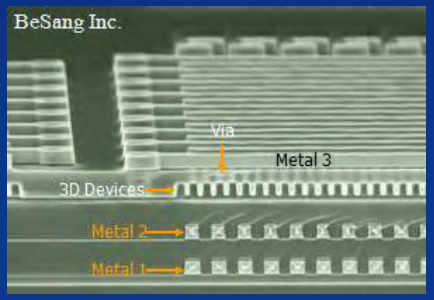
SSD-in-a-Chip Structure

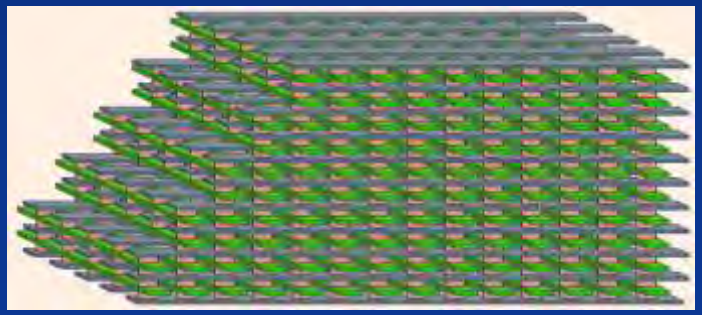
0.1 F²

Effective Cell Size
with 5-Layer Stacking

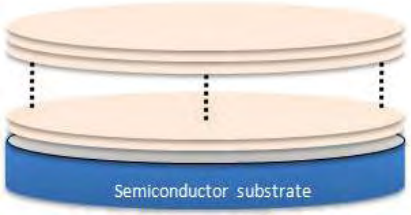








3D IC vs. Cross-Point Memories

	3D IC	Cross-Point Memories
Memory Stacking Density	 **5**-Layer Stacking	equivalent  **40**-Layer Stacking
# of mask per bit	< 1	3
Material	Single-Crystalline Silicon	Emerging Materials
Multi-bit per cell	YES	NO ?

Summary

- Single-crystalline silicon
  - Most reliable, manufacturable, multi-bit per cell enabled
- Vertical flash with multi-bit per cell
- Multi-layer stacking 3D IC
  - SSD control logic + High speed buffer + High density flash
- Ultra low cost SSD-in-a-Chip