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Spansion Inc.

Breaking Down the Barriers:

Bringing Disruptive Memory Technology to Market

FLASH FORWARD

SPANSION

How Radical Should Changes Be?

Disruptive

Interrupt the normal course of Technology

Evolutionary.

Continue to change from a lower to a higher, more complex, or better state of Technology

How Disruptive can Technology be?

- **New Applications, New Infrastructure and New Market**

OR

- **Improve the existing applications**
- **More applications without creating a new infrastructure**

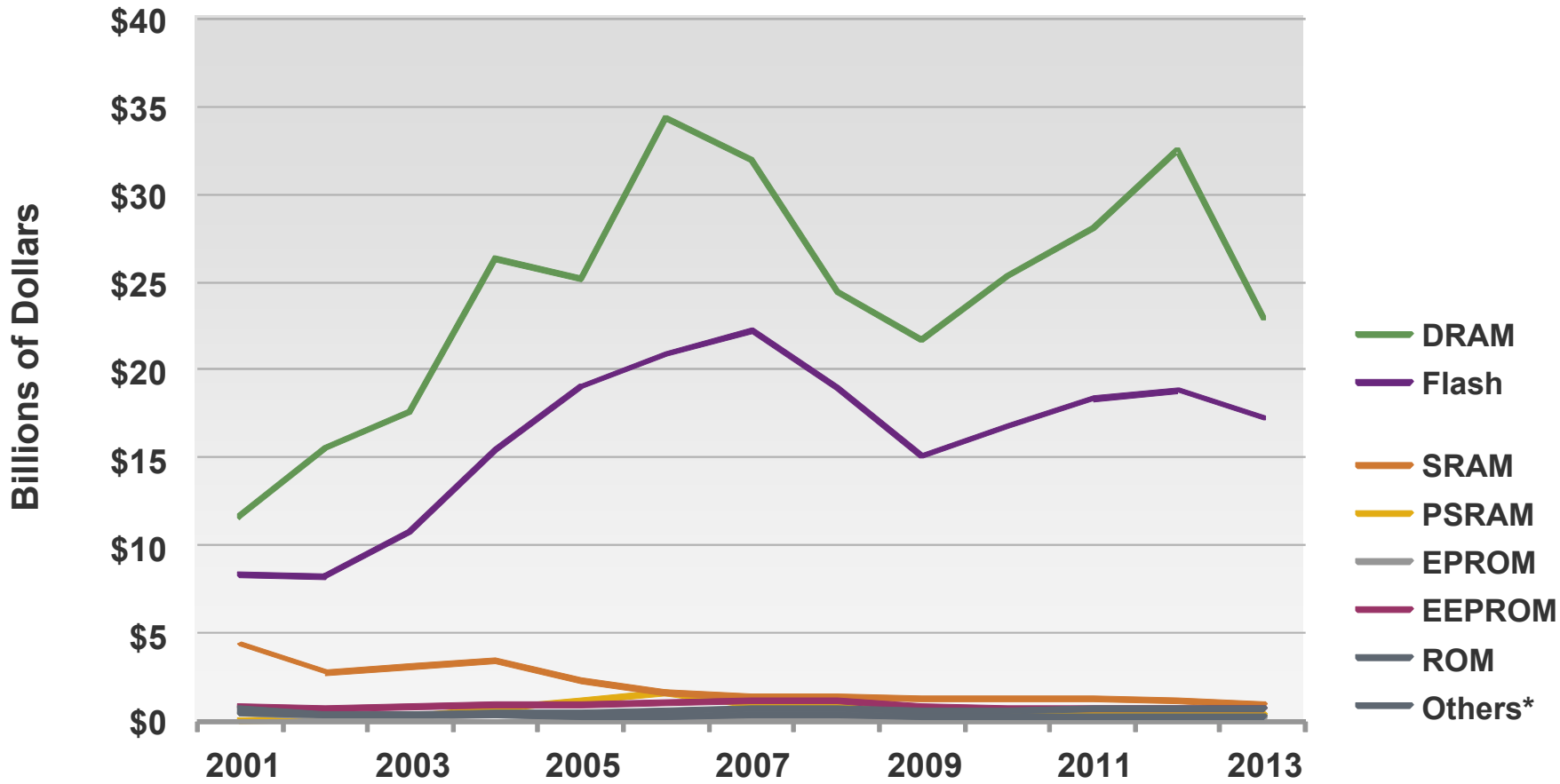
How Disruptive Technology can be effective?

"In spite of the rare instances when disruptive technology has been successfully deployed in the memory industry, we operate under the assumption that it can and should be, without fully examining how to do it or even if we should."

Spansion as one of the few companies that has successfully deployed a disruptive technology in the memory market.

Polarized Mainstream Memory Use

Defines infrastructure and ecosystem

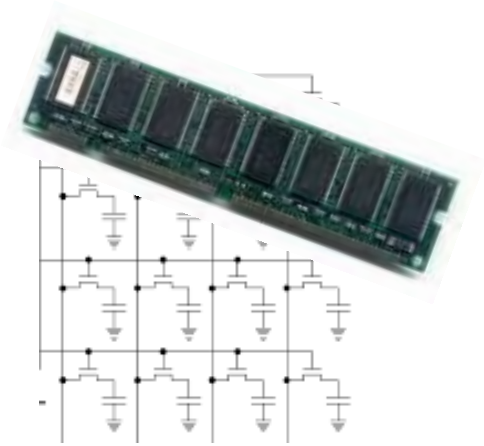


Source: Gartner (February 2009)

* Excludes memory embedded in ASIC or ASSP components.

Memory Attributes

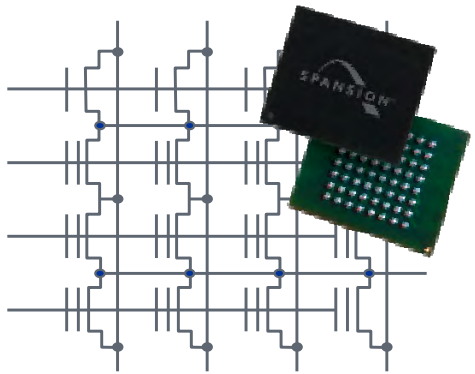
Keep discrete or combine in one technology?



DRAM

Volatile + Refresh
Most expensive
Very fast read & write

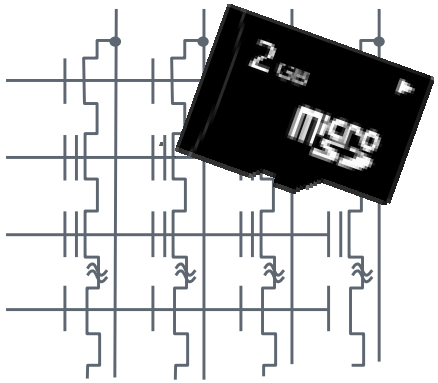
Best for
Real time code
execution cache



NOR

Non-volatile
Low cost
Fast read
High reliability

Best for
code storage and
execution



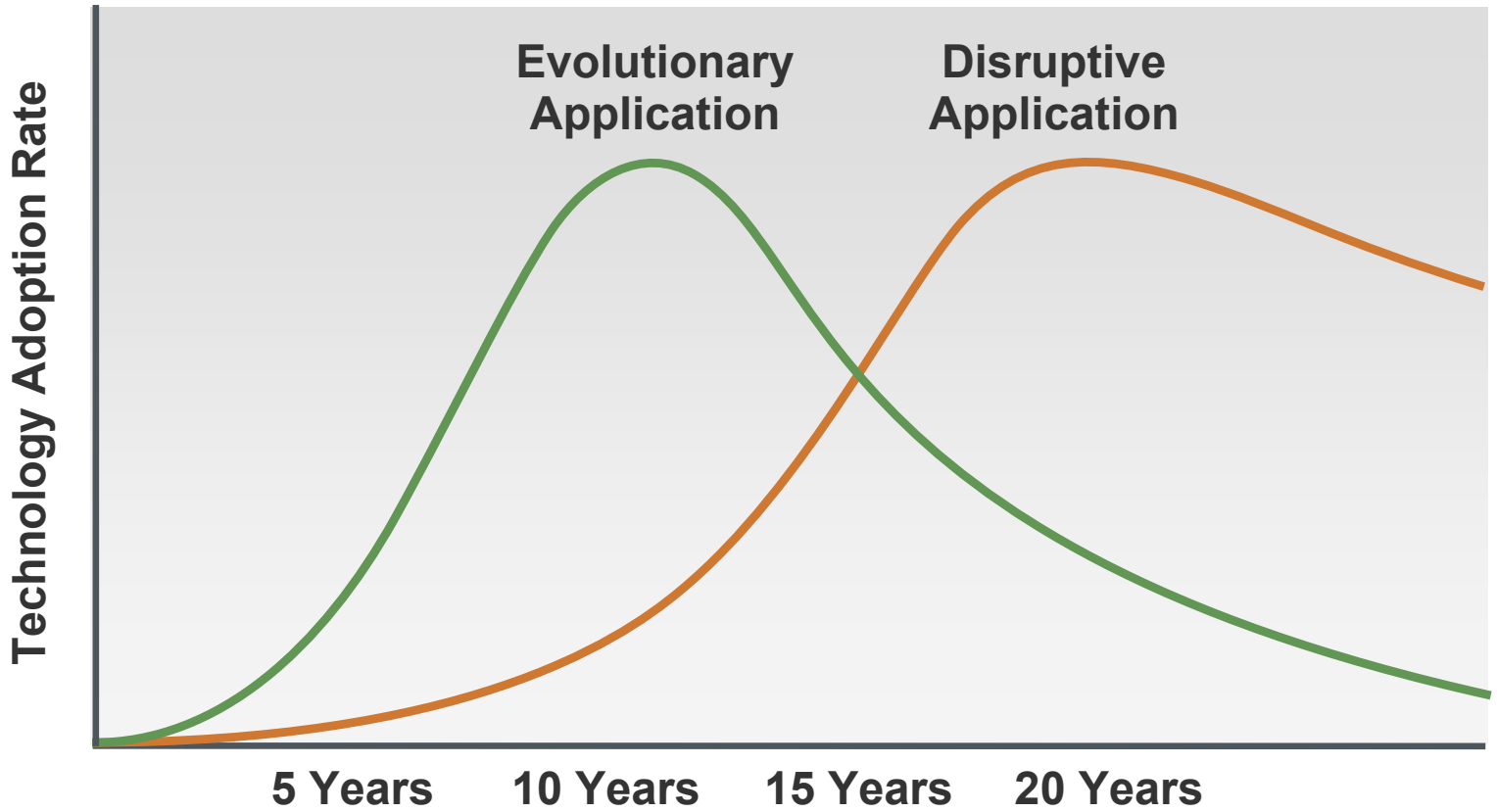
NAND

Non-volatile
Lowest cost
Fast write & erase

Best for
media
storage

Does Disruptive Technology = Disruptive Use?

Sometimes … but then it takes much longer to ramp



Source: Spansion

Next-Generation Memory Specification

Table stakes to deliver “acceptable” system benefits

- Competitive cost
- Compatible with high-volume manufacturing techniques
- Architecture balance
  - Performance
    - High speed read
    - High speed program, erase/overwrite
  - Low power
- Reliability
  - Data retention
  - Endurance

“Acceptable” defined by the infrastructure

- What is required from the memory device
- What can be exploited by the system software and hardware

Technology & Infrastructure Maturity

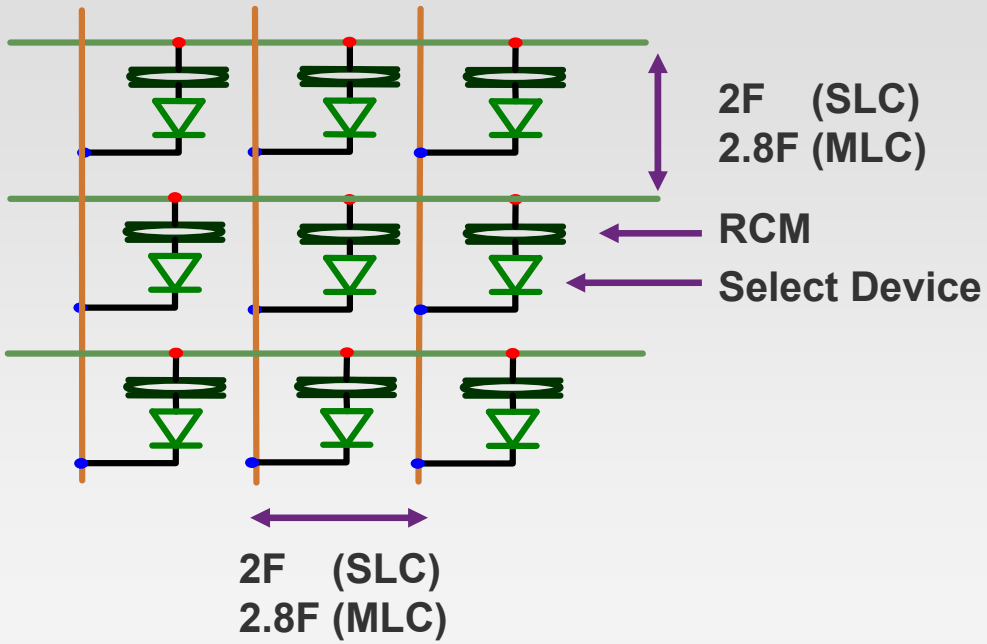
	Mature	Evolving	Disruptive (Near Term)	Disruptive (Long Term)
Technology	Floating Gate	Charge Trapping (e.g. MirrorBit®)	PCM	Other RCM RRAM MRAM
Mass Market Maturity	20 years	7 years	Years Away	Many Years Away

Source: Spansion

Resistive Change Memory

Near term or long term technology solution?

The Ideal RCM Technology



1. 4-5F^2 MLC cell
2. Compact select device with sufficient drive current, e.g. vertical diode
3. Minimum pitch, fine-line, high conductivity interconnect in both directions

Near Term: Phase Change Memory

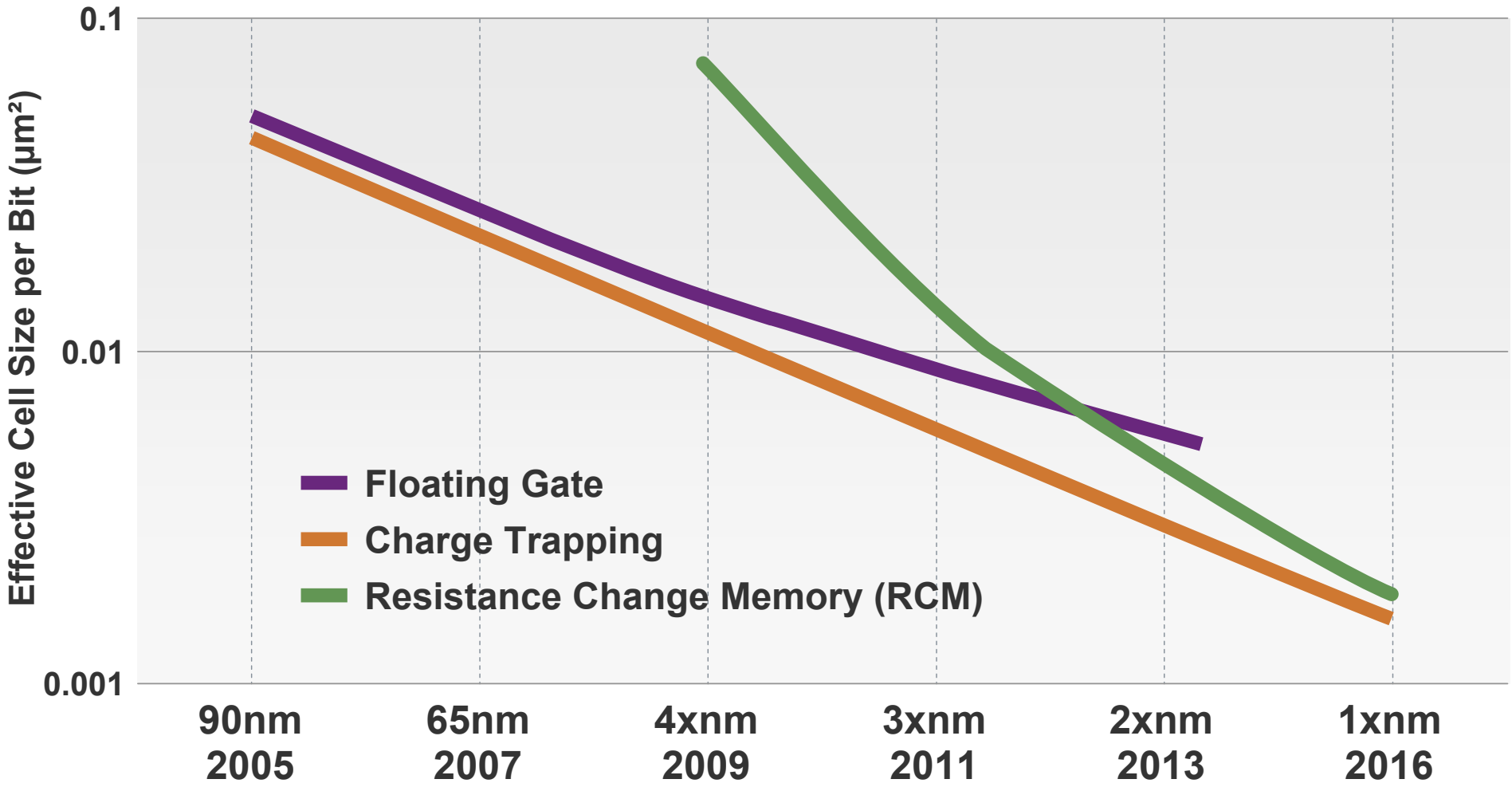
Challenges the industry has to overcome

	Issue	Risk	Comments
1	**Performance:** Programming speed	High	High current limits parallelism in programming
2	**Manufacturability:** Process complexity	High	Challenging integration with significant number of critical masking steps
3	**Cost and Manu:** Multi-level capability	High	Resistance drift challenges state placement
4	**Cost** Complexity vs. existing technology	High	SLC significantly more complex process
5	**Cost** Cell size	High	Compromises for shrink from $12F^2$
6	**Cost and Manu.** Scalability	High	Select devices may not scale. GST area is already sub-lithographic
7	Bit alterability	Low	Truly disruptive for NVM

Source: Spansion

Charge Trapping: Innovation at the Cell – Evolution in the System

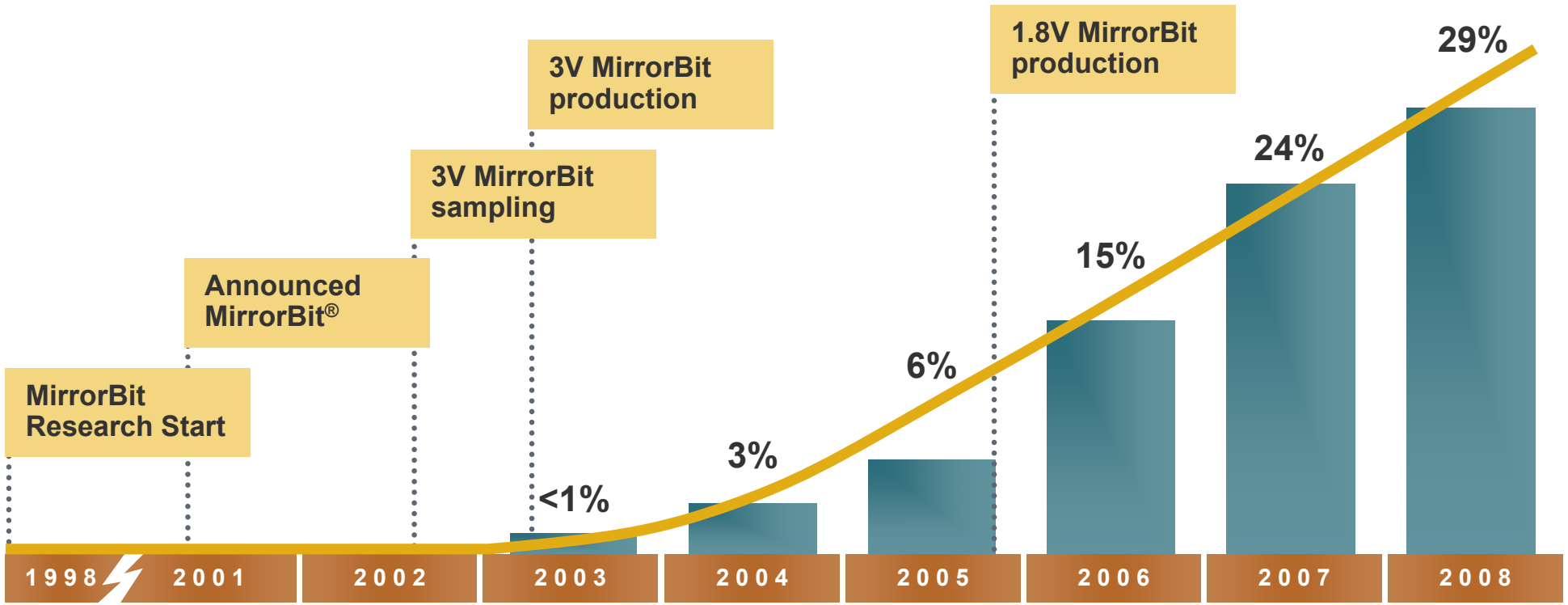
Disruptive Scalability



Source: Spansion estimates

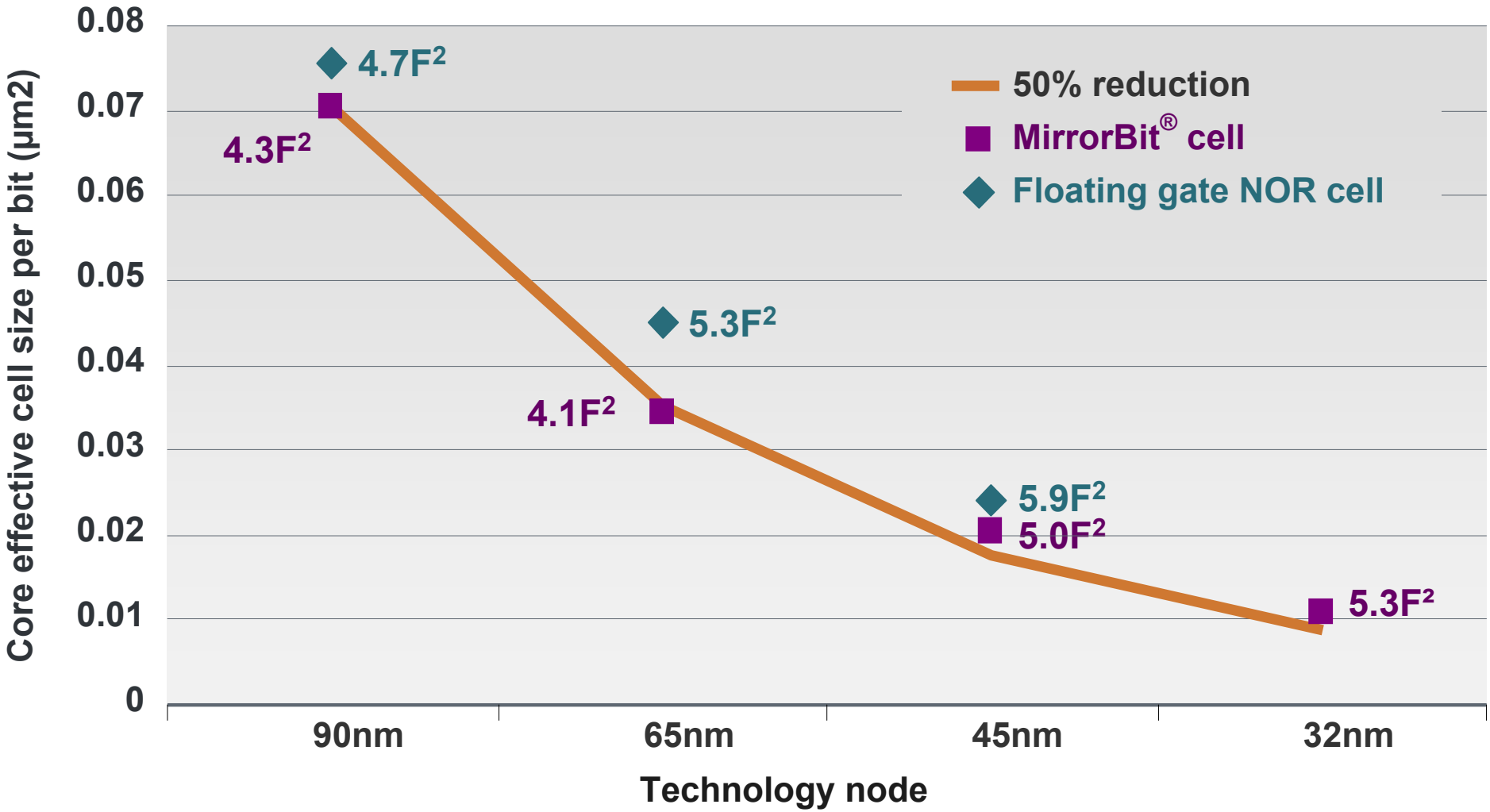
Evolutionary Ramp

New technology must be “acceptable” for the customer



Source: Spansion

NOR Cell Size Scaling Example



Source: Spansion estimates

What It Takes to Make "It" Work!

- **Intimate Technology, Design, Product Eng, Test Collaboration**
  - New & old technology aren't the same – Different mindset required
  - What works in the lab doesn't necessarily work in production

- **Specific MirrorBit® technology design innovations**

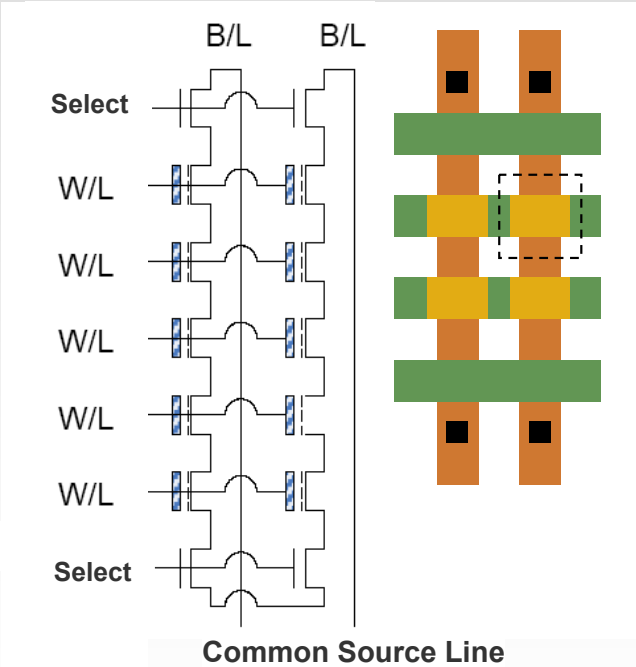
Advanced Program and Erase Algorithms	• Temperature and cell location compensation • Compact, uniform cell distributions	• Stabilizes cell behavior • Optimizes data retention
Advanced Read	• Increases margin by reducing parasitic currents • Opens up sensing window	
Advanced Process	• Creating the highest technique in process	

Charge Trapping Next Steps with MirrorBit® NAND Technology

“Evolution of Technology”

The Technology

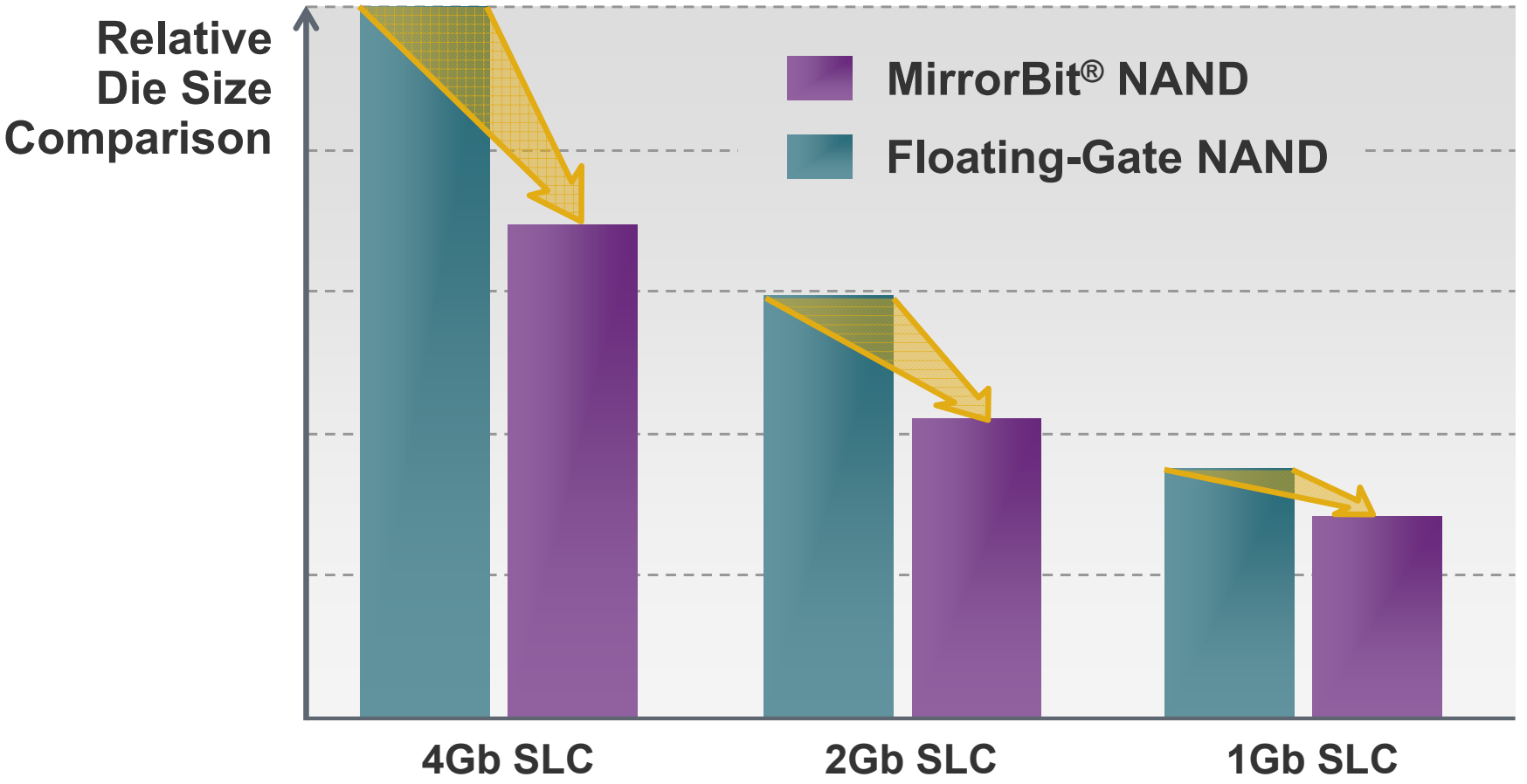
MirrorBit® NAND Technology



Cell Size ~ $4.0\lambda^2$

- SONOS-like cell structure
- Cells connected in NAND array
- Highly scalable
- SLC and MLC capable
- Leverages proprietary MirrorBit® charge trapping technology and manufacturing know-how
- Different technology but excellent process compatibility with MirrorBit NOR for production in same fabs

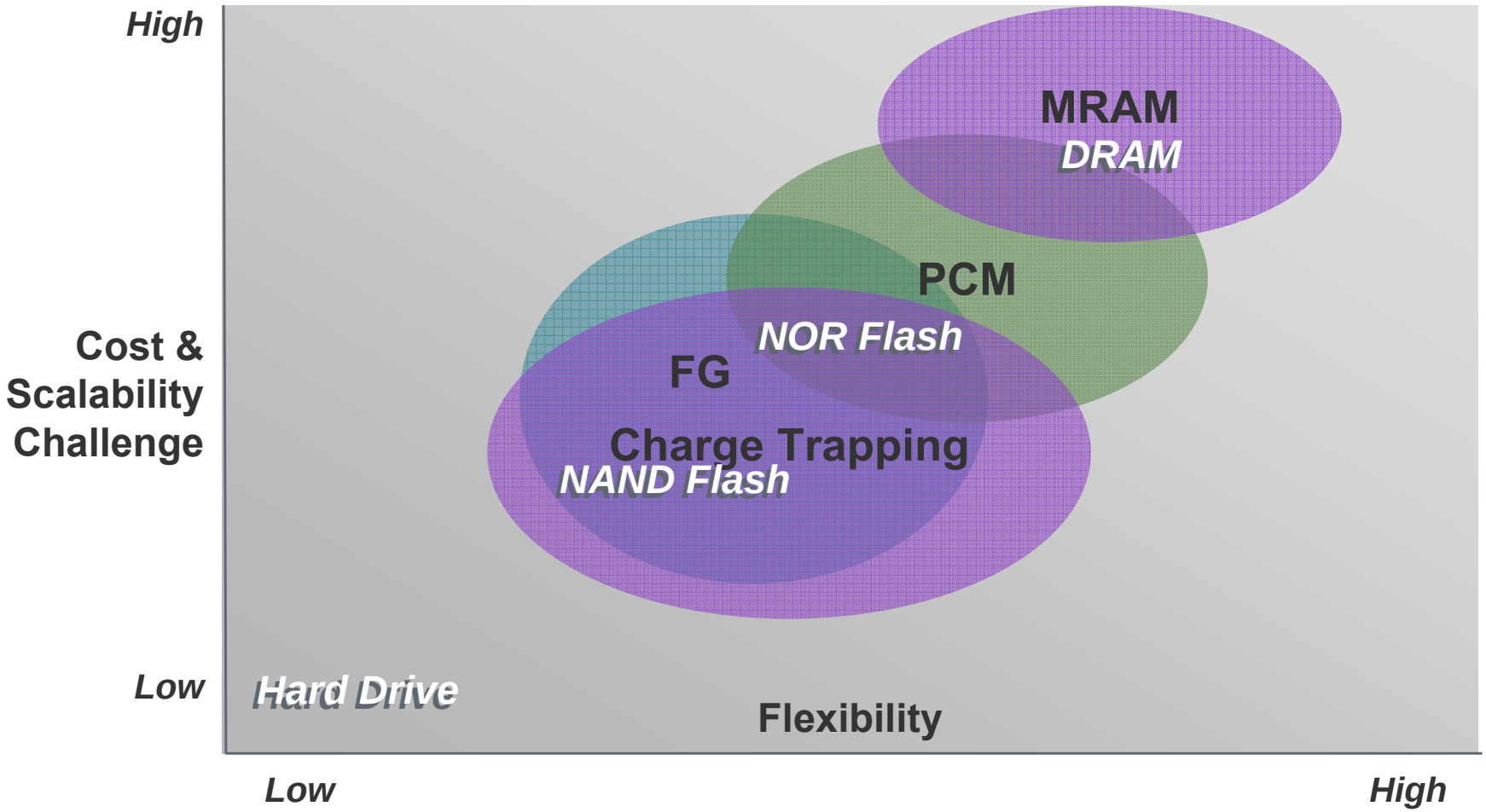
Efficient Die Size



* Source: Spansion estimates of MirrorBit® NAND versus 4xnm Floating gate SLC NAND solutions

What Will the Future Look Like?

Moving closer to the ideal memory



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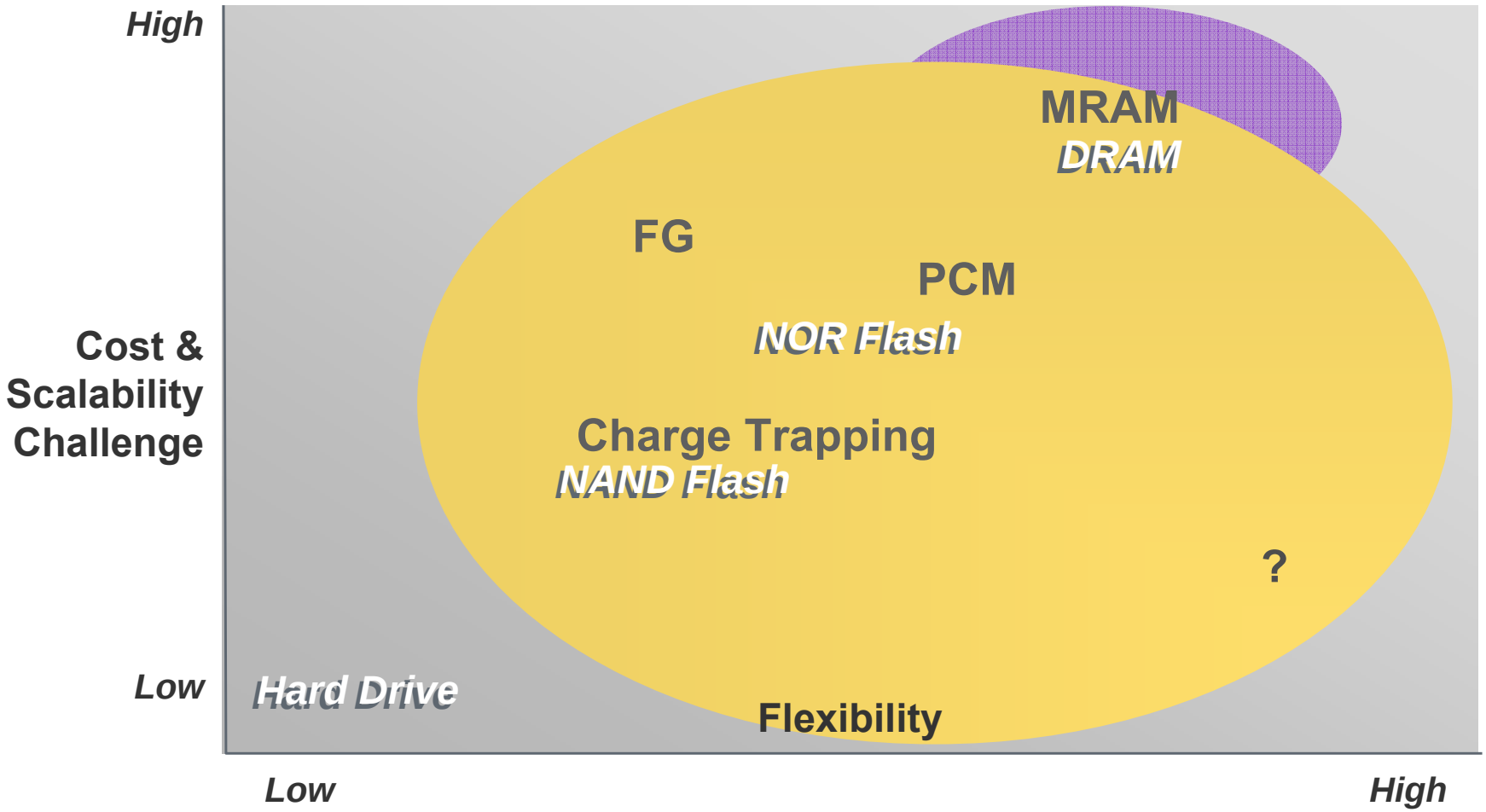

Source: Spansion

Conclusion

Existing industry is structured for evolution

- Even in Silicon Valley!
- Disruption can be risky – for both customers and suppliers
- It takes a long time to create new Infrastructure in a new Eco-System

New technology is never adopted quickly

- Memory doesn't exist in a vacuum
- Even evolution takes a while
- Disruption needs H/W and S/W infrastructure to change

Tomorrow's technologies…

- Must be relevant and must be viable
- Must offer more than today's technology … otherwise why change?


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