Power Requirements for Multi-Bit Per Cell NAND Flash

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Agenda

- Technology differences in SLC, MLC-2, MLC-3, and MLC-4
- Power consumption considerations
- Summary

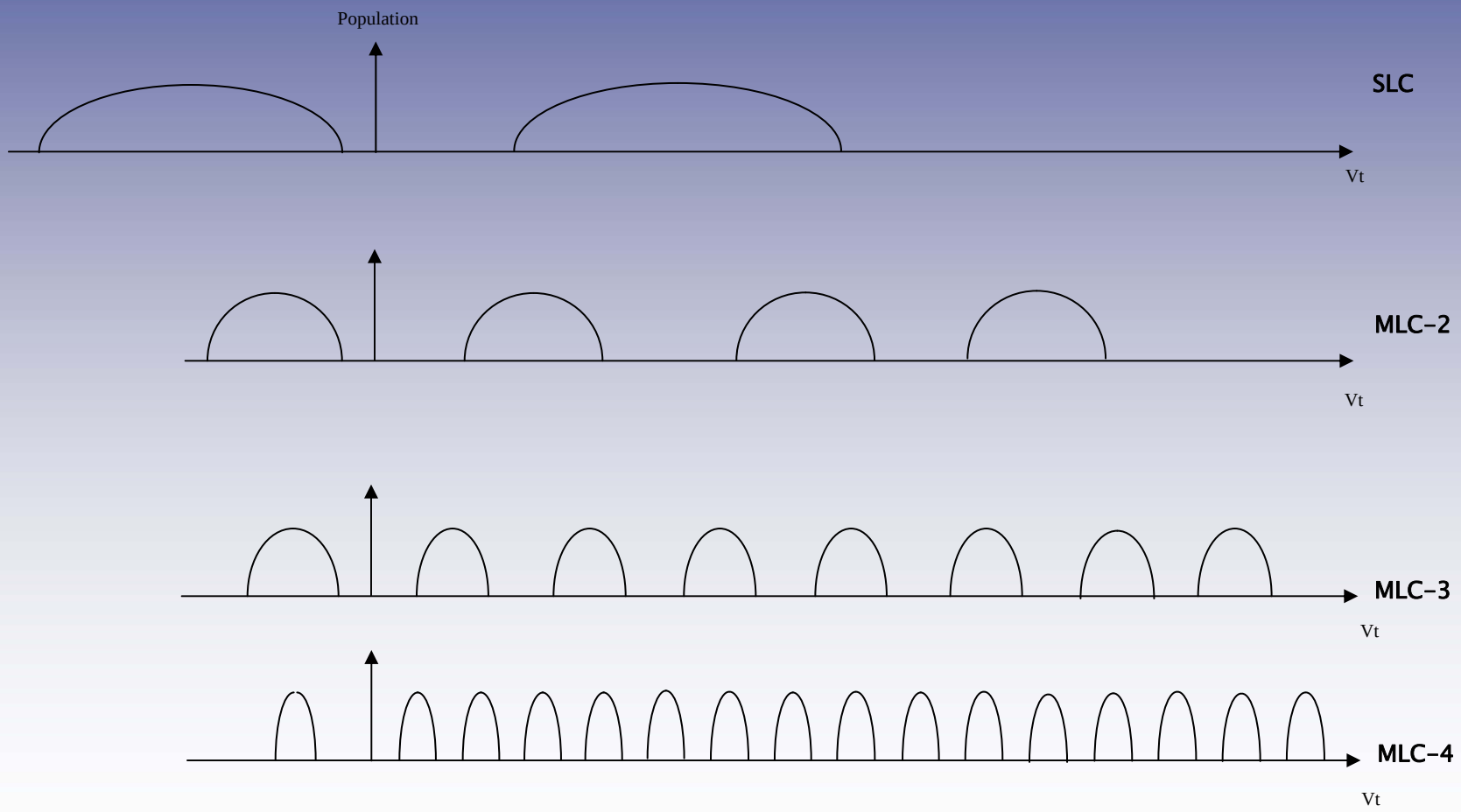
Technology Differences

- SLC
  - Single-level cell
  - One bit per cell
- MLC
  - Multi-level cell
  - Two bits per cell (MLC-2)
  - Three bits per cell (MLC-3)
  - Four bits per cell (MLC-4)
- Endurance
  - SLC typically 10–20 times better than MLC-2
  - MLC-2 is much better than MLC-3 and MLC-4

Technology Differences

- Performance
  - Significantly better performance with fewer bits per cell
- Price
  - SLC-based products greater than 2X the $/GB over MLC-2
  - Some cost advantages with more bits per cell

NAND Flash Cell Vt distributions



Power Consumption Considerations

- Chip reduction for equal density
- Controller power considerations
- Higher program voltage
- Array operation
- Standby power

Chip Reduction for Equal Density Applications

- True that the same number of bits uses less space on silicon
- Does not necessarily result in fewer chips per system
  - Would require half densities for MLC-3
  - Yet to be seen for MLC-4
- Smaller die does mean possible lower bitline and tub capacitance, which should result in lower power consumption during precharge

Controller Power Consumption Considerations

- Tradeoffs in latency/bandwidth vs. power consumption
- Even if assume double number of gates, this amount will be minimal in relation to overall NAND read energy consumption

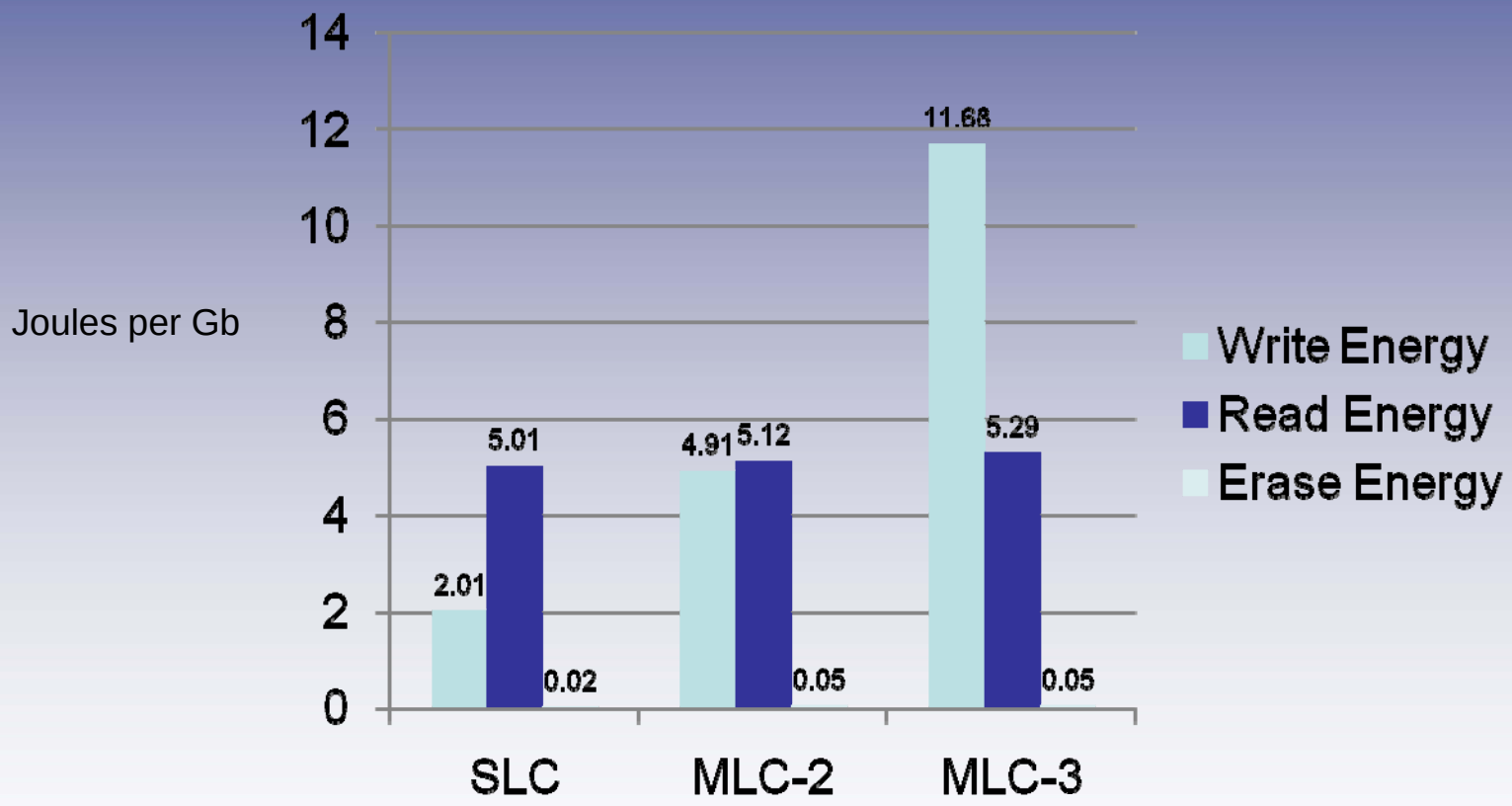
Higher Program Voltage

- Higher wordline voltage required does not significantly contribute to overall program current draw
- Capacitance of wordline is dwarfed by capacitance of bitlines

Longer Array Operation Times

- Much longer array operations will cause increased energy usage
- Similar peak and average power will be drawn during the array operations, but for a longer period due to requirement for finer Vt placement
- In system, performance vs. power consumption tradeoffs exist

Comparing Raw NAND



Standby Power Considerations

- Only active energy will be different for multi-bit per cell technology
- Standby power consumption will be the same

Summary

- MLC-3 and MLC-4 NAND Flash power consumption will be increased primarily due to the longer program times required
- System design will require decisions for tradeoff on power consumption vs. performance