MMI:
A General Narrow Interface for Memory Devices

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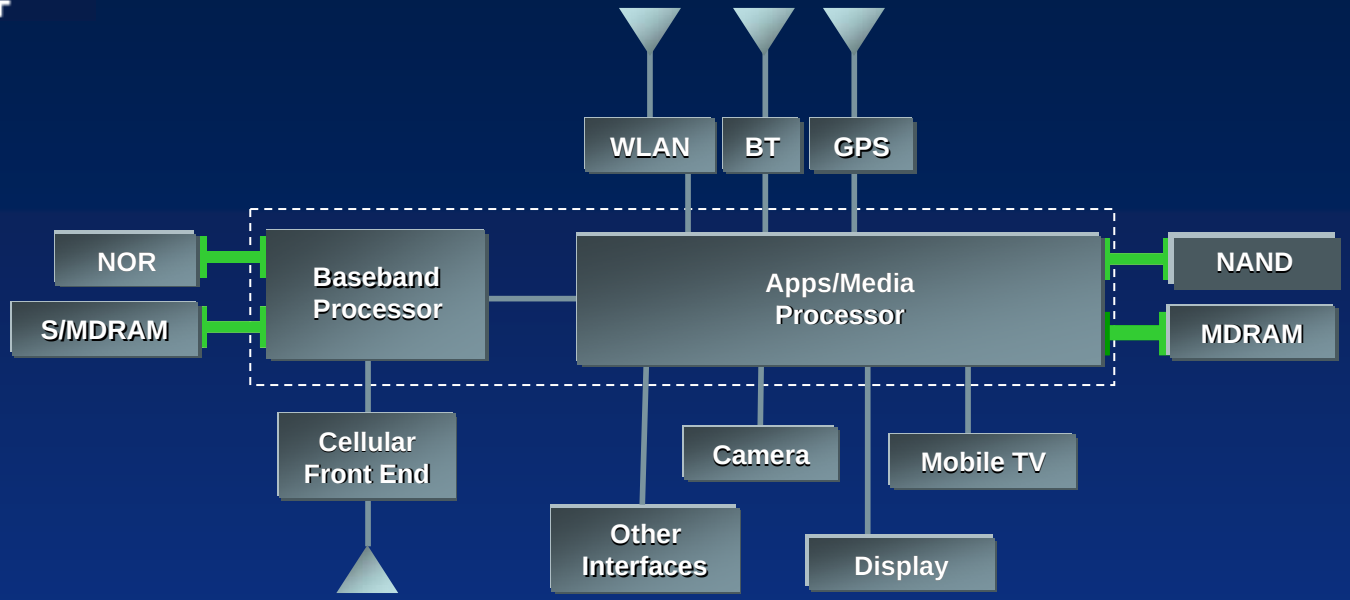
What is MMI?



- The Rambus Mobile Memory Initiative is focused on *high-bandwidth, low-power* memory interface technologies for next-generation mobile memory systems
- It is a highly scalable, narrow bus processor-to-memory interface solution with best-in-class power-performance
  - Designed for the handset architecture
  - It eases the challenges of having to support a growing diversity of IO's
- It provides a lower risk path to easier integration and cost
  - Reduces pin count to avoid pad limitation and reduce cost
  - Provides a path to flexible packaging
- In Feb, test silicon demonstrated 4.3Gbps per link with low power and fast power mode transitions

Future-proof your mobile memory roadmap with MMI

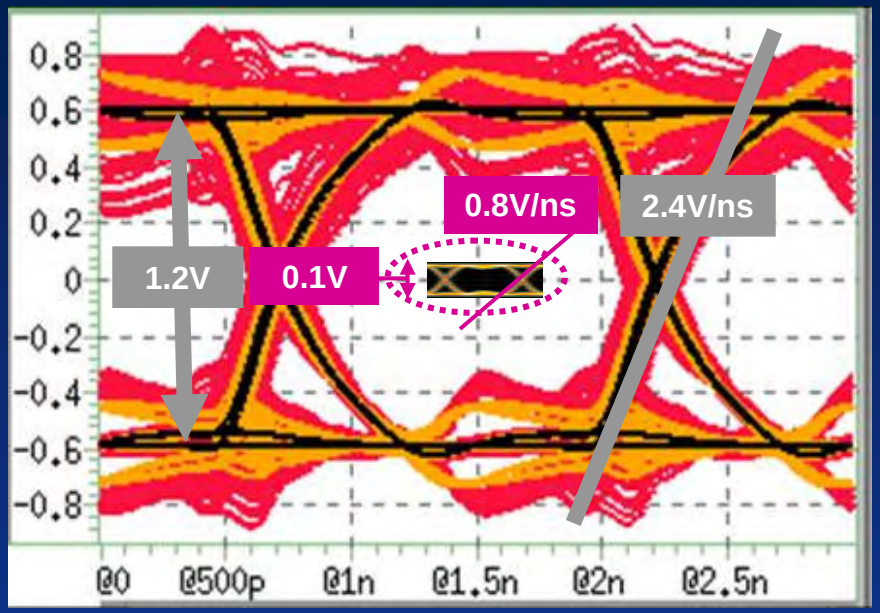
MMI is an ideal follow-on interface to LPDDR2

- **60% less pin count at equivalent device BW**
- **Scalable interface across DRAM, NOR, and NAND devices**
- **67% less interconnect power at equivalent device BW**

MMI Interface Link Innovations

LPDDR2

MMI



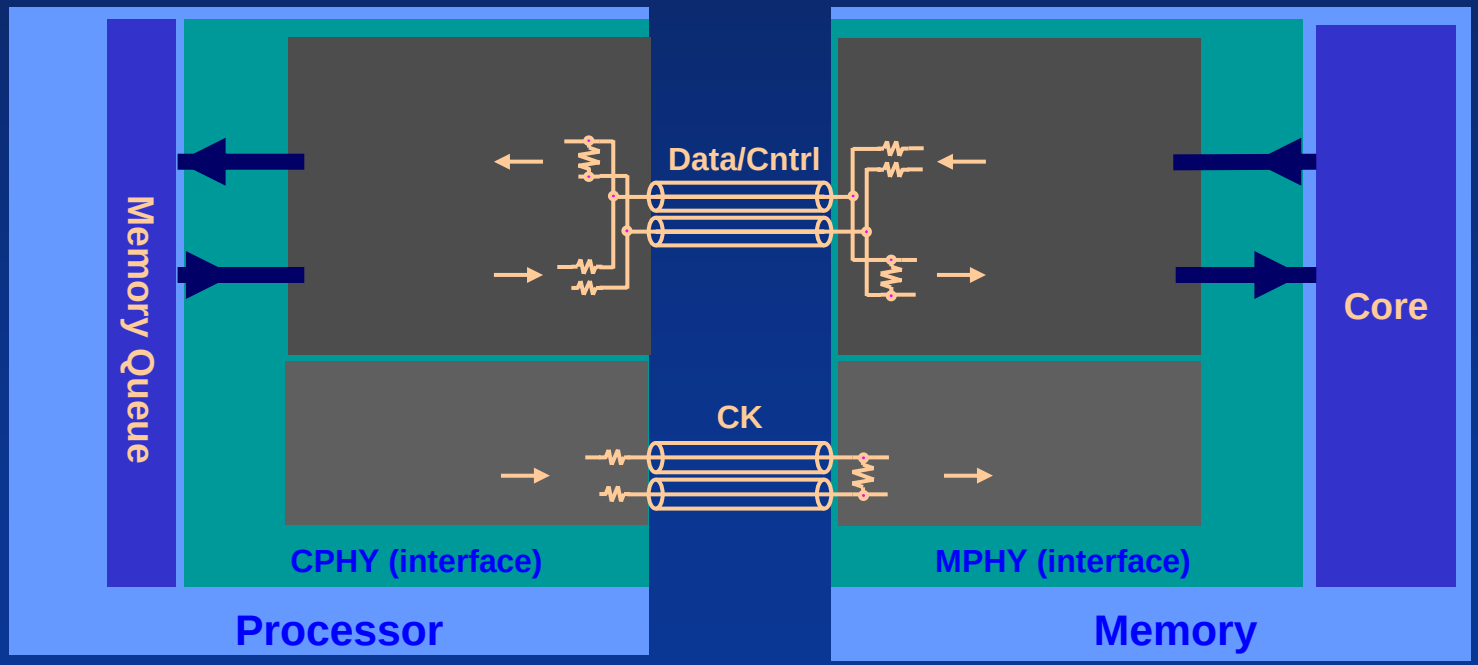
Higher BW and Lower Power are achieved by minimizing the effects of ISI, Crosstalk, EMI, SSO, High-Z Power Distribution Networks and Vref distribution with:

- **Bidirectional, very low voltage swing differential signaling**
- **Series-source termination (transmitter)**
- **Differential termination (receiver)**
- **Low C_i**

Processor and Memory Technologies are Asymmetric

- Faster transistors
- Lower Vth
- Higher leakage
- Lower Vdd
- Many metal layers

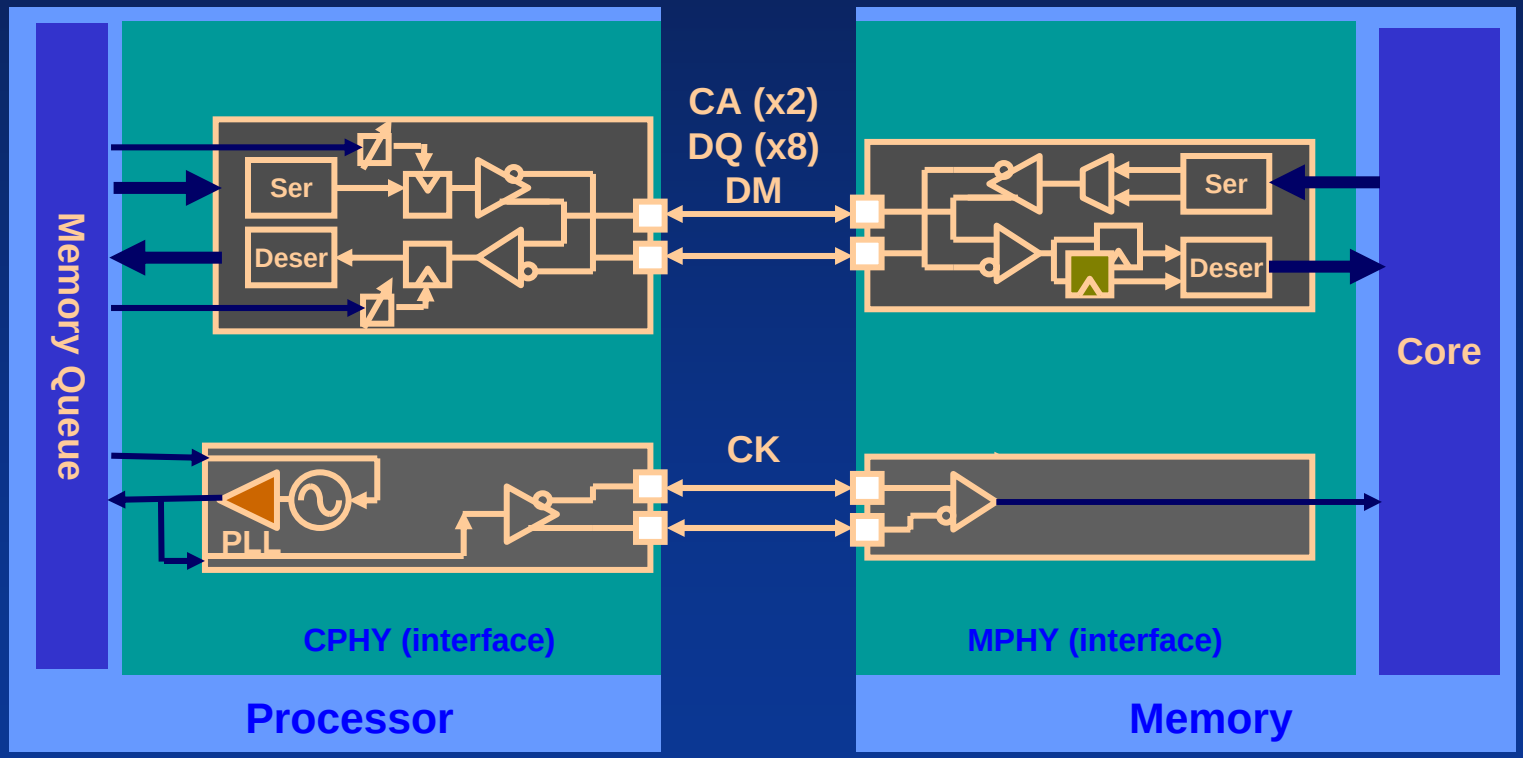
- Slower transistors
- Higher Vth
- Lower leakage
- Higher Vdd
- Fewer metal layers



MMI Optimizes Cost, Complexity, Power-Performance With An Asymmetric Architecture

All Tx and Rx timing control is performed on the ASIC side

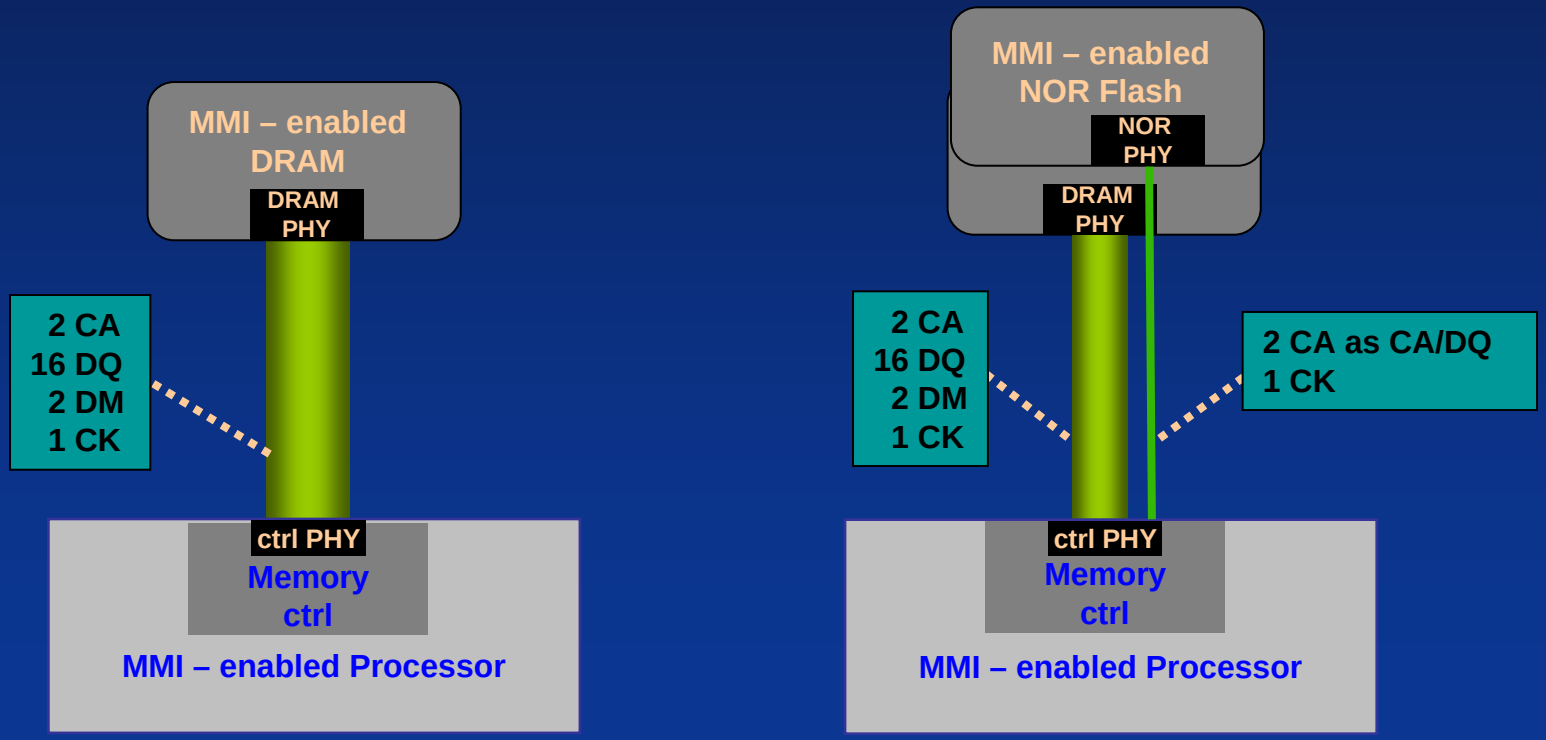
DRAM or Flash side is kept simple – no timing control



System Configuration Options: DRAM + A Single Flash Device

Option 1
1 x16 DRAM
~6400MB/s DRAM BW

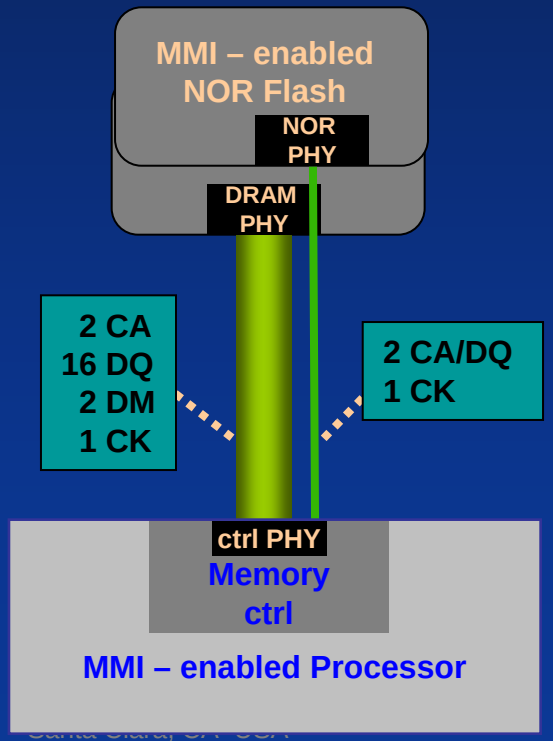
Option 2
~6400MB/s DRAM BW
~700MB/s NOR/NAND Flash BW



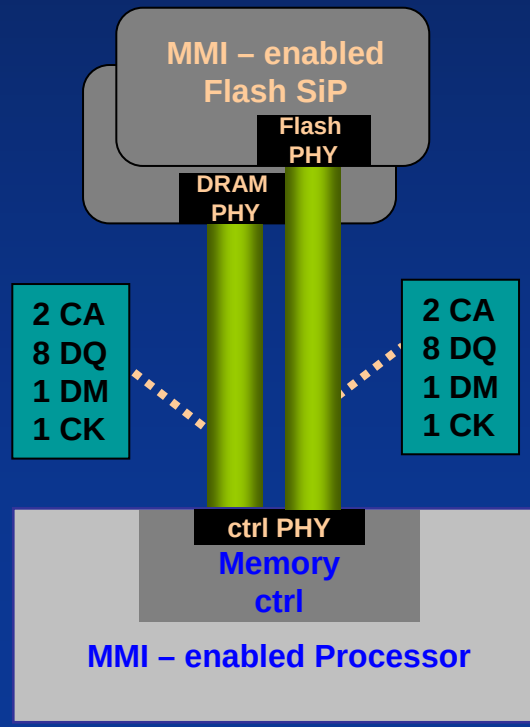
* x16 PHY Includes 3 redundant links (2 CA and 1 CK) that are available to support a second DRAM or additional Flash devices

System Configuration Options: DRAM + NOR/NAND Flash Package

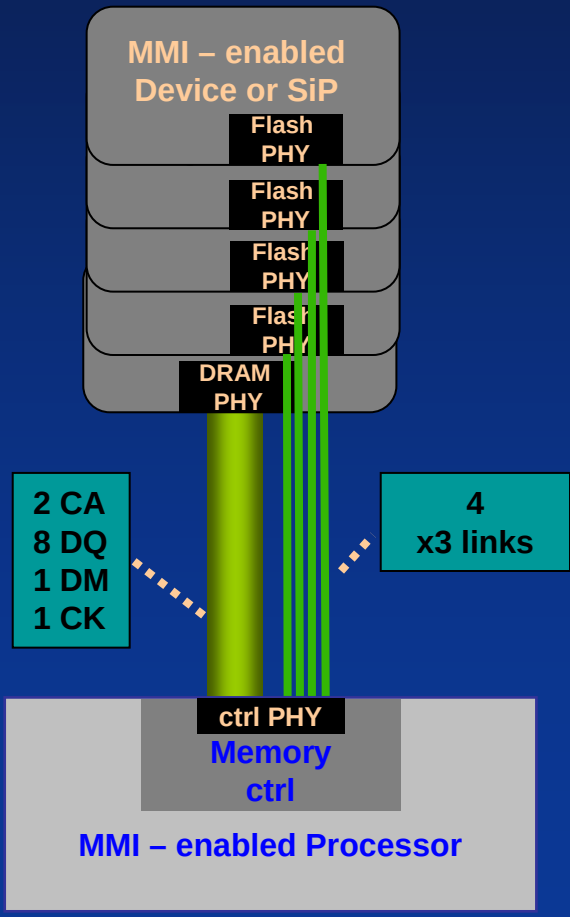
Option 1
~700MB/s Flash BW
~6400MB/s DRAM BW



Option 2
~3200MB/s Flash BW
~3200MB/s DRAM BW

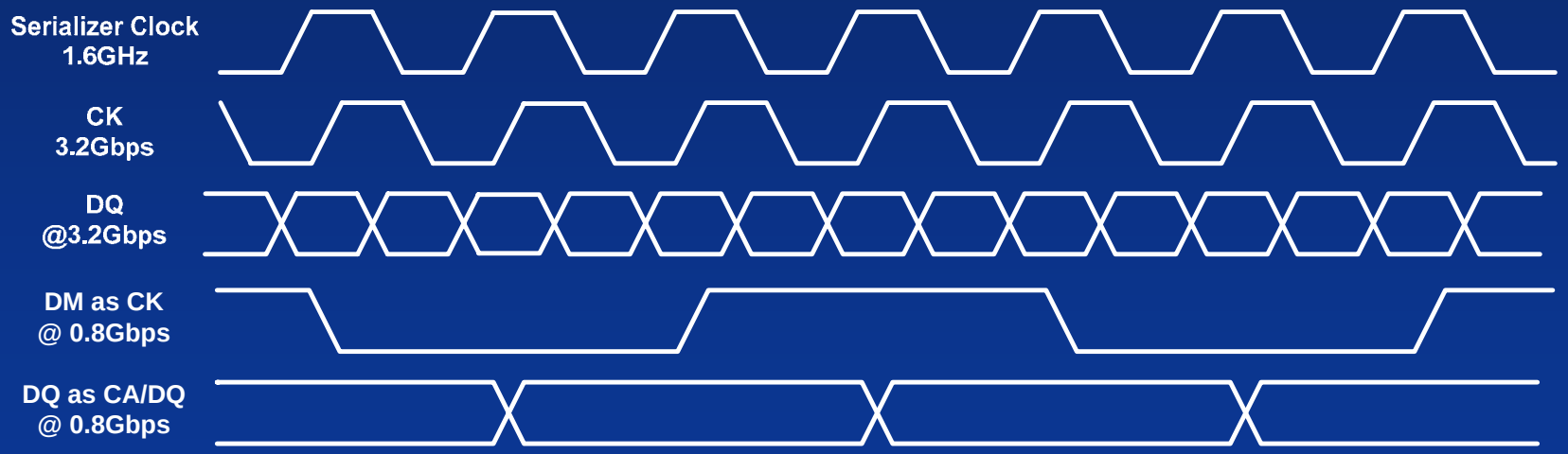


Option 3
~2800MB/s Flash BW
~3200MB/s DRAM BW



MMI Matches Native Device Core and Interface BW

- **MMI's asymmetric timing easily operates with Low Core BW or Low Interface Speed Memory Devices**
- **SDR, ½DR, ¼DR, etc. Clock and Data streams are created by bit replication at the controller PHY serializer interface**



High Level Summary

- **Growing number of different IO's, processors reaching pad limitations, lack of BW scalability, higher active power, package design & SI challenges all hinder current roadmap**

- **MMI is ideally suited to extend the mobile memory roadmap**
  - **Scalable general memory interface for all memory devices in the handset**
  - **Fewer pins: 60% less pins than equivalent LPDDR2 solution**
  - **High Bandwidth: 88MB/s-12.8GB/s per Memory**
  - **Low Power: 67% less active power than equivalent LPDDR2 solution**
  - **Reduced board complexity with much easier PoP design**
  - **Lower cost and lower risk solution than other alternatives**

- **MMI can support NOR and NAND Flash with no change to the controller PHY design or pin out**
  - **MMI can provide high scalable peak Flash BW: 88MB/s to 3.2+GB/s**
  - **MMI can support lower Flash Device BW at better power efficiency through clock synthesis**
  - **MMI can support high Flash capacity: 1 – 4 devices or controllers**