



Modifying a DRAM controller to support LPDDR2-NVM

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Agenda

- What is LPDDR2?
- Why is a DRAM controller a good starting point for LPDDR2-NVM?
- What are some major controller changes required to support LPDDR2-NVM?
- What system changes are necessary for NVM?
- Conclusion

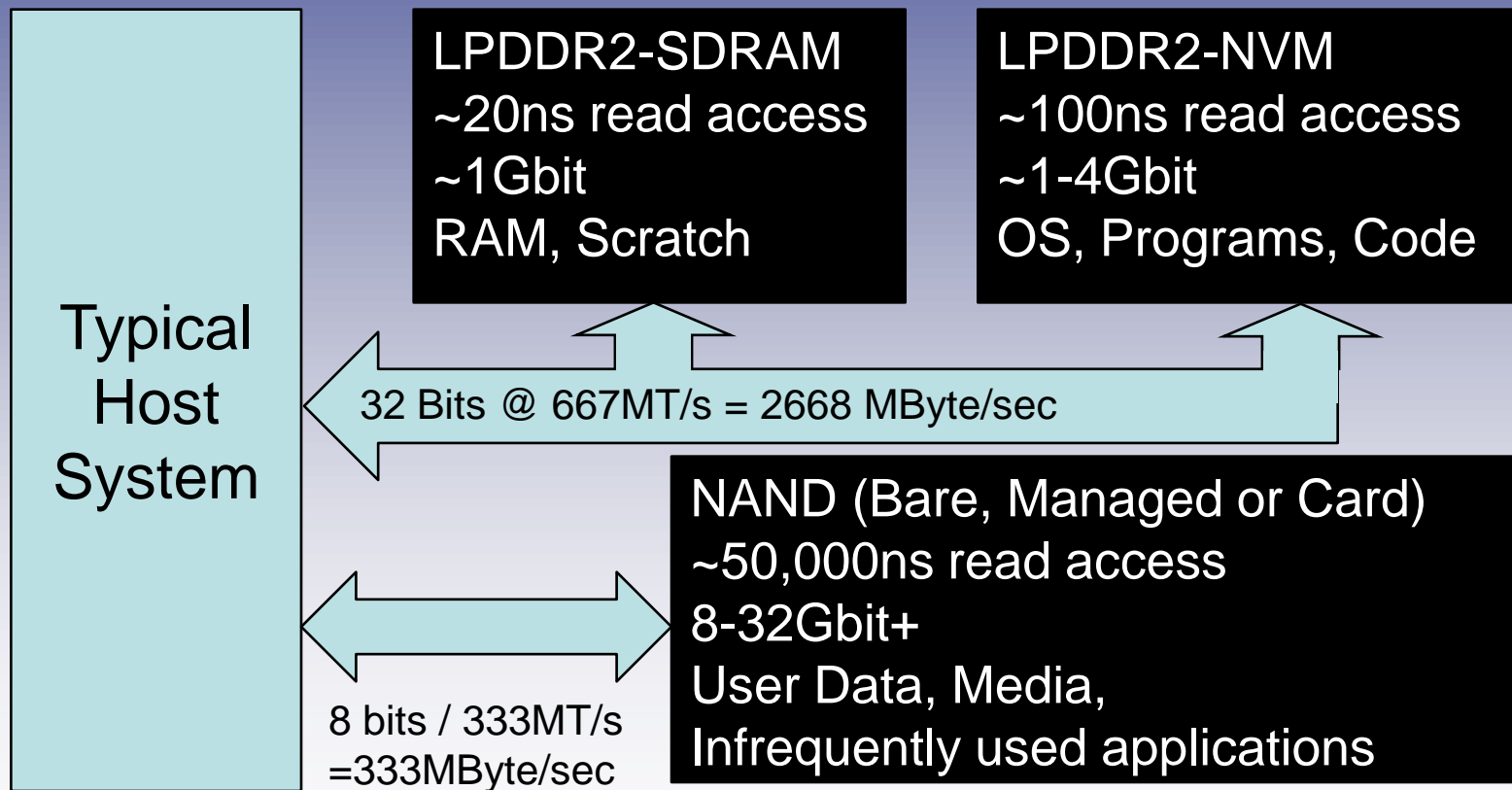
What is LPDDR2?

- JEDEC standard JESD209-2
- Replacement for:
 - LPDDR1-DRAM
 - Popular technology, however 6 years old
 - LPDDR1-NVM (NOR)
 - PSRAM + Bare NOR
- More speed, more density, less power, lower voltage (1.2v), fewer pins... AND...
- Sharing of DRAM and NVM on the same bus

What is LPDDR2-NVM?

- NVM = Non-Volatile Memory
- Intent: LPDDR2-NVM should support memory technologies that allow execute-in-place:
 - NOR Flash
 - Phase Change Memory (PCM)
- Several barriers exist which would make attachment of NAND Flash difficult
 - If the system requires NAND, use Bare NAND, managed NAND, flash cards, etc.

Using LPDDR2-NVM



LPDDR2 status



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JEDEC ARLI

standards development for the microelectronics industry, today announced the publication of JESD209-2 LPDDR2 Low Power Memory Device Standard. Available for **free download** from JEDEC's website at

Sampling	Yes	64Mb	x64	1.2V	POP	216-ball	333 MHz	LPDDR2-667	3ns	-40C to +85C
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Samsung Electronics and Numonyx join forces on Phase Change Memory

SEOUL and GENEVA, June 23, 2009 – Samsung Electronics Co., Ltd. and Numonyx B.V. today announced they are jointly developing market specifications for Phase Change Memory (PCM) and software compatibility – for mobile, embedded and other potential computing applications supporting the JEDEC LPDDR2 Low Power Memory Device Standard. The LPDDR2 standard offers advanced power management features, a shared interface for nonvolatile memory (NVM) and volatile memory (SDRAM), and a range of densities and speeds.

Why is a DRAM controller a good starting place for LPDDR2-NVM?

- LPDDR2-NVM was designed to be compatible with SDRAM
- Similar system assumptions
 - Read access (RAS) time within 1 order of magnitude
 - Random-ish access (not block access)
 - Buffered Writes
- Good DRAM memory controller design & architecture will yield good results for NVM

What are some major controller changes required to support LPDDR2-NVM?

- Supporting heterogeneous memories
 - Different size and organization
 - Some different timing parameters
- NVM Boot Mode
- Mode Register Read Capability
- 3-phase addressing
 - Addition of “Preactivate” command
- Row Buffer Allocation Mechanism
- Few changes to LPDDR2-DRAM PHY

LPDDR2 NVM Support – Architectural Decisions

- Command queue: separated or unified
 - Separated: must arbitrate for command access, extra care required for coherency
 - Unified: risk of NVM commands blocking DRAM commands
- Row Buffer allocation algorithm
- DNV Support
- Memory controller interaction with driver

What system changes are necessary for NVM?

- Usual Flash System Changes
 - Drivers
 - Writes only - No driver interaction expected for reads
 - Block oriented erase-before-write
 - Probably NOR only – probably not required for PCM
- Driver must manage NVM “Overlay Window”
- Boot
 - Need to figure out how to boot system from the NVM device using low-speed boot mode, then switching to operational speed

Conclusion

- LPDDR2-NVM was architected to be compatible with LPDDR2-NVM
- Good architectural design of an LPDDR2-DRAM controller will yield good results with LPDDR2-NVM
- Several changes are necessary
- Denali's Memory Controller and PHY for LPDDR2-NVM+ DDR2/LPDDR2 DRAM is in development for end 2009 delivery