# Storage SoC controller trends – Balancing performance and power

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# Agenda

- Application requirements
- Design tradeoffs
- Example architectures
- Architectural Selection Criteria

# Application Drivers

## Enterprise

- Green IT driving lower power
- Enterprise Reliability and Availability
- Security
- Application acceleration (SAP, Oracle, web Cache driving performance

## NoteBook and ePC

- Ruggedness, reliability and battery life requirements
- Business applications users driving performance and density
- Thermal challenges and battery life drive lower power requirements

## USB Flash Drives (UFD)

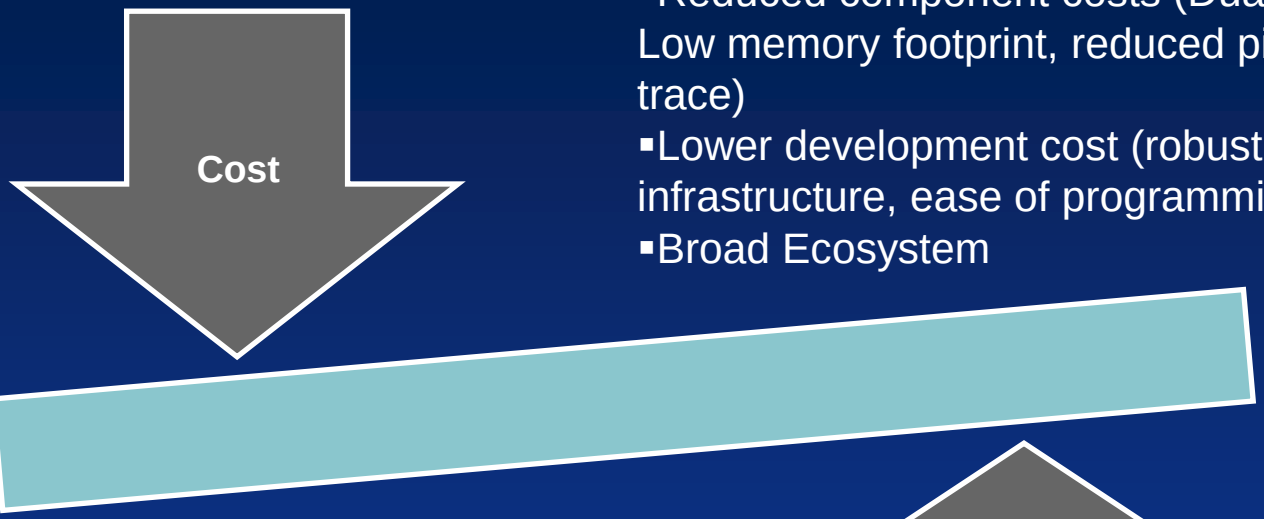
- Media content driving higher performance and larger memory sizes
- Security for Digital Rights Management
- Support for end application portability (Skype, Firefox)

Cost

Performance

Power

# SoC Architecture Trade-offs

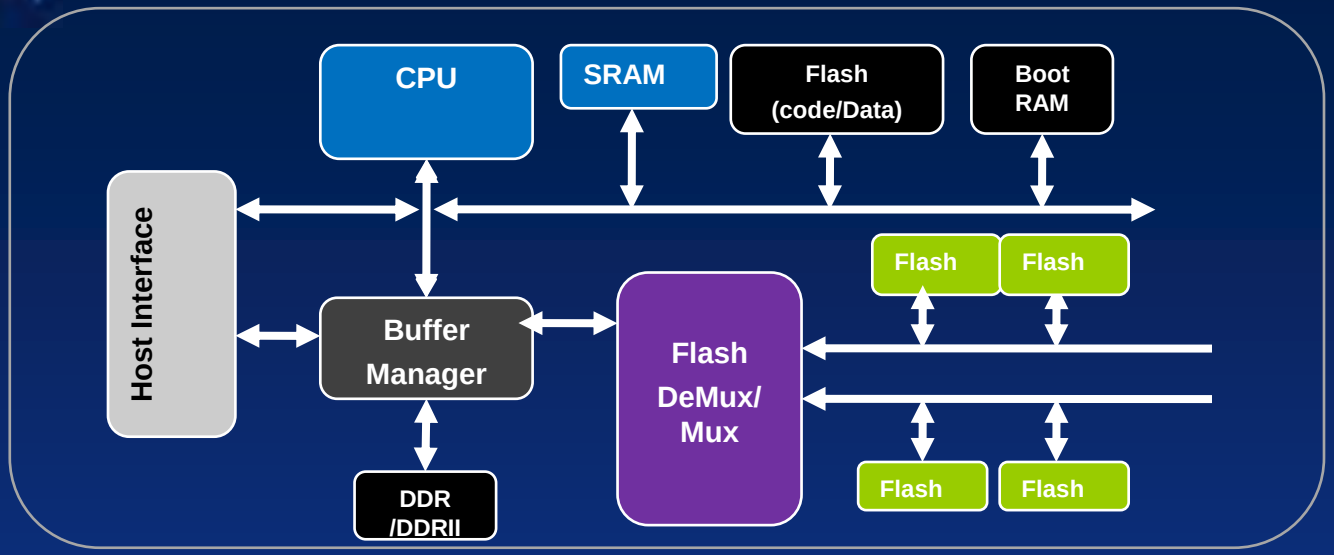



- Small, low power processor
- Reduced component costs (Dual sourcing, Low memory footprint, reduced pin counts for trace)
- Lower development cost (robust tools infrastructure, ease of programming )
- Broad Ecosystem

- Scalable performance up to1GHz
- Multi-layer, high-speed interconnect
- Standard High performance architectural features
- Superior Debug and Trace Capabilities
- Code density and performance

Architecture must scale up and down product lines

# Enterprise and Notebook/ePC SSD Controller architectures



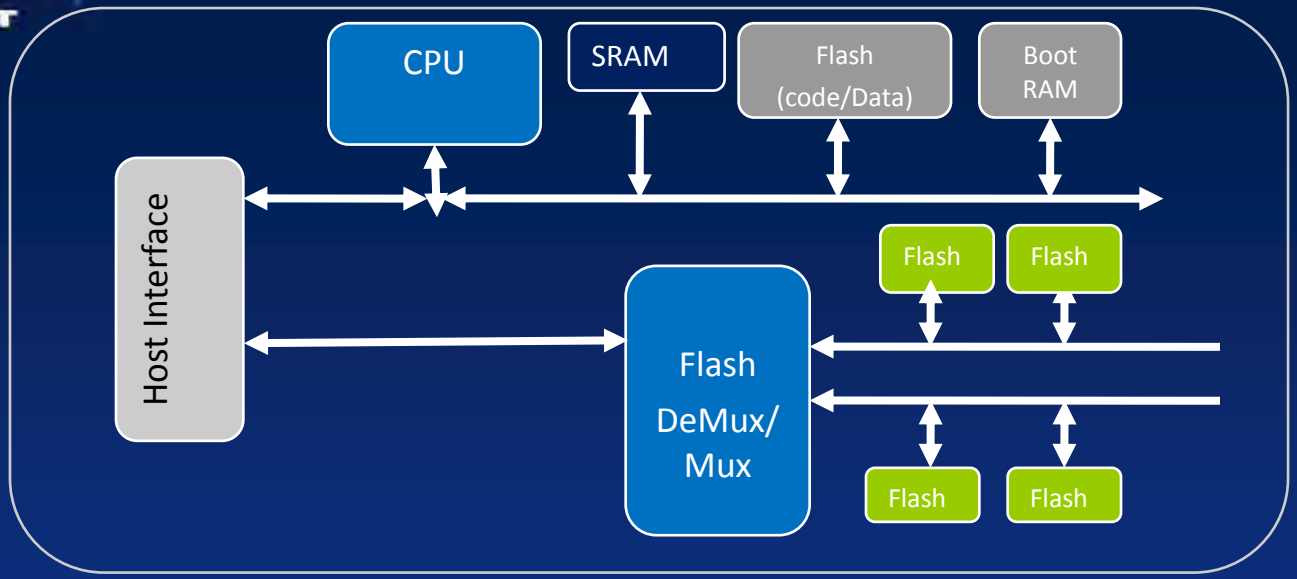

## Enterprise SSD

- CPU –Single core today moving to dual core
  - 400-1000 DMIPS
  - ECC support on all memories
- Host I/F -SATA II going to SATA III (6GBps)
  - IOPS 10K going to 50K
- Flash -Moving to ONFI 2.0 133-400MB/S
  - 4-10 Channels today moving to 16 -20 channels
  - Some implementations using embedded Cortex M3 class core for ECC and wear-leveling

## Notebook/ePC SSD

- CPU –single core
  - 200-500 DMIPS
- Host I/F -SATA I going to SATA II (3GBps)
  - IOPS 2-10K
  - Random IO Reads kill performance
- Flash -Moving to ONFI 2.0 133-400MB/S
  - 4-10 Channels today
  - MLC drives ECC and wear leveling

# Flash Card/USB Controller architecture




- CPU – approximately 40-100 DMIPS
  - Memory footprint for Flash Tables, ECC calc etc. is key
- Host I/F -USB 2.0 going to USB3.0
  - 4.8Gbps target is a 10X performance boost from USB2.0
  - Mainly sequential reads (media files etc.)
- Flash -Moving to ONFI 2.0 133-400MB/S
  - 2-10 Channels today


# Choosing the right architecture for Storage

- Established, proven architecture in Storage applications
- Architectural features such as ECC, and standard features for enhanced math performance, critical for algorithms calculations in storage.
- Open Programming model and rich software ecosystem
- Proven multi-core implementations with a common debug/trace environment for fast bring up and production
- IP eco-system around processor bus for rapid feature additions
- Roadmap and R&D commitment to performance/cost/power improvements enables designers to choose solutions that optimize their product goals