Storage Class Memory

the Future of Solid State Storage

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Santa Clara, CA USA
August 2009

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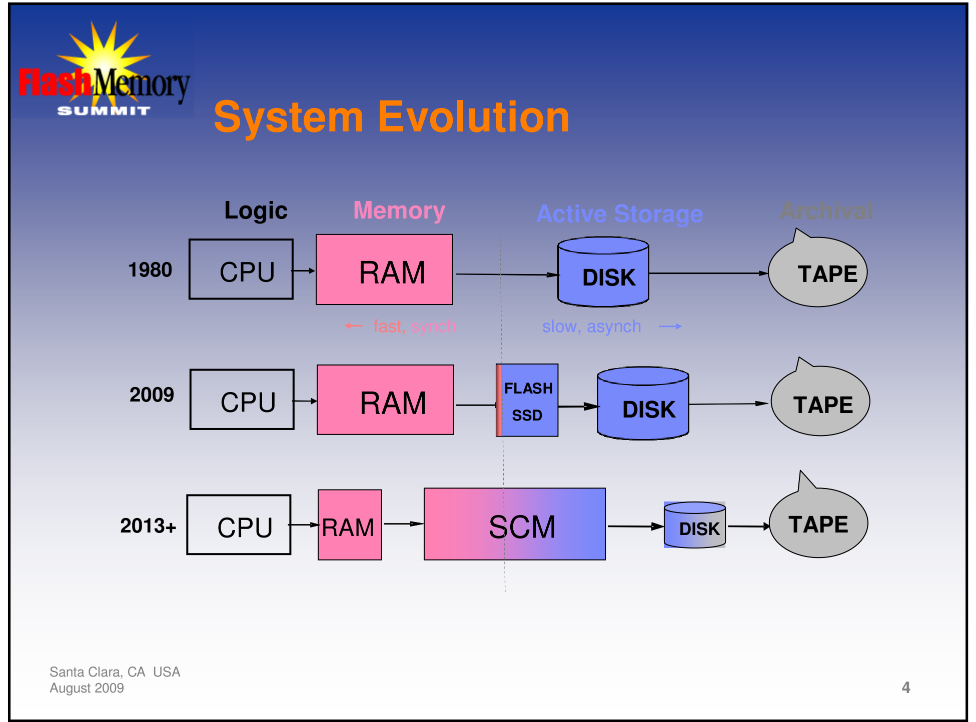
Abstract

- Storage Class Memory
  the Future of Solid State Storage
  - This tutorial describes 8 new technologies currently under development in research labs around the world that promise to replace today's NAND Flash technology. These new technologies - collectively called Storage Class Memory (SCM) - provide higher performance, lower cost, and more energy efficient solutions than today's SLC/MLC NAND Flash products. In this tutorial we extrapolate SCM technology trends to 2020 and analyze the impact on storage systems. The material is intended for those people that are closely watching the impact to the storage industry - brought about by NAND Flash - and want to understand what's next.

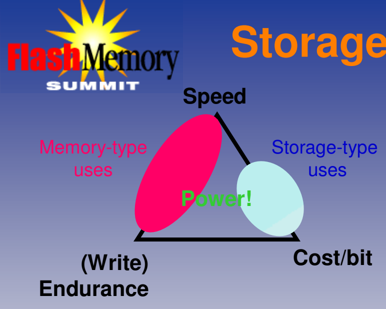
System Evolution



Definition of Storage Class Memory

- A new class of data storage/memory devices
  - many technologies compete to be the 'best' SCM
- SCM *blurs the distinction* between
  - MEMORY (*fast, expensive, volatile*) and
  - STORAGE (*slow, cheap, non-volatile*)
- SCM features:
  - Non-volatile
  - Short Access times (~ DRAM like)
  - Low cost per bit (DISK like – by 2020)
  - Solid state, no moving parts

Storage Class Memory



A solid-state memory that blurs the boundaries between storage and memory by being low-cost, fast, and non-volatile.

- SCM system requirements for Memory (Storage) apps
  - No more than 3-5x the Cost of enterprise HDD (< $1 per GB in 2012)
  - <200nsec (<1 µsec) Read/Write/Erase time
  - >100,000 Read I/O operations per second
  - >1GB/sec (>100MB/sec)
  - Lifetime of 10^9 – 10^{12} write/erase cycles
  - 10x lower power than enterprise HDD

Flash Memory
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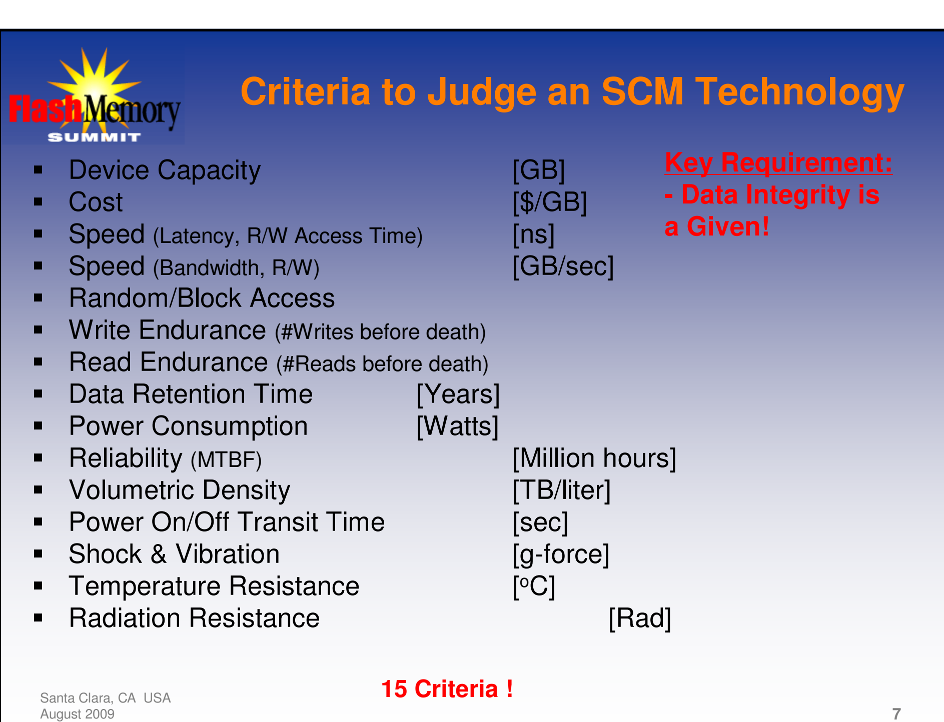
Flash Memory
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Criteria to Judge an SCM Technology
Device Capacity [GB]
Cost [$/GB]
Speed (Latency, R/W Access Time) [ns]
Speed (Bandwidth, R/W) [GB/sec]
Random/Block Access
Write Endurance (#Writes before death)
Read Endurance (#Reads before death)
Data Retention Time [Years]
Power Consumption [Watts]
Reliability (MTBF) [Million hours]
Volumetric Density [TB/liter]
Power On/Off Transit Time [sec]
Shock & Vibration [g-force]
Temperature Resistance [oC]
Radiation Resistance [Rad]
Key Requirement:
- Data Integrity is
a Given!
15 Criteria !
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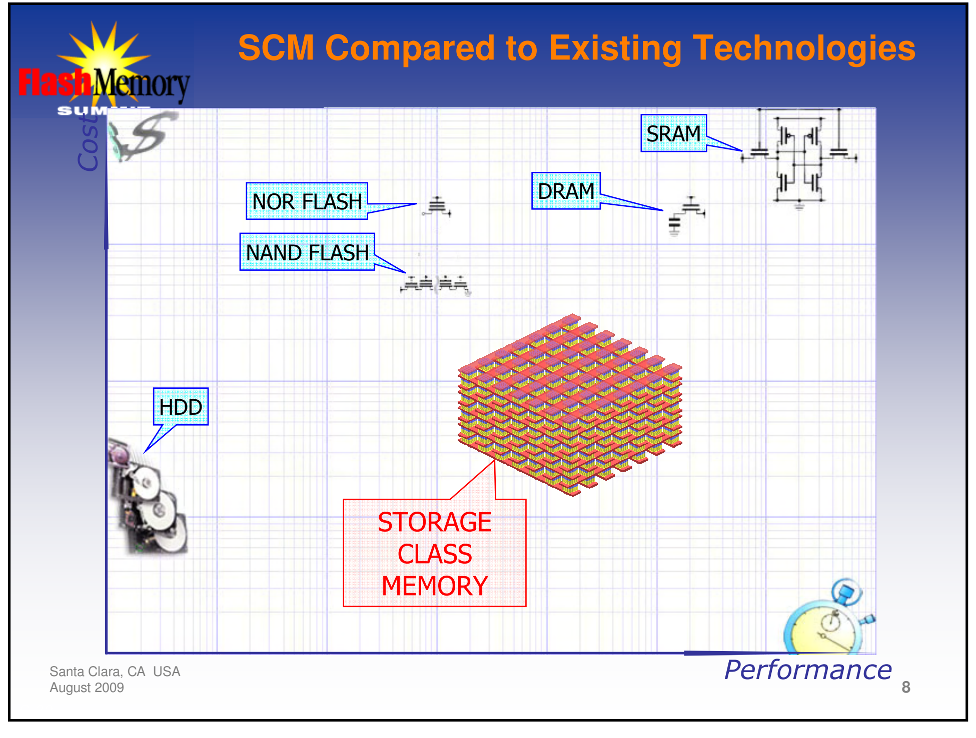
Flash Memory
SCM Compared to Existing Technologies
Cost
SRAM
NOR FLASH
DRAM
NAND FLASH
HDD
STORAGE
CLASS
MEMORY
Performance
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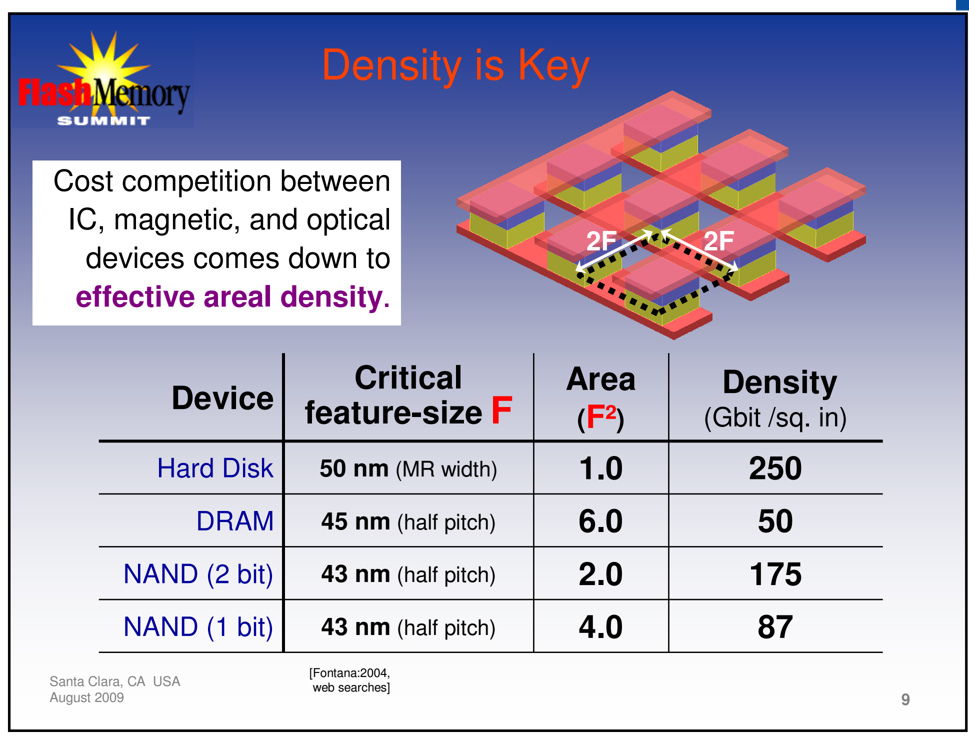
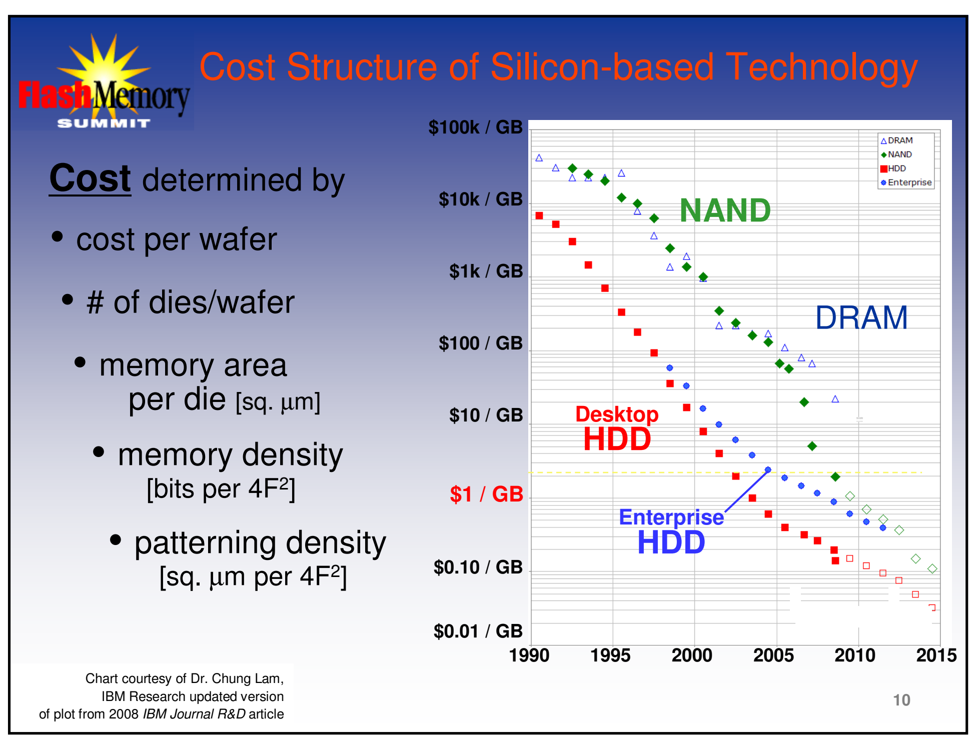


Device	Critical feature-size F	Area (F^2)	Density (Gbit /sq. in)
Hard Disk	50 nm (MR width)	1.0	250
DRAM	45 nm (half pitch)	6.0	50
NAND (2 bit)	43 nm (half pitch)	2.0	175
NAND (1 bit)	43 nm (half pitch)	4.0	87



Candidate Device Technologies

- Improved Flash
- FeRAM (Ferroelectric RAM)
- MRAM (Magnetic RAM)
  - Racetrack Memory
- RRAM (Resistive RAM)
  - Memristor
- Solid Electrolyte
- Phase Change Memory

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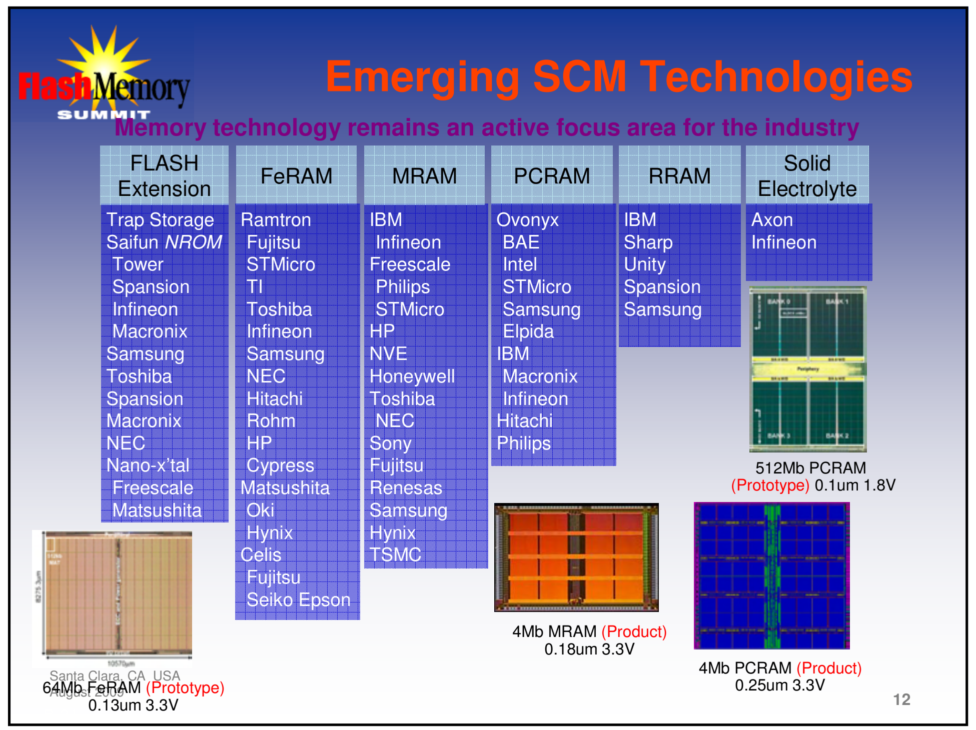

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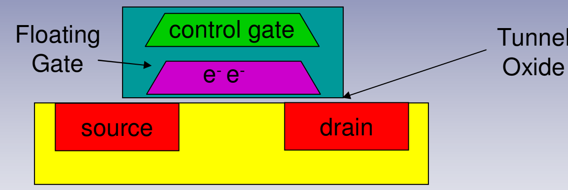
Improved Flash

- Flash – based on the metal-oxide-silicon (MOS) transistor with redesigned “floating gate”
  - Voltage threshold (Vth) is shifted by the charge near the gate, enabling non-volatile memory function



- Tradeoff exists between scaling, speed, and endurance
  - Designers are choosing to hold speed & endurance constant to continue scaling

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Flash Memory
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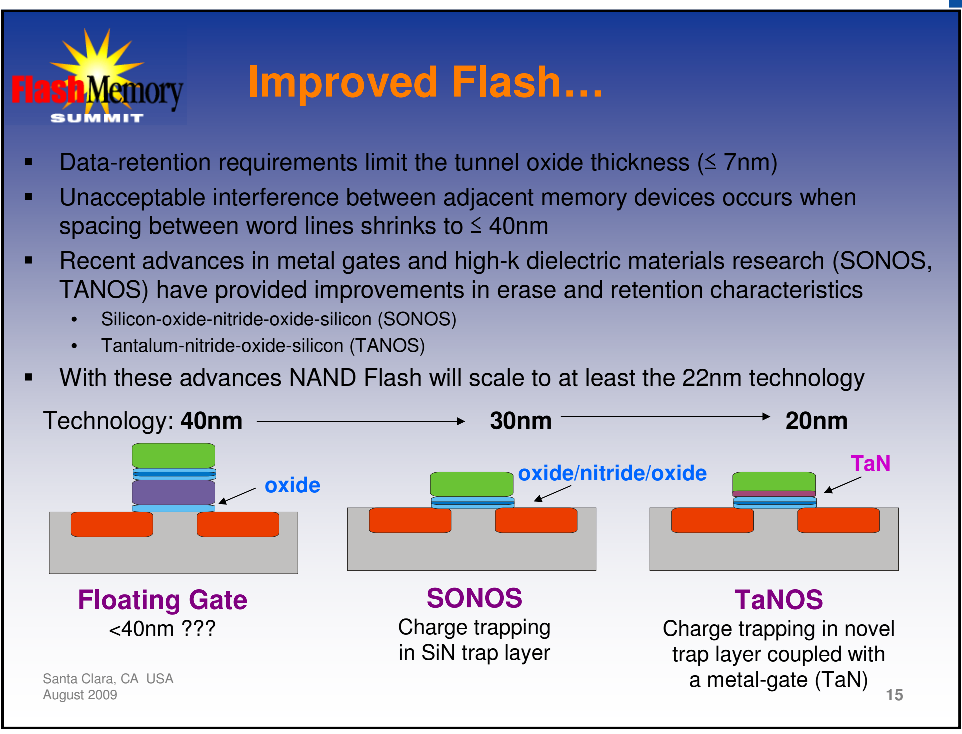
Improved Flash…
▪ Data-retention requirements limit the tunnel oxide thickness (≤ 7nm)
▪ Unacceptable interference between adjacent memory devices occurs when spacing between word lines shrinks to ≤ 40nm
▪ Recent advances in metal gates and high-k dielectric materials research (SONOS, TANOS) have provided improvements in erase and retention characteristics
• Silicon-oxide-nitride-oxide-silicon (SONOS)
• Tantalum-nitride-oxide-silicon (TANOS)
▪ With these advances NAND Flash will scale to at least the 22nm technology
Technology: 40nm
30nm
20nm
oxide
oxide/nitride/oxide
TaN
Floating Gate
<40nm ???
SONOS
Charge trapping in SiN trap layer
TaNOS
Charge trapping in novel trap layer coupled with a metal-gate (TaN)
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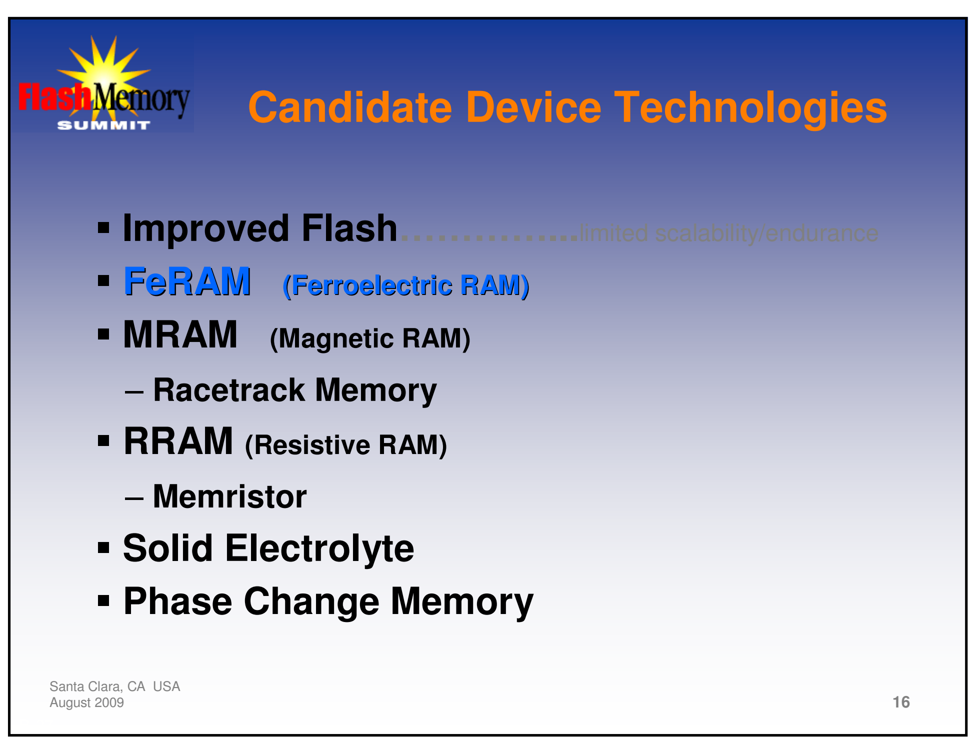
Candidate Device Technologies
▪ Improved Flash……………limited scalability/endurance
▪ FeRAM (Ferroelectric RAM)
▪ MRAM (Magnetic RAM)
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▪ RRAM (Resistive RAM)
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▪ Solid Electrolyte
▪ Phase Change Memory
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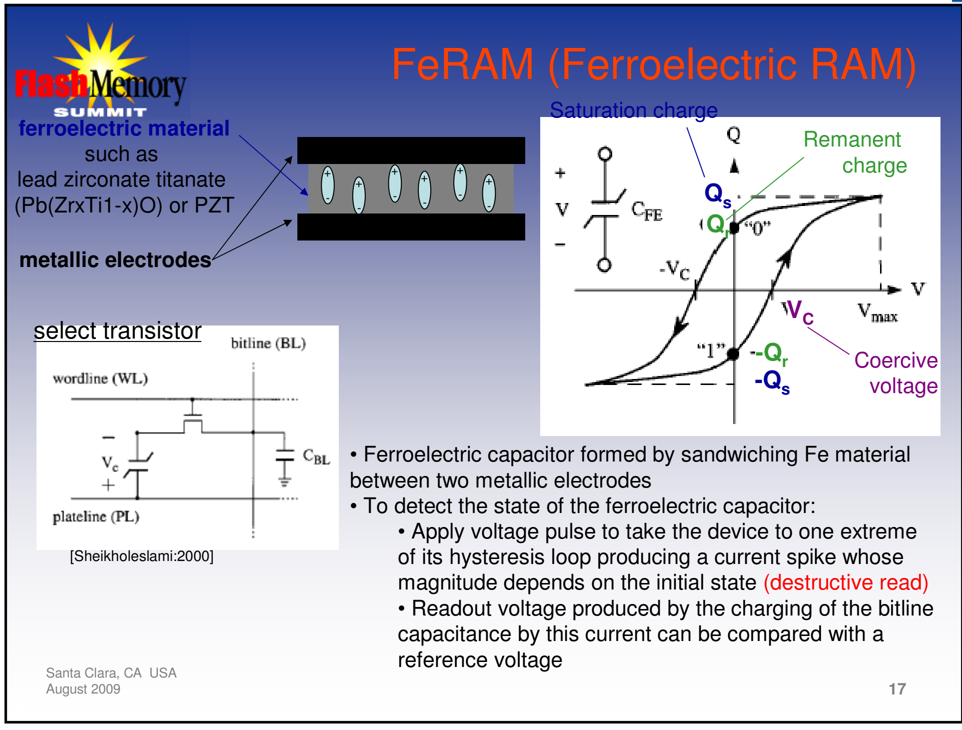

FeRAM (Ferroelectric RAM)

- Lots of attention in 1998-2003
  - Successfully used in Playstation 2 (embedded memory)
- Initially – very strong candidate to be the next NVRAM due to its non-volatility plus DRAM characteristics
  - Speed (as low as 20ns)
  - Low power
  - Low voltage operation
  - Straightforward CMOS integration
- Problem – cell size does not scale
  - Signal is directly proportional to cell size (scaling = reduced signal)
- More Problems – fatigue/insufficient remanent polarization, imprint, retention, high temp processing
  - Most recent work addresses embedded memory applications

Flash Memory
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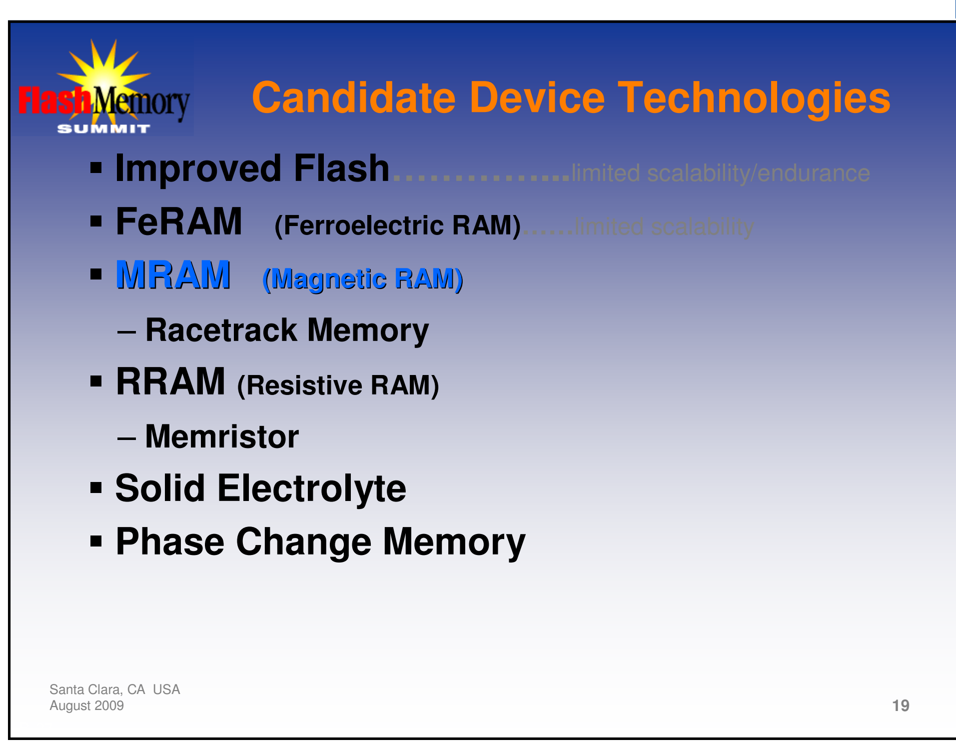
Flash Memory
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Solid Electrolyte
Phase Change Memory
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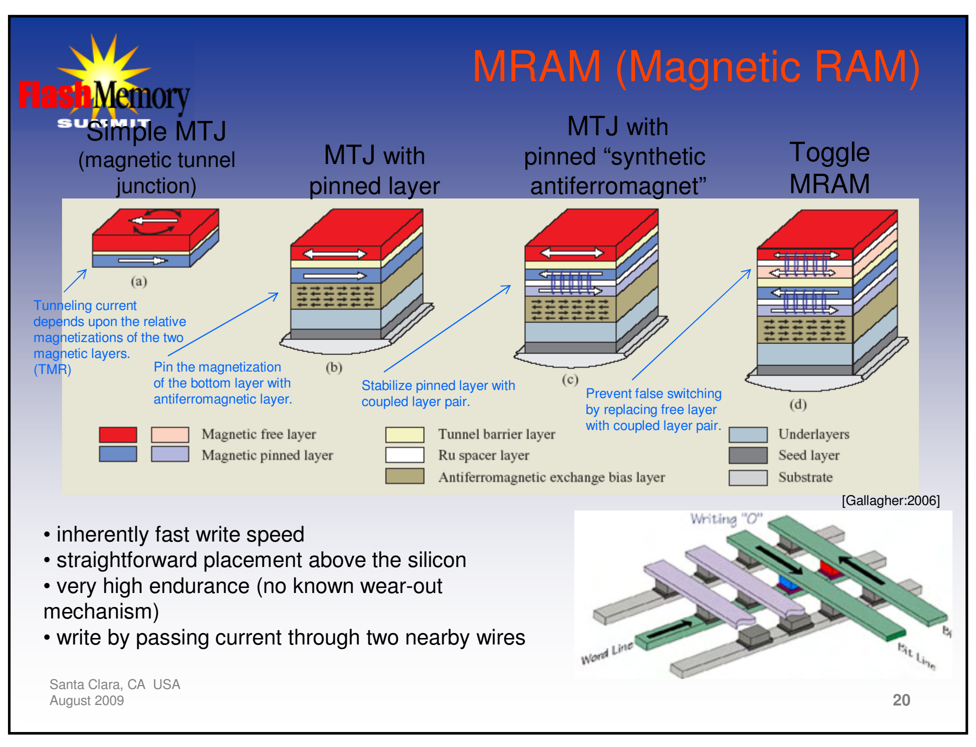
MRAM (Magnetic RAM)
Simple MTJ (magnetic tunnel junction)
MTJ with pinned layer
MTJ with pinned "synthetic antiferromagnet"
Toggle MRAM
Tunneling current depends upon the relative magnetizations of the two magnetic layers. (TMR)
Pin the magnetization of the bottom layer with antiferromagnetic layer.
Stabilize pinned layer with coupled layer pair.
Prevent false switching by replacing free layer with coupled layer pair.
(a)
(b)
(c)
(d)
Magnetic free layer
Magnetic pinned layer
Tunnel barrier layer
Ru spacer layer
Antiferromagnetic exchange bias layer
Underlayers
Seed layer
Substrate
[Gallagher:2006]
• inherently fast write speed
• straightforward placement above the silicon
• very high endurance (no known wear-out mechanism)
• write by passing current through two nearby wires
Writing "0"
Word Line
Bit Line
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Problems with MRAM

- Substantial progress made 2001 – 2004
- Commercially available as embedded memory

- **BUT**, write currents are very high – do not appear to scale well
  - → electromigration even at 180nm node
- Possible solutions
  - heat MTJ to reduce required current
  - use "spin-torque" effect
    - →rotate magnetization by passing current through the cell, but this causes a wear-out mechanism (thin tunneling layers)

- **Alternative:** store data in magnetic domain walls by building a magnetic racetrack in the third dimension

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Candidate Device Technologies

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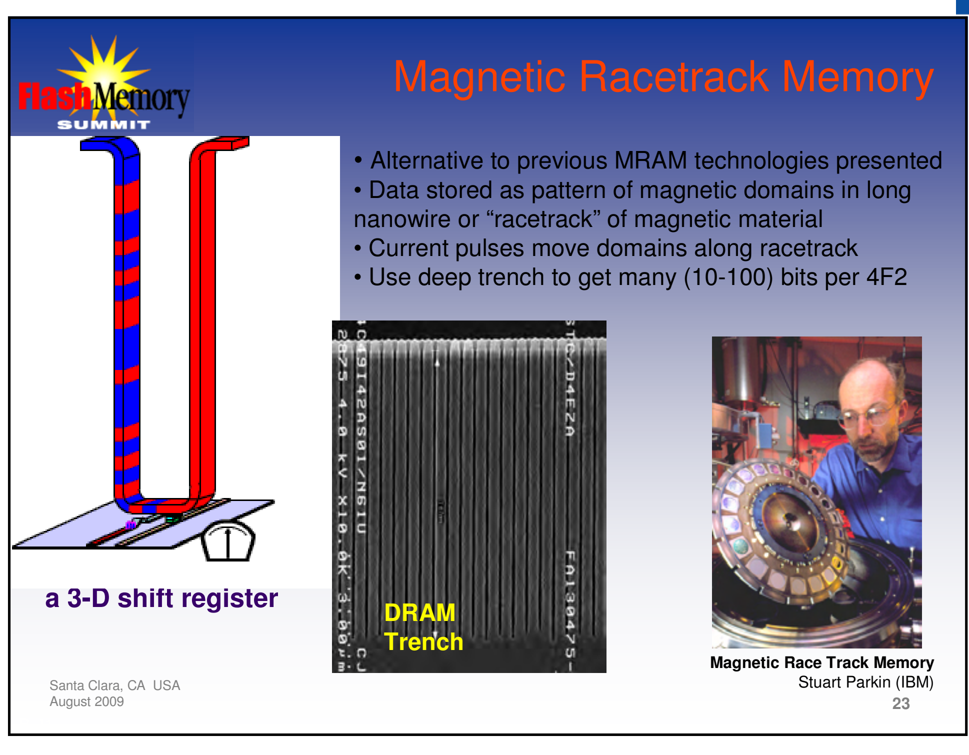
Magnetic Racetrack Memory
• Alternative to previous MRAM technologies presented
• Data stored as pattern of magnetic domains in long nanowire or "racetrack" of magnetic material
• Current pulses move domains along racetrack
• Use deep trench to get many (10-100) bits per 4F2
a 3-D shift register
DRAM Trench
Magnetic Race Track Memory
Stuart Parkin (IBM)
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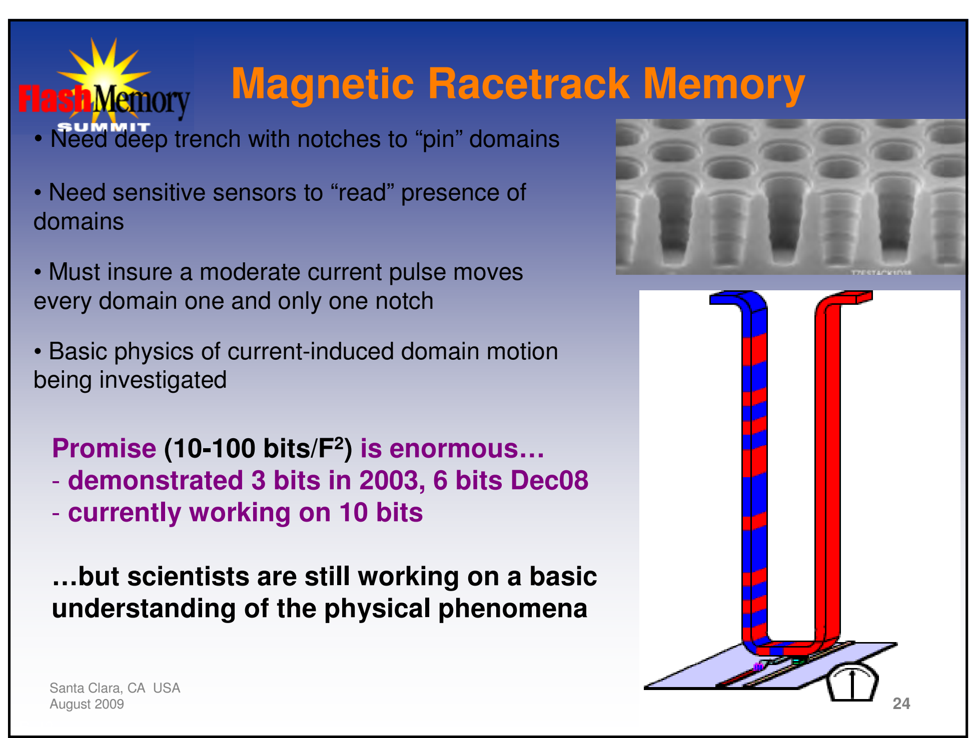
Magnetic Racetrack Memory
• Need deep trench with notches to "pin" domains
• Need sensitive sensors to "read" presence of domains
• Must insure a moderate current pulse moves every domain one and only one notch
• Basic physics of current-induced domain motion being investigated
Promise (10-100 bits/F²) is enormous…
- demonstrated 3 bits in 2003, 6 bits Dec08
- currently working on 10 bits
…but scientists are still working on a basic understanding of the physical phenomena
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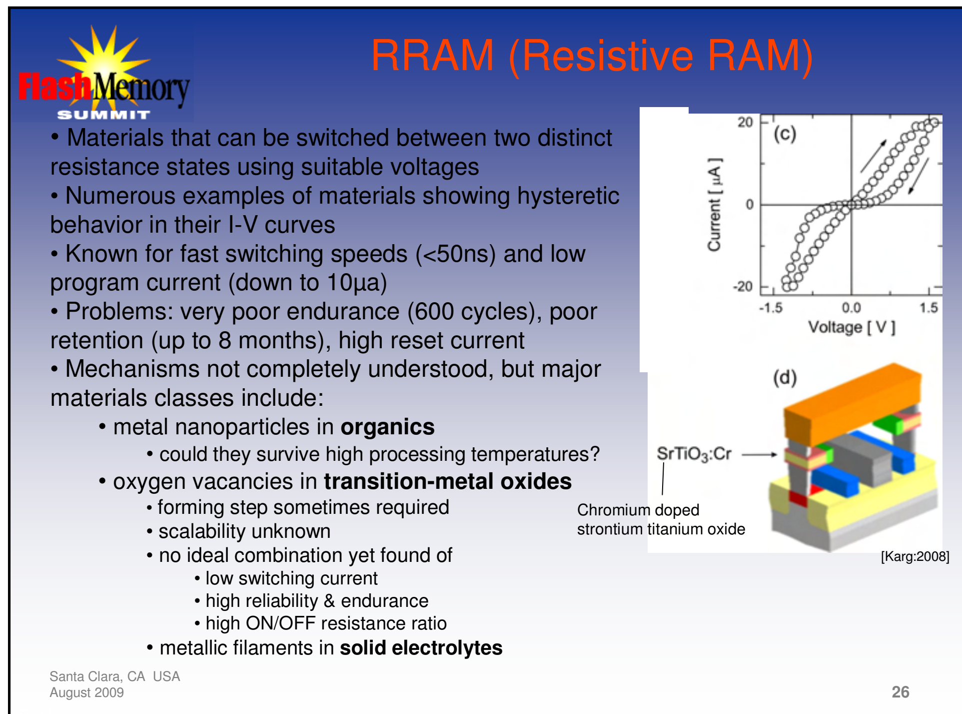

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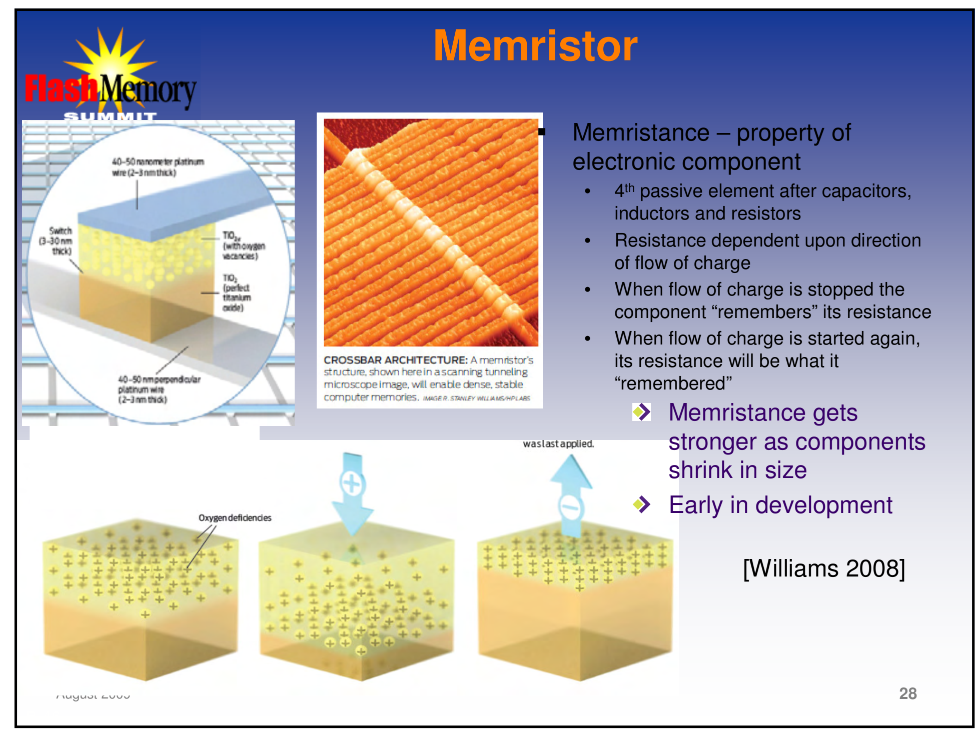
Memristor



- Memristance – property of electronic component
  - 4th passive element after capacitors, inductors and resistors
  - Resistance dependent upon direction of flow of charge
  - When flow of charge is stopped the component "remembers" its resistance
  - When flow of charge is started again, its resistance will be what it "remembered"
    - Memristance gets stronger as components shrink in size
    - Early in development

[Williams 2008]

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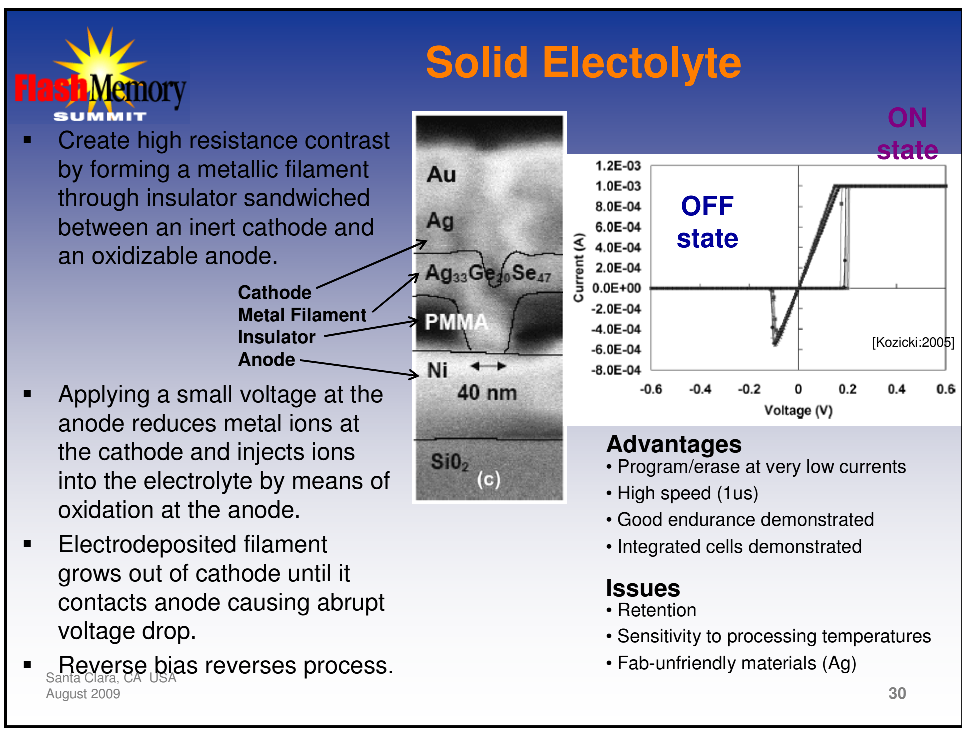

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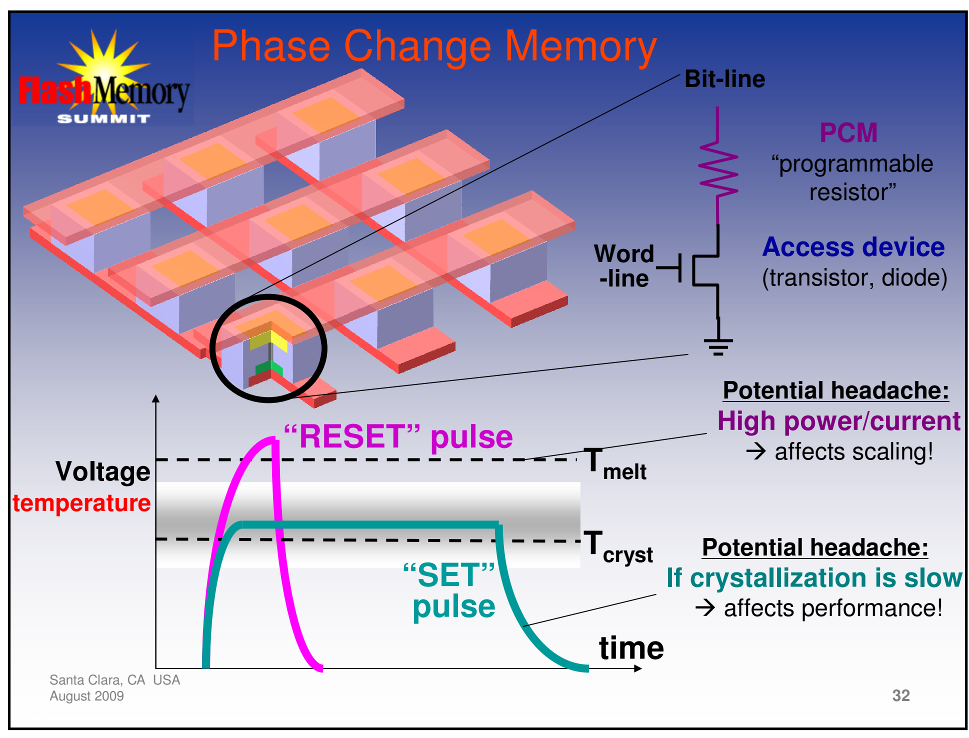

Flash Memory
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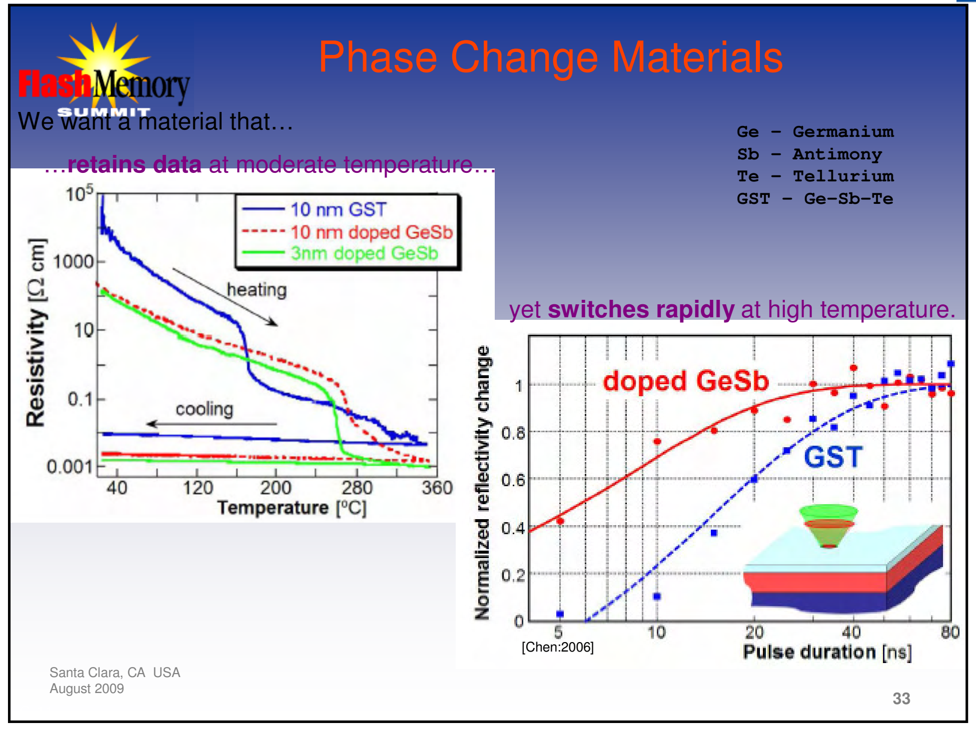
Phase Change Materials
We want a material that…
…retains data at moderate temperature…
Ge – Germanium
Sb – Antimony
Te – Tellurium
GST – Ge-Sb-Te
10 nm GST
10 nm doped GeSb
3nm doped GeSb
heating
cooling
Resistivity [Ω cm]
Temperature [°C]
yet switches rapidly at high temperature.
doped GeSb
GST
Normalized reflectivity change
Pulse duration [ns]
[Chen:2006]
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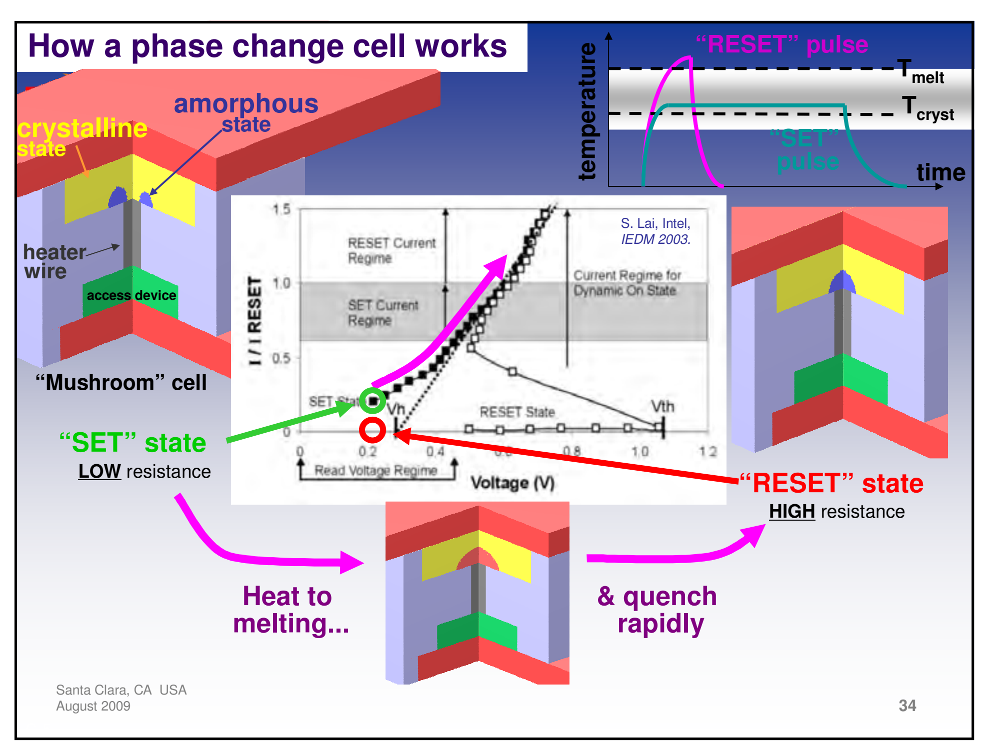
How a phase change cell works
"RESET" pulse
T_{melt}
T_{cryst}
"SET" pulse
temperature
time
crystalline state
amorphous state
heater wire
access device
"Mushroom" cell
S. Lai, Intel, IEDM 2003.
RESET Current Regime
SET Current Regime
Current Regime for Dynamic On State
RESET State
Vth
Vh
I / I RESET
Read Voltage Regime
Voltage (V)
"SET" state
LOW resistance
"RESET" state
HIGH resistance
Heat to melting...
& quench rapidly
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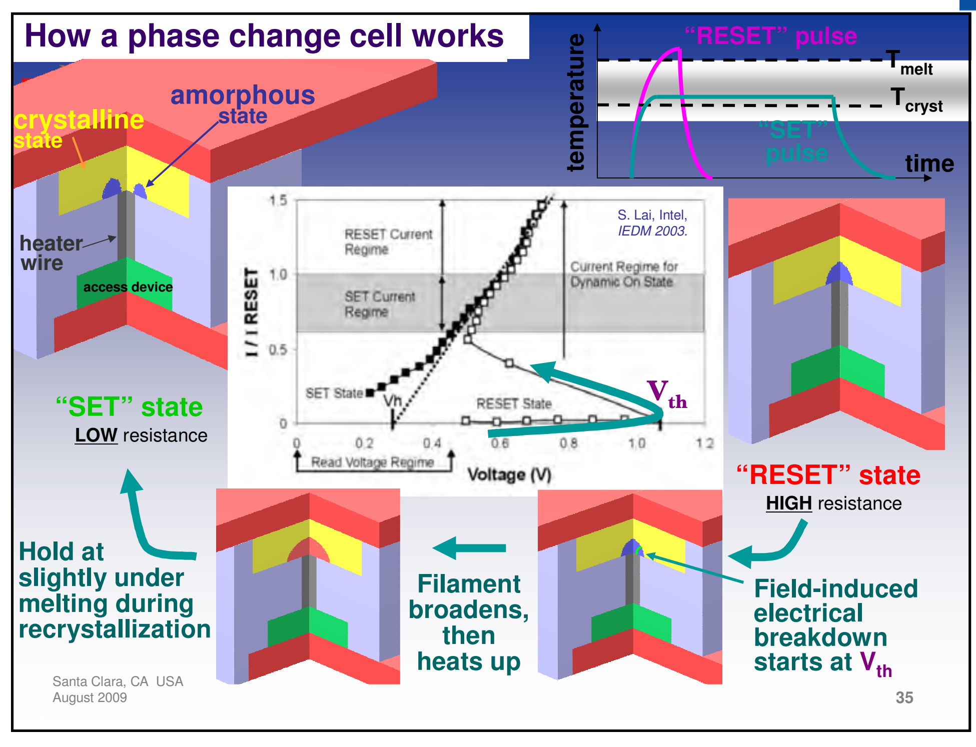
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SET State
RESET State
Vh
V_{th}
I / I RESET
Read Voltage Regime
Voltage (V)
"RESET" state
HIGH resistance
Hold at slightly under melting during recrystallization
Filament broadens, then heats up
Field-induced electrical breakdown starts at V_{th}
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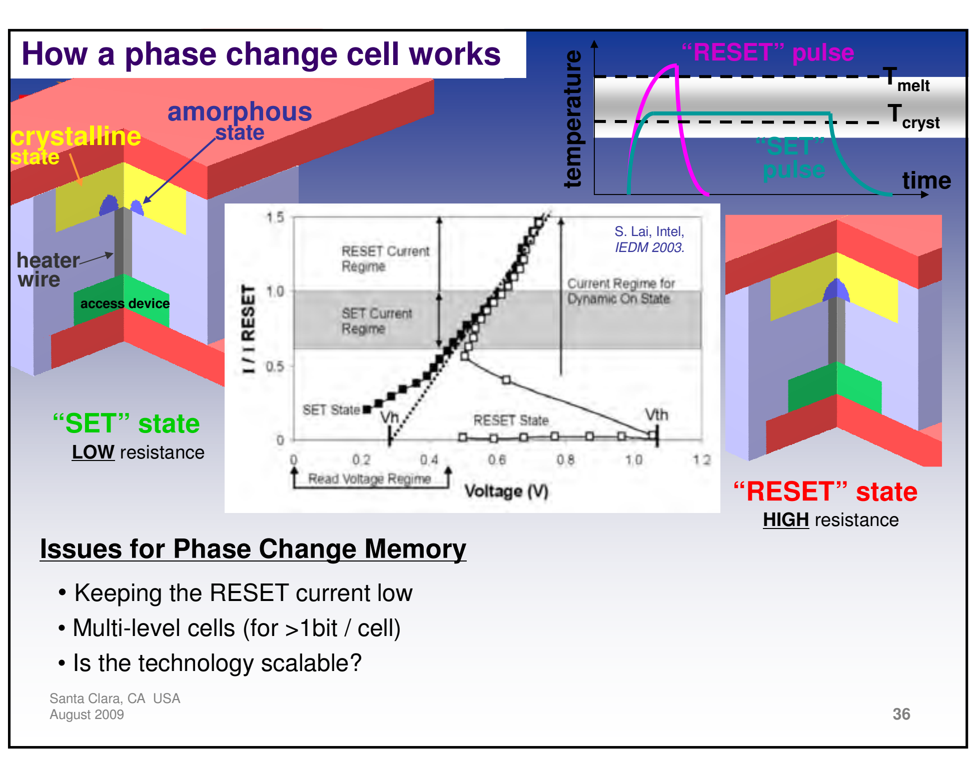
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Read Voltage Regime
Voltage (V)
"RESET" state
HIGH resistance
Issues for Phase Change Memory
• Keeping the RESET current low
• Multi-level cells (for >1bit / cell)
• Is the technology scalable?
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PCM Characteristics

Basic requirements

- ✓ widely separated SET and RESET resistance distributions
- ✓ switching with accessible electrical pulses
- ✓ the ability to read/sense the resistance states without perturbing them
- ✓ high write **endurance** (many switching cycles between SET and RESET)
- ✓ long data **retention** ("10-year data lifetime" at some elevated temperature)
  → avoid unintended re-crystallization
- ✓ **fast** SET speed
- ✓ **MLC** capability – more than one bit per cell

Phase Change Nano-Bridge

- Invented in Dec 2006
- memory device with ultra-thin films (3nm)
- works at the 22nm node
- fast SET (<100ns)
- low RESET current (<100µa)

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Outlook of PCM

Scaling outlook appears to be "good" for PC-RAM

By adding two bits per cell, Intel and ST Microelectronics have put phase-change memory on par with today's flash technology, says H.-S. Philip Wong, professor of electrical engineering at Stanford University. Intel has already mastered a similar trick with flash

Phase-change memory has made a lot of progress in the past few years, Wong adds. "A few years ago it looked promising," he says. "But now it's going to happen. There's no doubt about it."

February 4, 2008
[http://www.technologyreview.com/Infotech/20148/]

→ Focus now on novel IP, implementation, and cost reduction.

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  - **Memristor**.........................early in development
- **Solid Electrolyte**.............in development, promising
- **Phase Change Memory**....it's going to happen

In Comparison…

	Improved Flash	FeRAM	MRAM	Racetrack
Knowledge level	advanced development	product	product	basic research
Smallest demonstrated cell	$4F^2$ ($1F^2$ per bit)	$15F^2$ (@130nm)	$25F^2$ @180nm	—
Prospects for… …scalability	**maybe** (enough stored charge?)	**poor** (integration, signal loss)	**poor** (high currents)	**unknown** (too early to know, good potential)
…fast readout	yes	yes	yes	yes
…fast writing	**NO**	yes	yes	yes
…low switching Power	yes	yes	**NO**	**uncertain**
…high endurance	**poor** ($1e^7$ cycles)	yes	yes	should
…non-volatility	yes	yes	yes	**unknown**
…MLC operation	yes	**difficult**	**NO**	yes **(3-D)**

In Comparison…

	RRAM	Memristor	Solid Electrolyte	PCRAM
Knowledge level	Early development	Early development	development	advanced development
Smallest demonstrated cell	—	—	$8F^2$ @90nm ($4F^2$ per bit)	$5.8F^2$ (diode) $12F^2$ (BJT) @90nm
Prospects for… …scalability	unknown	unknown	promising (filament-based, but new materials)	promising (rapid progress to date)
…fast readout	yes	yes	yes	yes
…fast writing	sometimes	sometimes	yes	yes
…low switching Power	sometimes	sometimes	yes	poor
…high endurance	poor	poor	unknown	yes
…non-volatility	sometimes	sometimes	sometimes	yes
…MLC operation	yes	yes	yes	yes

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Take - Aways

- One or more of these technologies will successfully be introduced within the next 5 years or so, bringing us lower costs and higher performance
- NAND Flash still has a lot of life left and will serve the storage industry well
- Most likely technologies to replace NAND Flash (in order):
  1. Phase Change Memory
  2. Solid Electrolyte
  3. Racetrack Memory
  4. Memristor
- No date projections yet for these new technologies, but…
  - Numonyx announced in Feb 2008 that they were sampling 128Mb, 90nm Phase Change Memory parts (“Alverstone”)

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Q&A / Feedback

- Please send any questions or comments on this presentation to SNIA: tracksolidstate@snia.org

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Geoffrey W. Burr
Bulent Kurdi
Dr. Richard Freitas
Phillip R. Mills

References

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  - http://www.usenix.org/events/fast/tutorials/T3.pdf
- **IBM Journal of Research and Development**
  - **Special issue on storage**
  - **http://www.research.ibm.com/journal/rd52-45.html**
  - **Four papers related to SCM**