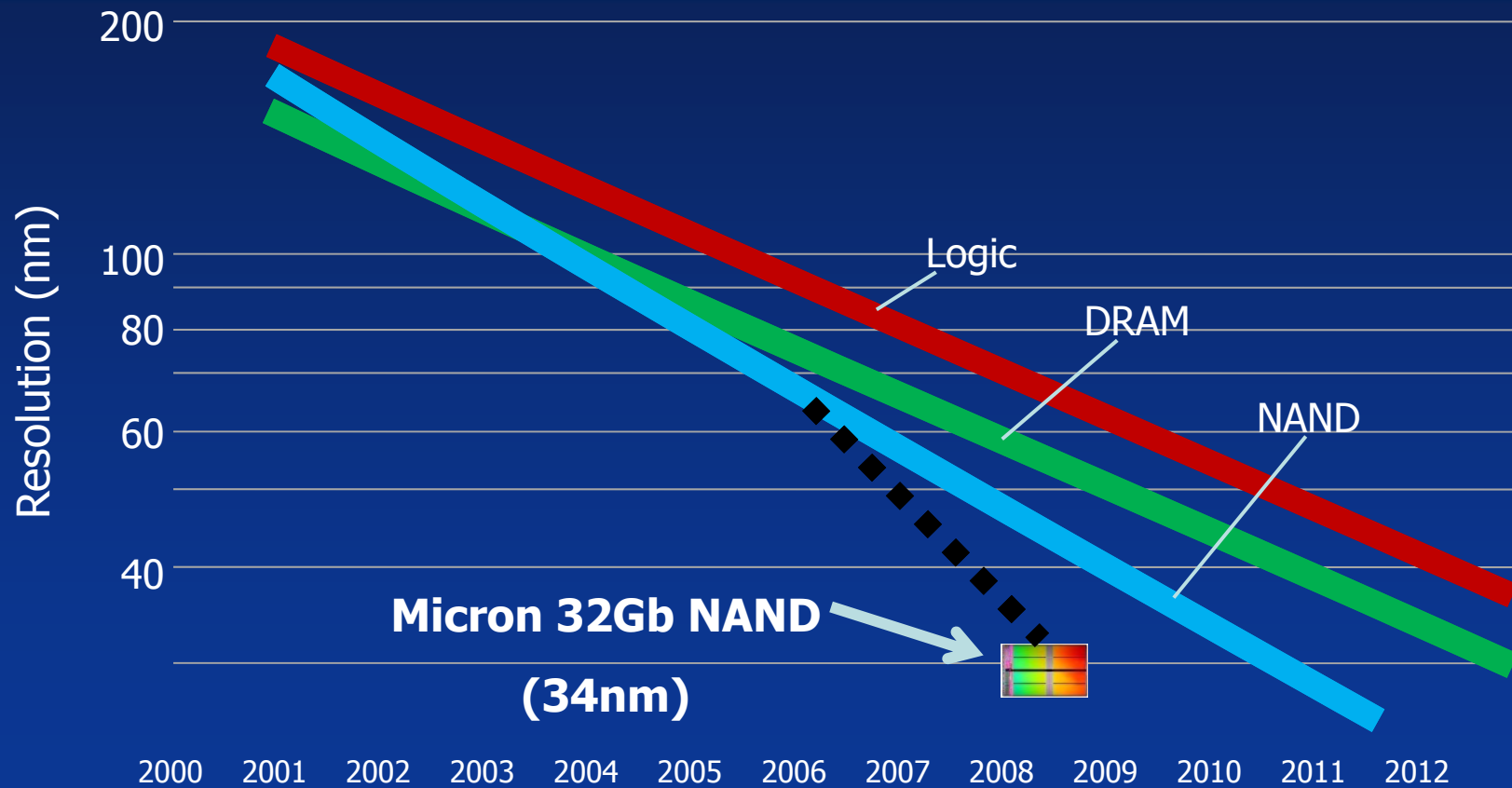# NAND Flash Architecture and Specification Trends

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Abstract

- As NAND Flash continues to shrink, page sizes, block sizes, and ECC requirements are increasing while data retention, endurance, and performance are decreasing.

- These changes impact systems including random write performance and more.

- Learn how to prepare for these changes and counteract some of them through improved block management techniques and system design.

- This presentation also discusses some of the tradeoff myths – for example, the myth that you can directly trade ECC for endurance
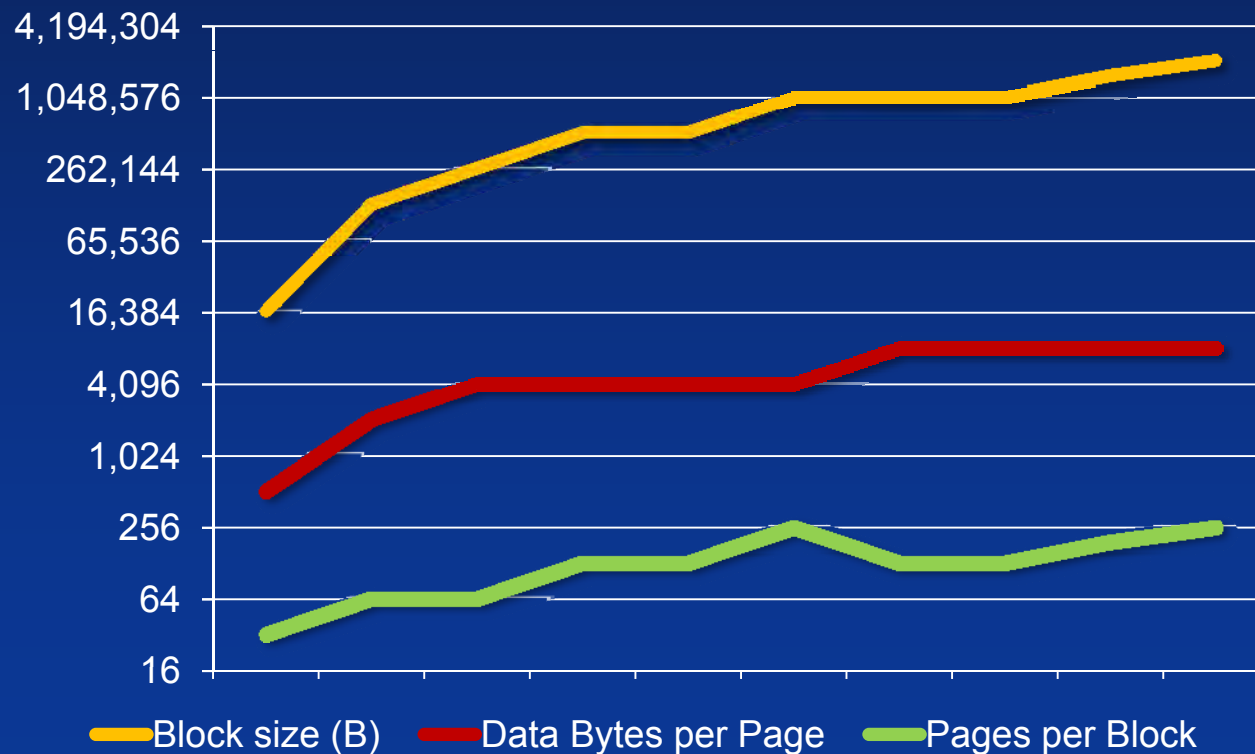
NAND Flash: Shrinking Faster Than Moore's Law

Resolution (nm)

- 200
- 100
- 80
- 60
- 40

Logic

DRAM

NAND

Micron 32Gb NAND

(34nm)

2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012

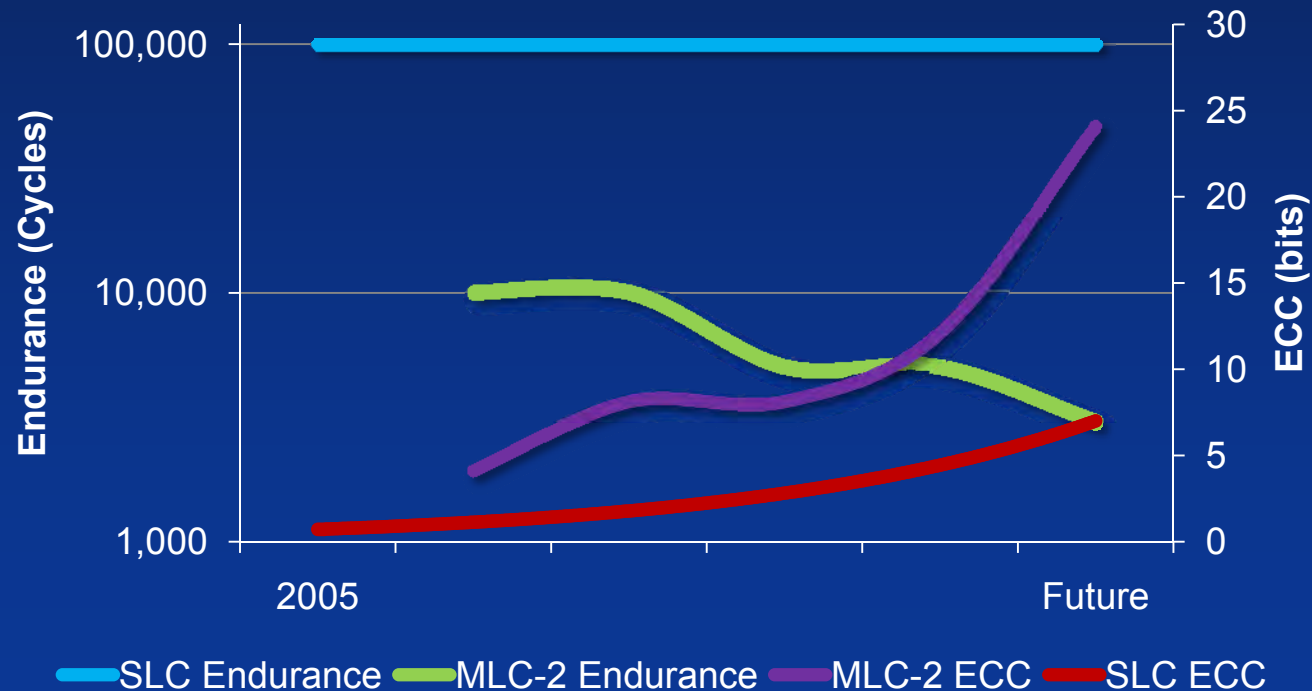Semiconductor International, 1/1/2007

Memory Organization Trends

- Over time, NAND block size is increasing.
  - Larger page sizes increase sequential throughput.
  - More pages per block reduce die size.

Block size (B)   Data Bytes per Page   Pages per Block

Consumer-grade NAND Flash: Endurance and ECC Trends

- Process shrinks lead to less electrons per floating gate.
- ECC used to improve data retention and endurance.
- To adjust for increasing RBERs, ECC is increasing exponentially to achieve equivalent UBERs.
- For consumer applications, endurance becomes less important as density increases.

SLC Endurance ▬ MLC-2 Endurance ▬ MLC-2 ECC ▬ SLC ECC
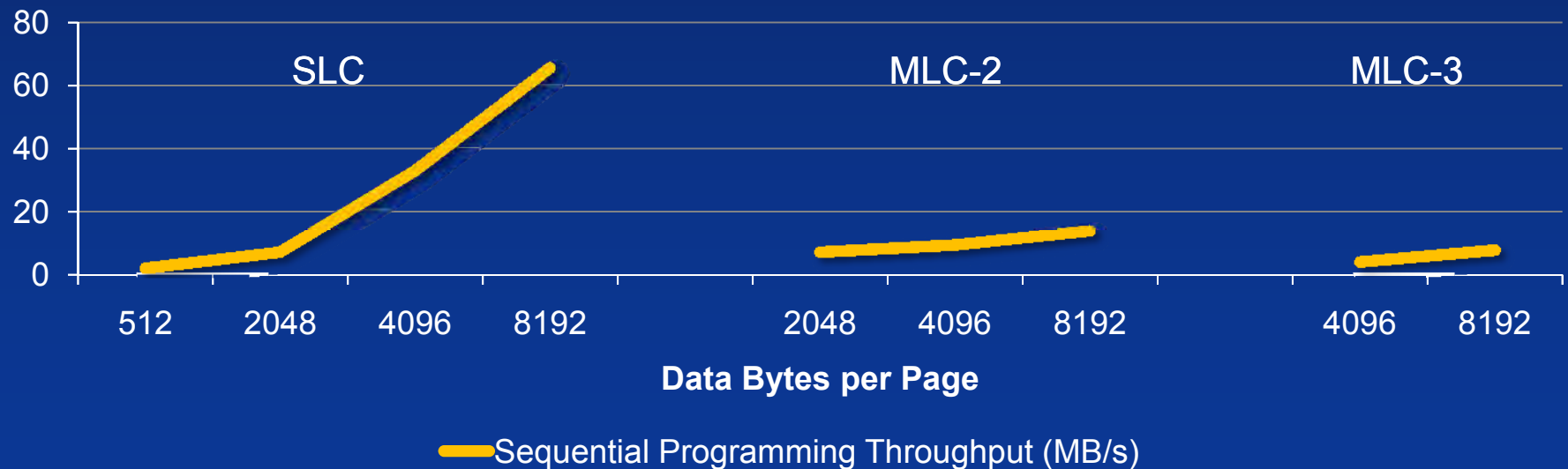
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Myth: More ECC Extends Block Endurance

- Block endurance is how long a block is usable before program or erase status failures occur.

- Applying more ECC than required does not automatically extend the block endurance.

- NAND devices are configured to trigger program and erase status failures for a specific, fixed ECC value predetermined at the factory to meet qualification requirements.

- Applying extra ECC does not change these predetermined thresholds, which means that program and erase status failures begin to occur at the same cycling intervals regardless of the amount of ECC applied.

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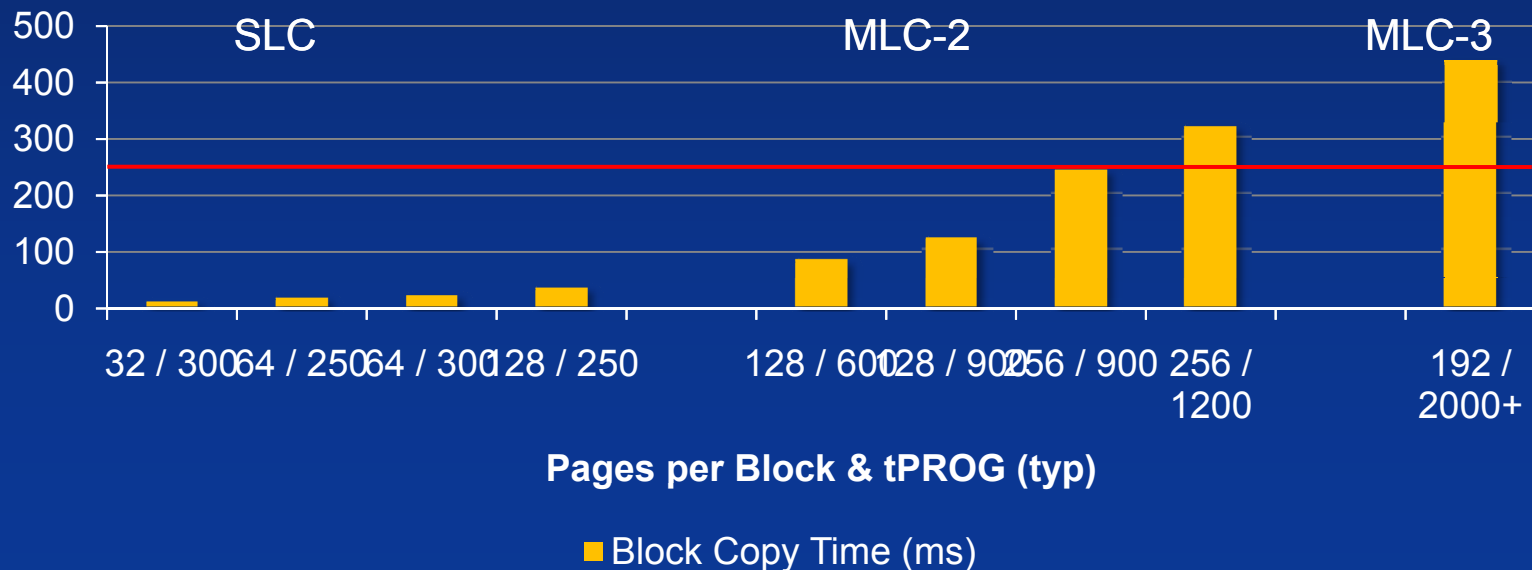# Larger Page Sizes Improve Sequential Write Performance

- For a fixed page size, write throughput decreases as NAND process shrinks
- NAND vendors increase the page size to compensate for slowing array performance
- Write throughput decreases with more bits per cell

Sequential Programming Throughput (MB/s)

More Pages Per Block Affect Random Write Performance

- The block copy time is the largest limiting factor for random write performance.
- As block copy time increases, random performance decreases.
  - Number of pages per block is the dominant factor.
  - Increase of tPROG is the next largest factor.
  - Increase in I/O transfer time due to increasing page size (effect not shown below) is also a factor.
- Some card interfaces have write timeout specs at 250ms, which means that block management algorithms manage partial blocks.

Pages per Block & tPROG (typ)
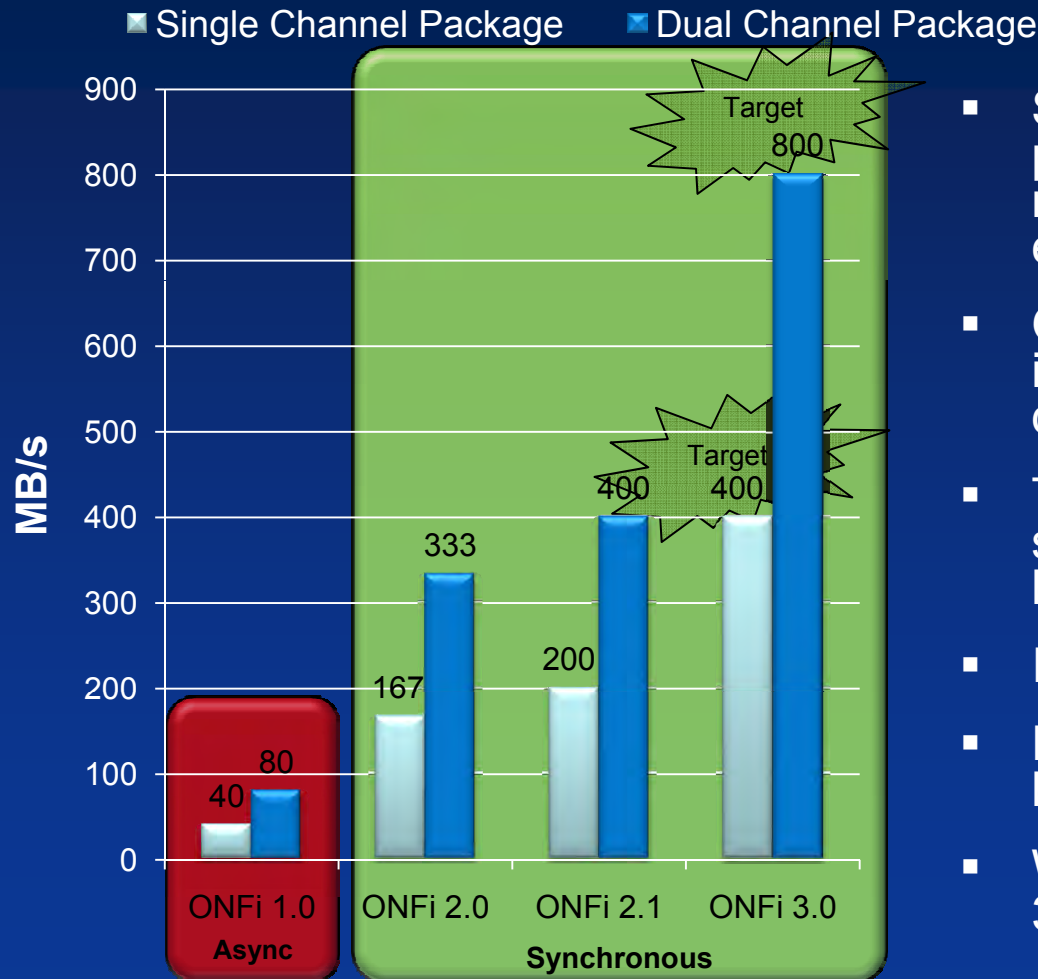
■ Block Copy Time (ms)

NAND Interface

- The NAND interface is increasing in throughput
  - Allows better utilization of I/O channels – higher bandwidth
  - Immediately useful for single die read performance
  - Modest improvement for write performance with multiple die
- Important for SSDs, enterprise applications
  - Reduces I/O channels

NAND Interface Trends

Interface Standard (x8)	Max Throughput (MB/s)
No standard	40
ONFI 1.0 Async (12/06)	50
ONFI 2.0 Sync (2/08)	133
ONFI 2.1-2.2 Sync (1/09, 9/09)	200
Toggle Mode (not published)	133
ONFI 3.0 Sync	400

The ONFI Advantage

Single Channel Package   Dual Channel Package

- Supports simultaneous read, program, and erase operations on multiple die on the same chip enable since ONFI 1.0

- Only industry-standard NAND interface capable of 200MB/sec data rate from a single die

- Two independent channels in a single package (doubles the bandwidth)

- In volume production today

- Headroom for 400MB/sec and beyond

- Work has already begun on ONFI 3.0

Members

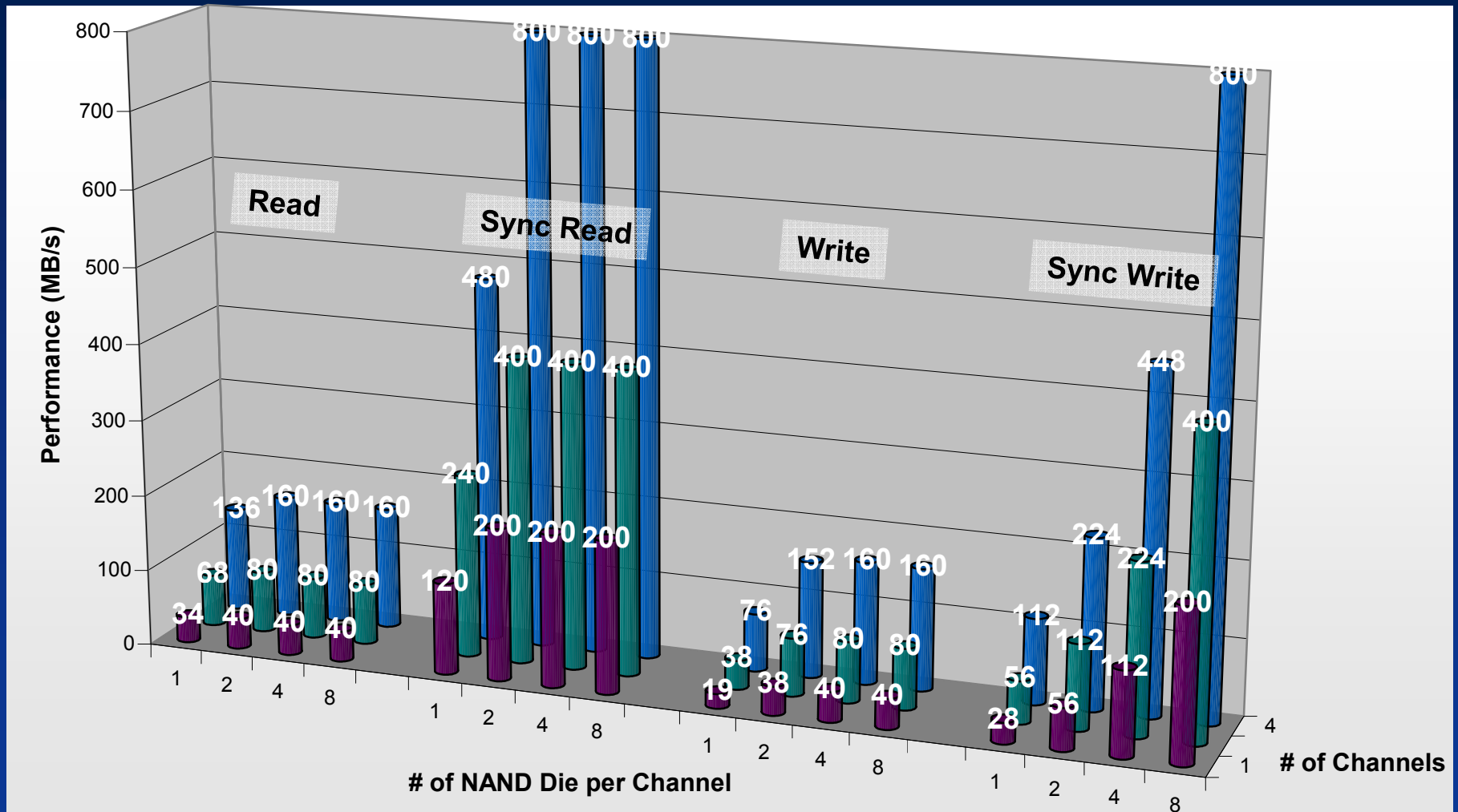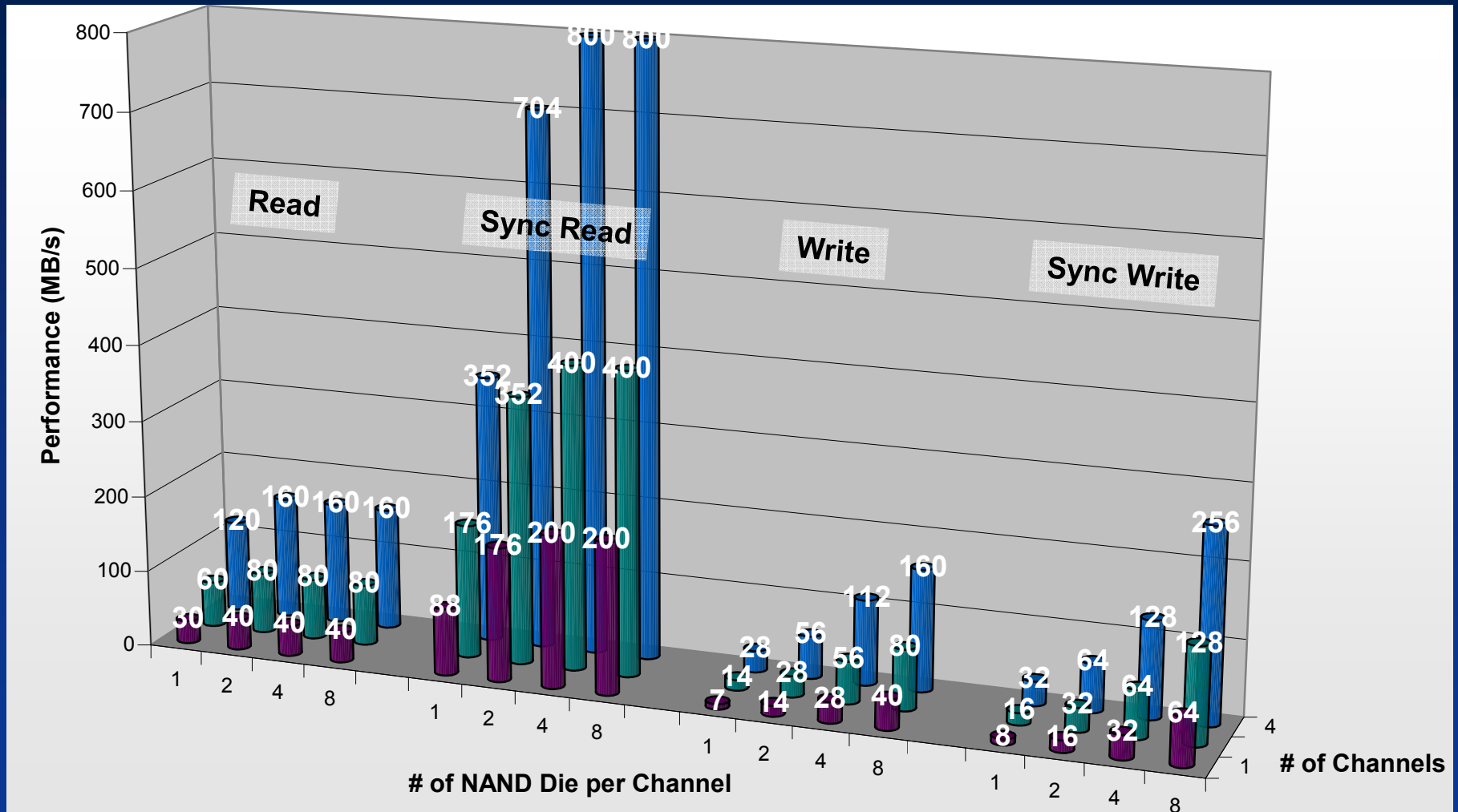|		
A-Data	Afa Technologies	Alcor Micro
Aleph One	Anobit Tech.	Apacer
Arasan Chip Systems	ASMedia Technology	ATI
Avid Electronics	BitMicro	Biwin Technology
Chipsbank	Cypress	DataFab Systems
Data I/O	Datalight	Denali Software
ENE Technology	Entorian	FCI
FormFactor	Foxconn	Fresco Logic
Fusion Media Tech	Genesys Logic	Hagiwara Sys-Com
HiperSem	Hitachi GST	Hyperstone
InCOMM	Indilinx	Inphi
Intelliprop	ITE Tech	Jinvani Systech
Kingston Technology	Lauron Technologies	Lotes
LSI	Macronix	Marvell
Mentor Graphics	Metaram	Moai Electronics
Molex	NVidia	Orient Semiconductor
P.A. Semi	Powerchip Semi.	Power Quotient International
Prolific Technology	Qimonda	Sandforce
Seagate	Shenzhen Netcom	Sigmatel
Silicon Integrated Systems	Silicon Motion	Silicon Storage Tech
Silicon Systems	STEC	Skymedi
Smart Modular Tech.	Solid State System	Super Talent Electronics
Synopsys	Tandon	Tanisys
Telechips	Teradyne, Inc.	Testmetrix
Transcend Information	Tyco	UCA Technology
University of York	Virident Systems	WinBond

Improving System Performance

- System performance is increased by adding more channels or more die per channel.
- Ignoring effects of ECC and block management algorithms, total throughput is either array or I/O throughput limited.

MLC 4KB 2-plane Throughput Example: Async vs. Sync Interface

Conclusions

- Larger block sizes to become more difficult to manage
- Page size doubles increasing sequential performance while reducing random performance to compensate for overall slower array throughput
- ECC increases to compensate for data retention and endurance; even still endurance is decreasing for consumer NAND memory
- 2bpc MLC has a lower manufacturing cost per bit as long as it is on a smaller process node than 3bpc MLC memory – and it fits more customer applications!
- Pages per block increasing to reduce die size
- Interface performance increasing to open up a whole new market – enterprise solutions – while helping improve SSD performance
- ONFI provides a proactive, scalable interface for the future with broad industry support

Questions?

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About Michael Abraham

- Manager of Micron's NAND Flash Applications Engineering group

- B.S. in Computer Engineering from Brigham Young University

- Technical representative for Micron in ONFI and JEDEC for NAND Flash

- Key role in defining and standardizing the high-speed, synchronous DDR NAND interface within Micron and at ONFI

Santa Clara, CA USA
August 2009