Error Correcting Techniques for Future NAND Flash Memory in SSD Applications

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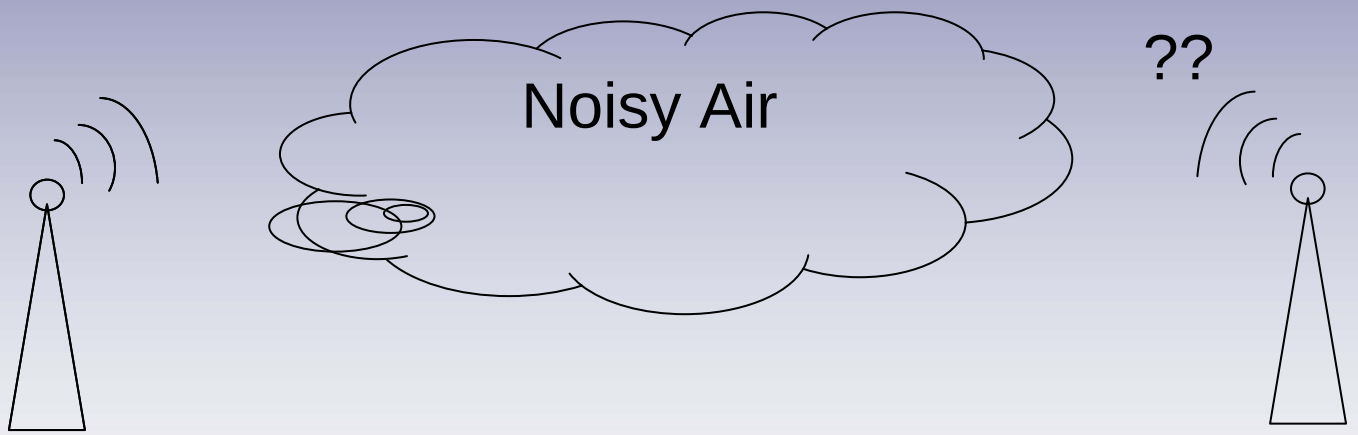
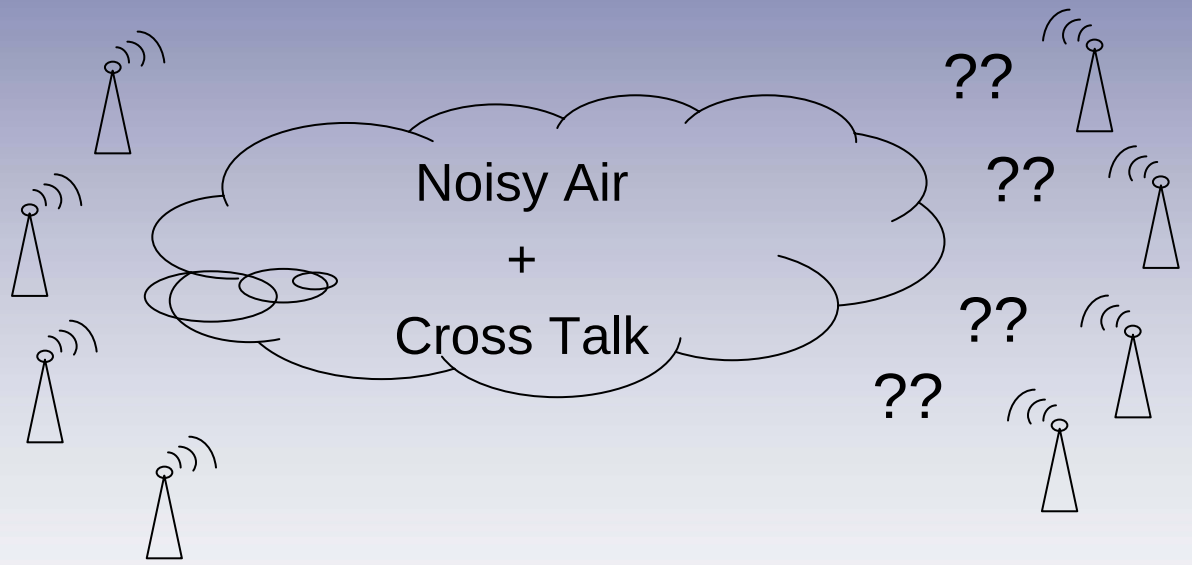
Agenda

- The Challenges on NAND Flash in SSD Applications
- Main Mechanisms of Bit Errors
- Trends and Developments of Error Correcting Code
- Error Distributions
- Efficient BCH Decoding and LDPC Code
- Reliability Issues of Multi-Channel SSD Applications
- Techniques to Improve the SSD Performance
- Conclusion

Flash and Noisy Air



MLC = Noisy Air + Cross Talk ?



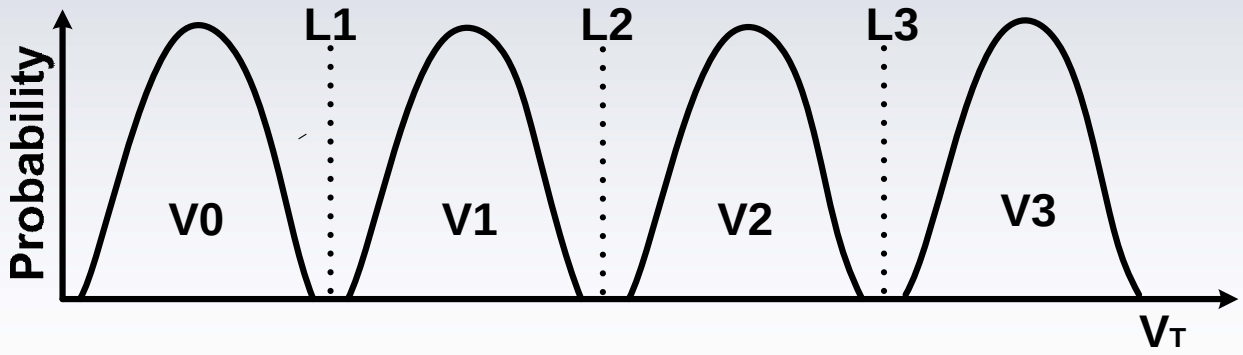
Signal Processing makes quality wireless communication possible

The Challenges on NAND Flash in SSD Applications

- Reliability of NAND Storage cells
- Program/Erase Count dramatically drops
- System stability becomes a critical issue in multi-channel SSD.
- After applying Error Correcting Code, the bit error rate is typically 10^-13 to 10^-16.

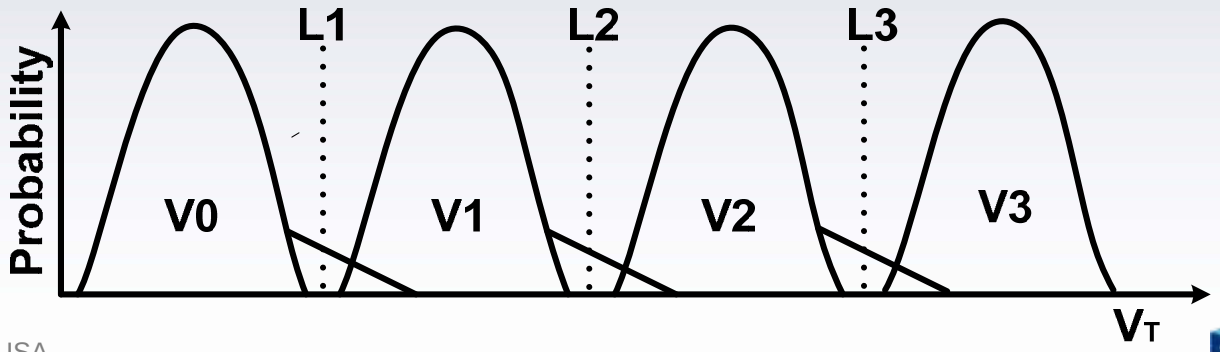
Main Mechanisms of Bit Errors

- Write errors
- Retention errors
- Read-disturb errors
- The following figure shows the distribution of cells in four levels for MLC flash. Bell-shaped curves represent the probability distributions of the four Vt levels.



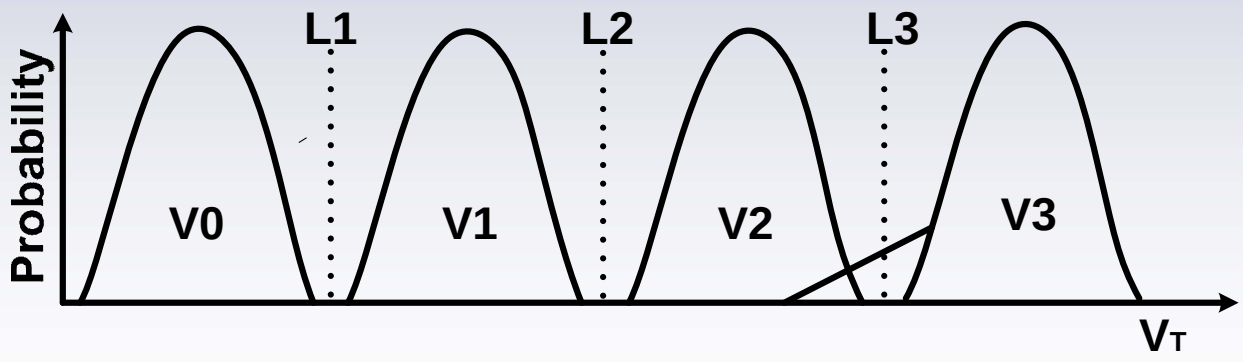
Write Errors

- The overprogramming failures are caused by cells being intentionally programmed to one level but ended up too high.
- Erratic tunneling caused by unstable positive charges.
- The cell may be moved if adjacent cells are later programmed.
- Products from different manufacturers have different occurrence probabilities.



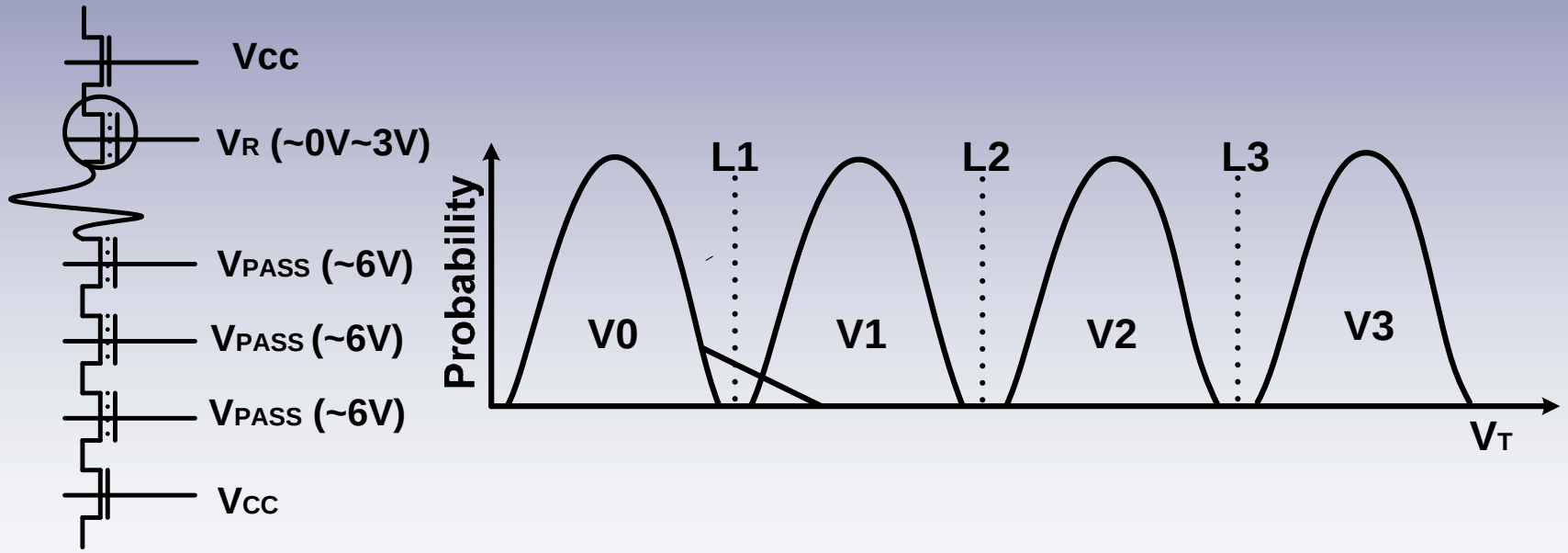
Retention Errors

- Mostly due to charge loss
- Cells lose charge and thus move from one Vt level to the one below.
- Some flash: V3➔V2, and the others: V2➔V1.
- The retention problem can be improved by SMI Intelligent Global Wear Leveling.



Read-Disturb Errors

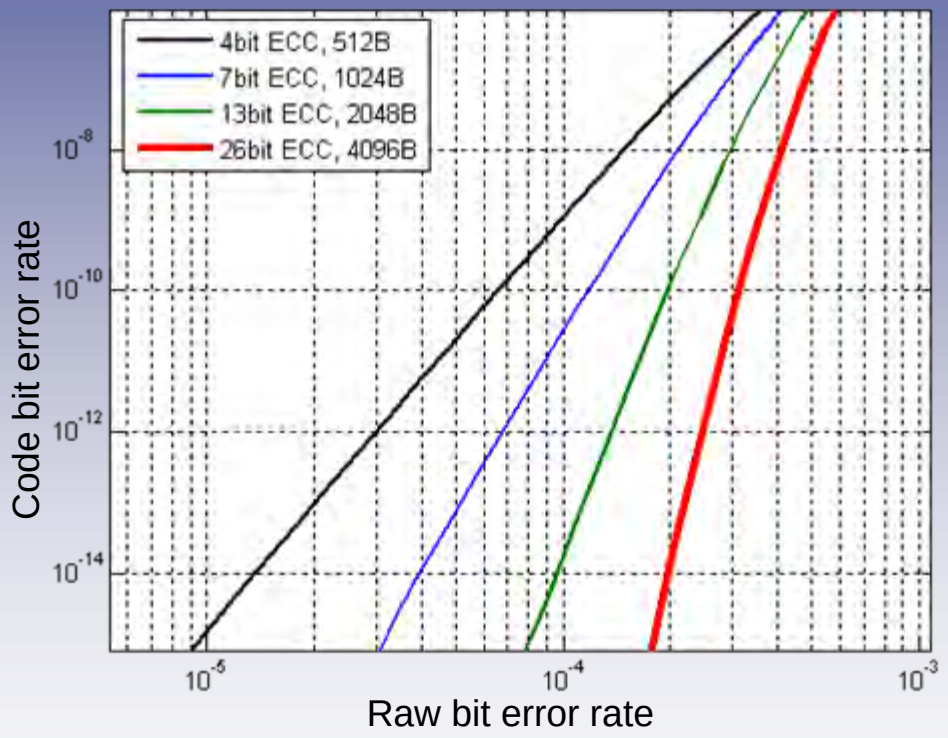
- When a read operation is applied on one cell, the other cell may be regarded as weakly programmed.



Trends and Developments of ECC

- In MLC flash cells, the complex combination of the three main mechanisms leads to partly burst bit errors and partly random errors.
- The ECC types developed are moving from Hamming code (correct fewer errors), RS-code (correct burst errors), to BCH code (correct large random errors).
- In the BCH code, the codeword (CW) length increases from 512B to 1K or 2K Bytes.

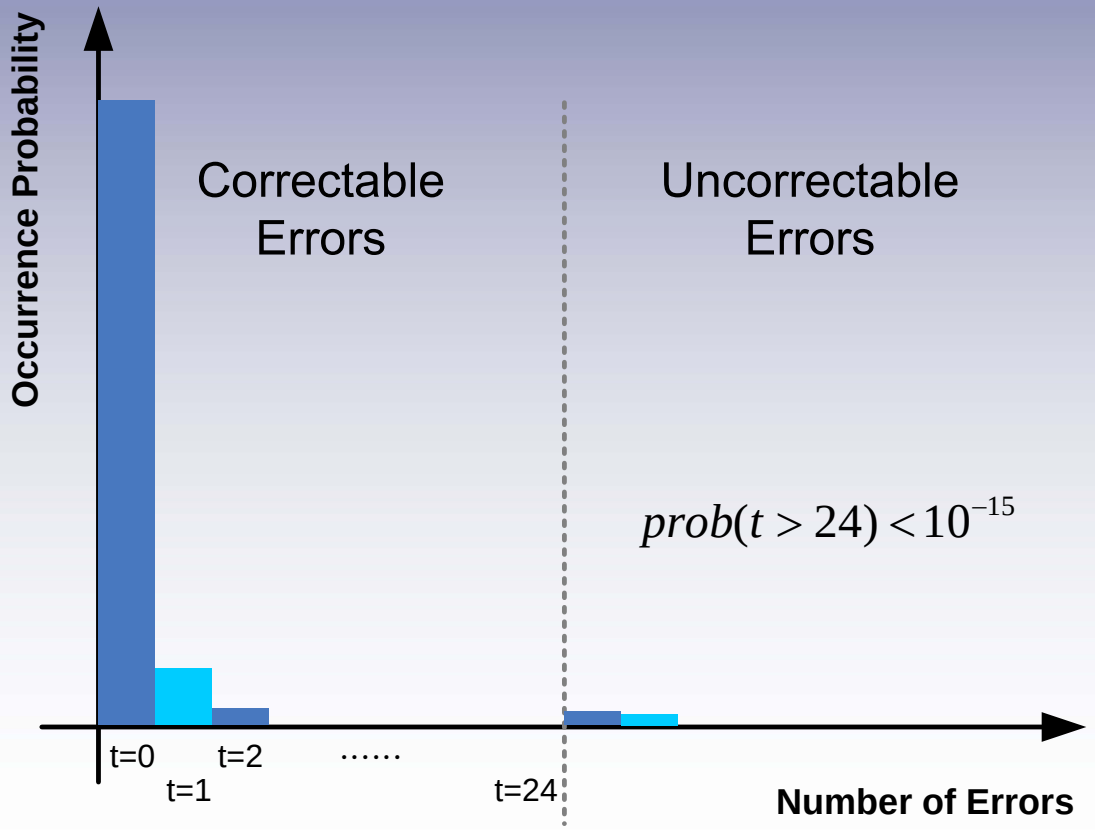
Why Need Larger Data Sector?



- 4K Byte data + 52 Byte-spare:
  - Sector size 4K Byte ➔ 26bit ECC
  - Sector size 2K Byte ➔ 13bit ECC
  - Sector size 1K Byte ➔ 7bit ECC
  - Sector size 512 Byte ➔ 4bit ECC
- The larger the sector size, the better the performance of correction capability.

Error Distributions

- Error Probability Distribution Before/After Applying Error Correction Code

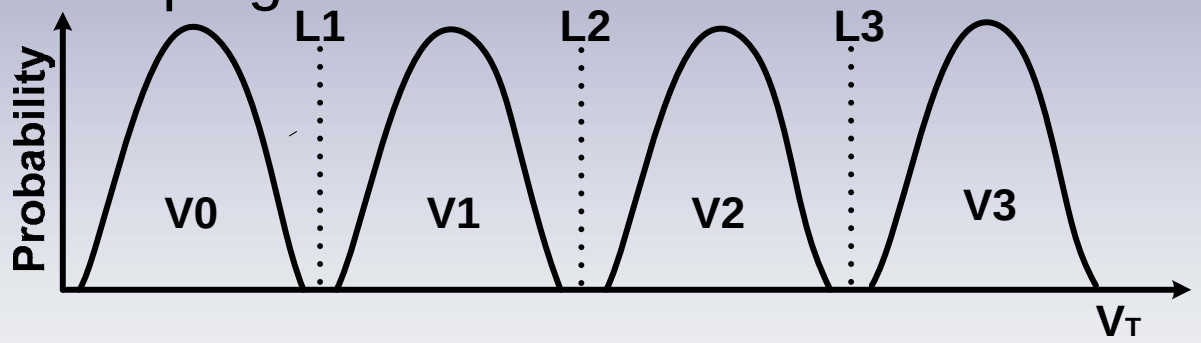


BCH Code good enough?

- The guaranteed error bit correction is important in SSD applications.
- Better BCH Codec
  - Smaller
  - Less power
  - Higher code efficiency
  - Shorter correction time
- SMI can achieve a power-efficient BCH decoder and accelerate the decoding speed in some error cases
  - we only need extra 1000 gate counts to find the error location within 10 cycles.
- But, for future advanced process node flash, is BCH good enough?

More Bad News -- Relationship Between Strong Page and Weak Page

- The error in strong page corresponds to the content in weak page?
- If V3 is a more stable state, we may increase the probability of this programmed state by using the data shaping method.

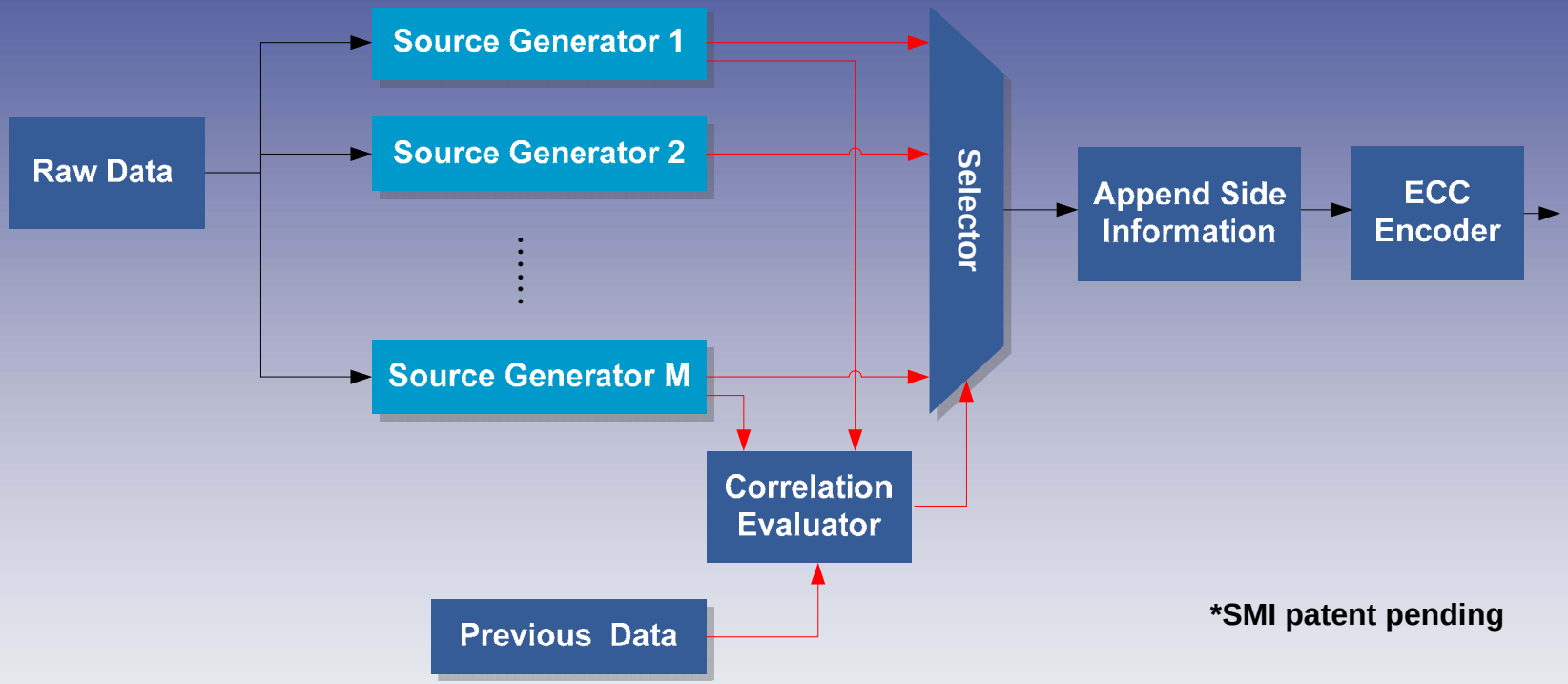


- The right correlation between two CW in strong page and weak page needs a smarter data shaping mechanism.

Techniques to Improve SSD Performance

- Data Shaping
- Faster Correction with Multi-Layer ECC
- Soft Decoding of LDPC
- Dynamic ECC Strategies

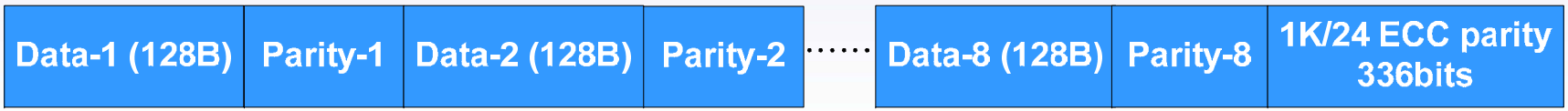
Smarter Data Shaping Algorithm



- Execute the correlation evaluation and select the best generator to increase the system stability.
- The appended side-information can be regarded as an extra redundancy.

Faster Correction with Multi-layer ECC

- As the occurrence rate of correctable CW increases, the error correcting process and data read performance becomes critical to high throughput host interface.
- Code concatenation increases the decoding speed.
- Small sectors share the same large parity group.
- The small sectors can start decoding and correction process before receiving complete CW.
- If only a fewer error bits are distributed in different sectors, it is not necessary to launch the large parity decoding scheme.



Soft-Decision Decoding -- LDPC

- Compared to BCH, the current LDPC (Low Density Parity Check) cannot guarantee such a low error floor by using the hard-decision decoding with the same coding rate.
- Powerful ECC decoding needs soft-decision information because soft-decision decoding improves correction capability

Dynamic ECC Strategies

- The reliability of flash cell varies in a large region as the levels increase.
- Dynamically adjust the ECC capability may increase the data reliability in an efficient way.
- Each channel should have respective data protection strategy, depending on data properties, data importance and the lifetime of flash cell.

Conclusion

- Redundant data may provide further advantages besides of error correction.
- LDPC is one of powerful and high efficiency technologies which may be widely applied in the future SSD applications.
- SMI is one of the manufacturers that can provide the most advanced memory storage technologies.

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