



Session 201

System and Controller Design (Error Correcting Codes)

Thursday, August 13 10:00 – 10:50AM

Chuck Sobey
ChannelScience

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System and Controller Design (Error Correcting Codes)

Nelson Duann, Product Marketing Manager, Silicon Motion

Error Correcting Techniques for Future NAND Flash Memory in SSD Applications

Arul Kumar Subbiah, Design Manager, Arasan Chip Systems

Throughput Driven Architecture for BCH Error Correction Codes

Eitan Yaakobi, Graduate Student, UCSD

Error Correction Coding for Flash Memories

Andy Tomlin, VP Firmware and Software, SandForce

A Closer Look at SSD Data Integrity Requirements

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