

TAS-MRAM Production Ready & Scalable

“From Lab to Fab”

Crocus Technology
August 2009

Comparison to Traditional High Volume Memories

Higher Performance

Lower Performance

Volatile

Non-Volatile

Comparison to Traditional High Volume Memories

Higher Performance

DRAM

SRAM

Lower Performance

Volatile

Non-Volatile

Comparison to Traditional High Volume Memories

Higher Performance

DRAM **SRAM**

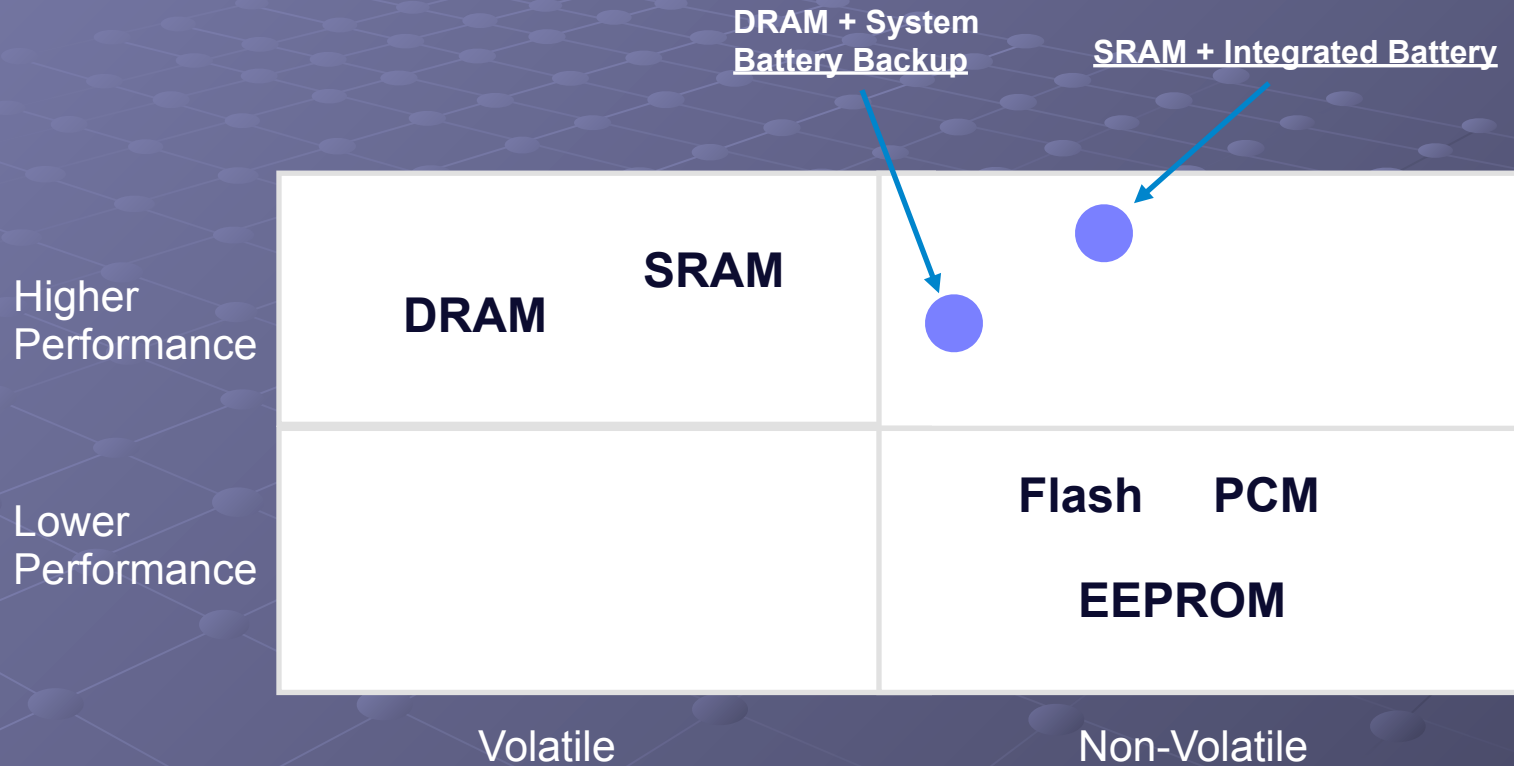
Lower Performance

Flash **PCM**
EEPROM

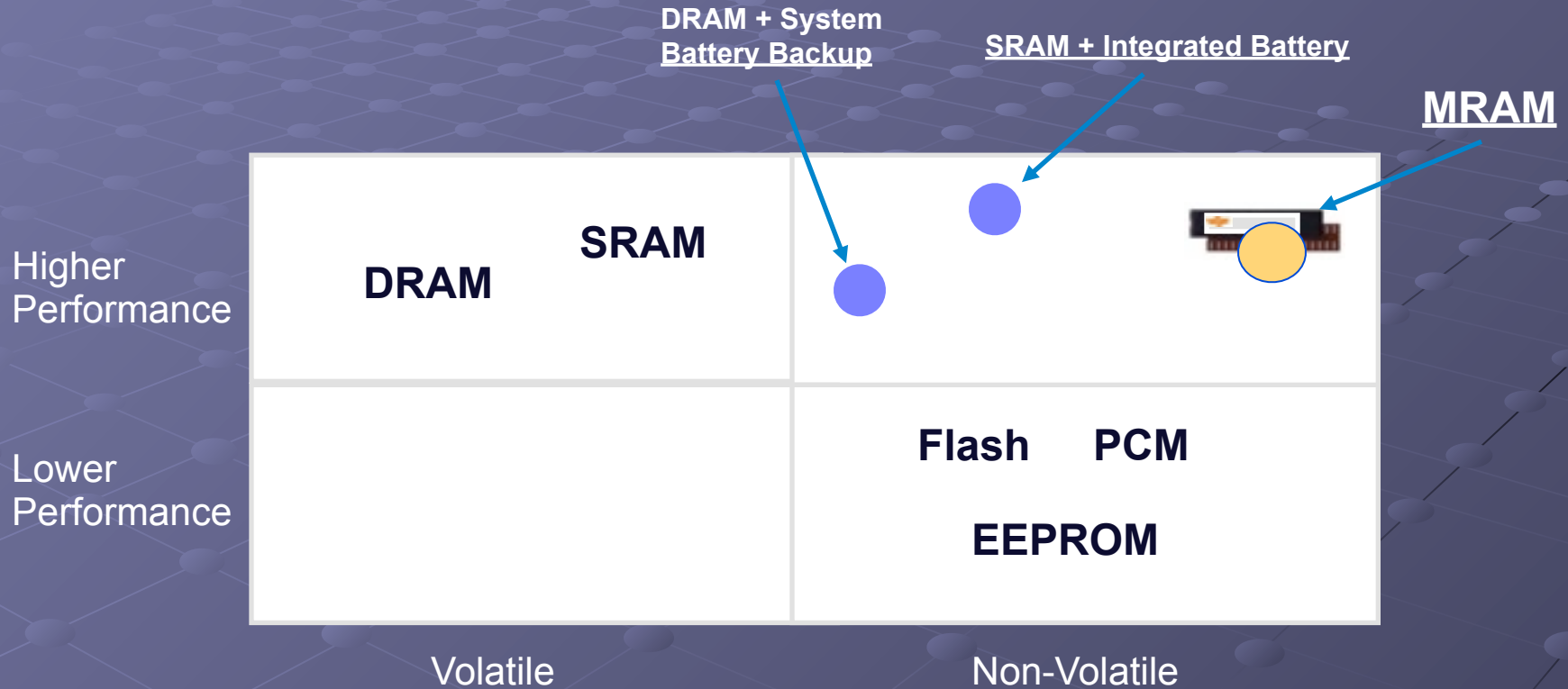
Volatile

Non-Volatile

Comparison to Traditional High Volume Memories



Comparison to Traditional High Volume Memories

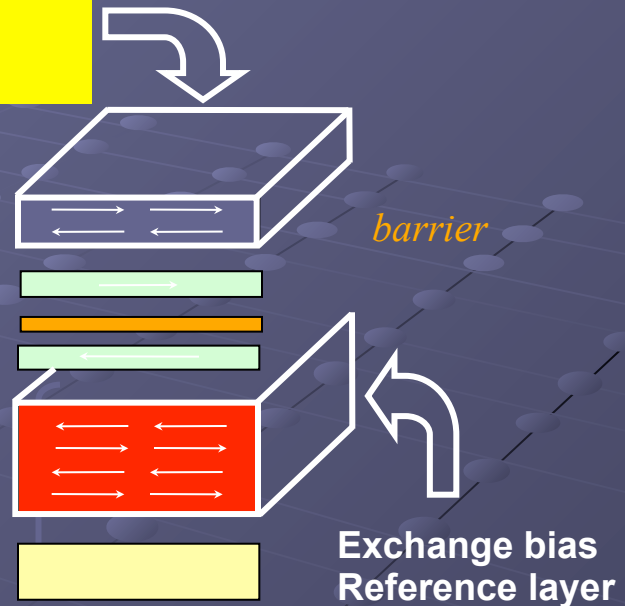
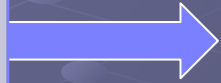


Data is stored in magnetic elements (Magnetic Tunnel Junction - MTJ) vs. stored charge (Flash, DRAM, etc.) or Flip-flop (SRAM)

MRAM Generations

Crocus Innovation:
Exchange biased
storage layer

1 st Generation	FIMS
2 nd Generation Production in 2010	TAS
3 rd Generation Samples in 2010	STT

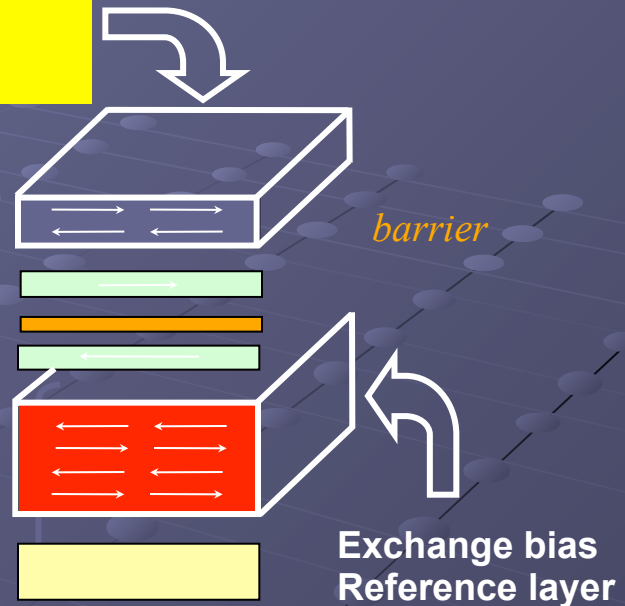
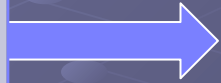


- MANUFACTURABLE
- SELECTIVITY
- STABILITY
- SCALABILITY

MRAM Generations

Crocus Innovation:
Exchange biased
storage layer

1 st Generation	FIMS
2 nd Generation Production in 2010	TAS
3 rd Generation Samples in 2010	STT



- MANUFACTURABLE
- SELECTIVITY
- STABILITY
- SCALABILITY

TAS-MRAM.....Volume production in 2010 on Tower Semiconductor's 130nm CMOS process!!

TAS-MRAM - Discrete

➤ Replacement for BBSRAM, nvSRAM, and FeRAM

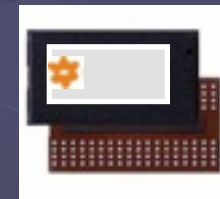
	TAS-MRAM	BBSRAM	nvSRAM	FeRAM
Write Cycle	35ns	70ns-150ns	15ns-45ns	90ns-115ns
Endurance	Unlimited	Unlimited	2×10^5 (store)	10^{14}
Data Retention	10yr	10yr (battery lifetime)	10yr	10yr
Relative Cost	Low	High	Medium	Low

TAS-MRAM - Discrete

➤ Replacement for BBSRAM, nvSRAM, and FeRAM

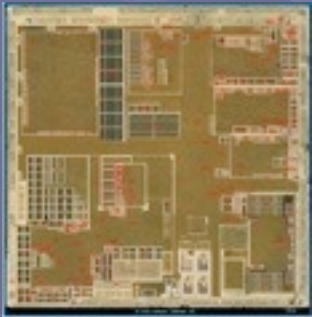
	TAS-MRAM	BBSRAM	nvSRAM	FeRAM
Write Cycle	35ns	70ns-150ns	15ns-45ns	90ns-115ns
Endurance	Unlimited	Unlimited	2x10 ⁵ (store)	10 ¹⁴
Data Retention	10yr	10yr (battery lifetime)	10yr	10yr
Relative Cost	Low	High	Medium	Low

1Mb -256Mb Densities
x8 and x16 Configurations

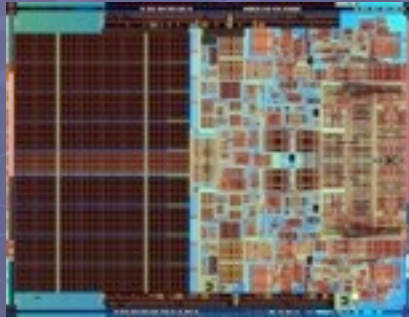


TAS-MRAM - Embedded

➤ Replacement for embedded SRAM and Flash



SOCs with over
150 SRAM macros



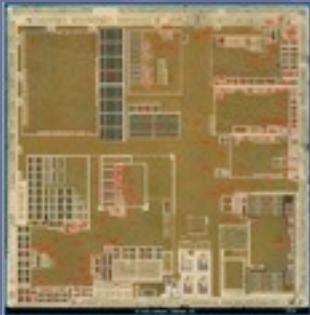
MPUs with L2/L3 caches

30% - 50% of the die area is SRAM
6T SRAM bit cell size is 4x MRAM equivalent

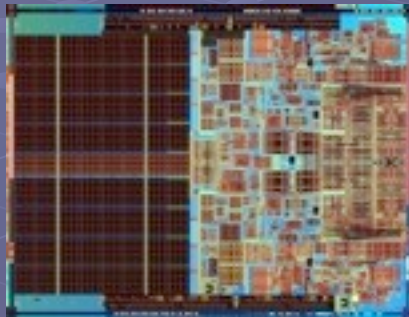
- **TAS-MRAM Benefits over SRAM....**
 - Die size savings of 25% to 38%
 - Power savings - “zero” standby current
 - Non-volatility is bonus

TAS-MRAM - Embedded

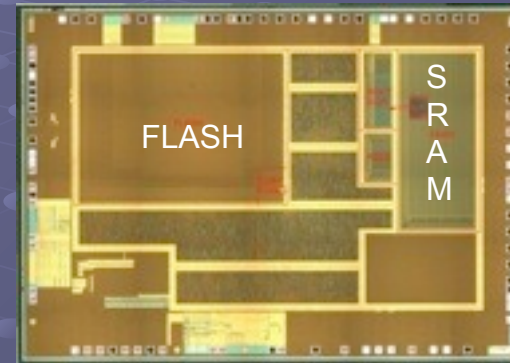
➤ Replacement for embedded SRAM and Flash



SOCs with over
150 SRAM macros



MPUs with L2/L3 caches



32Bit RISC MCU
- 64KB SRAM
- 512KB FLASH

30% - 50% of the die area is SRAM
6T SRAM bit cell size is 4x MRAM equivalent

● TAS-MRAM Benefits over SRAM....

- Die size savings of 25% to 38%
- Power savings - “zero” standby current
- Non-volatility is bonus

● TAS- MRAM Benefits over Flash....

- Faster write – Bit level write
- Higher endurance - No “wear leveling” needed
- Fast wake up - “Instant on”
- Cell size
 - 35f² bit cell
 - <1x circuit overhead
- Process
 - No high voltage / pump charge required
 - 3-4 process steps over CMOS

TAS-MRAM Applications

- Cache Memory
- Buffer Memory
- Data Logging

Wide range of applications !!

- Storage
- Networking
- PC Servers
- POS Terminals
- Advanced Metering
- Cell Phone
- Set top box
- Medical Instrumentation
- Casino Gaming
- Industrial Control
- Aerospace
- Automotive

TAS-MRAM Production Ready & Scalable

- Discrete ICs
- Embedded Memory Blocks
- Technology Licenses
- Foundry Services

For More Information Contact:
Khines@crocus-technology.com

or

650-823-8355