A Novel Embedded OTP Memory Bit Cell Based on Oxide Breakdown

Jim Lipman

Sidense Corp.

Agenda

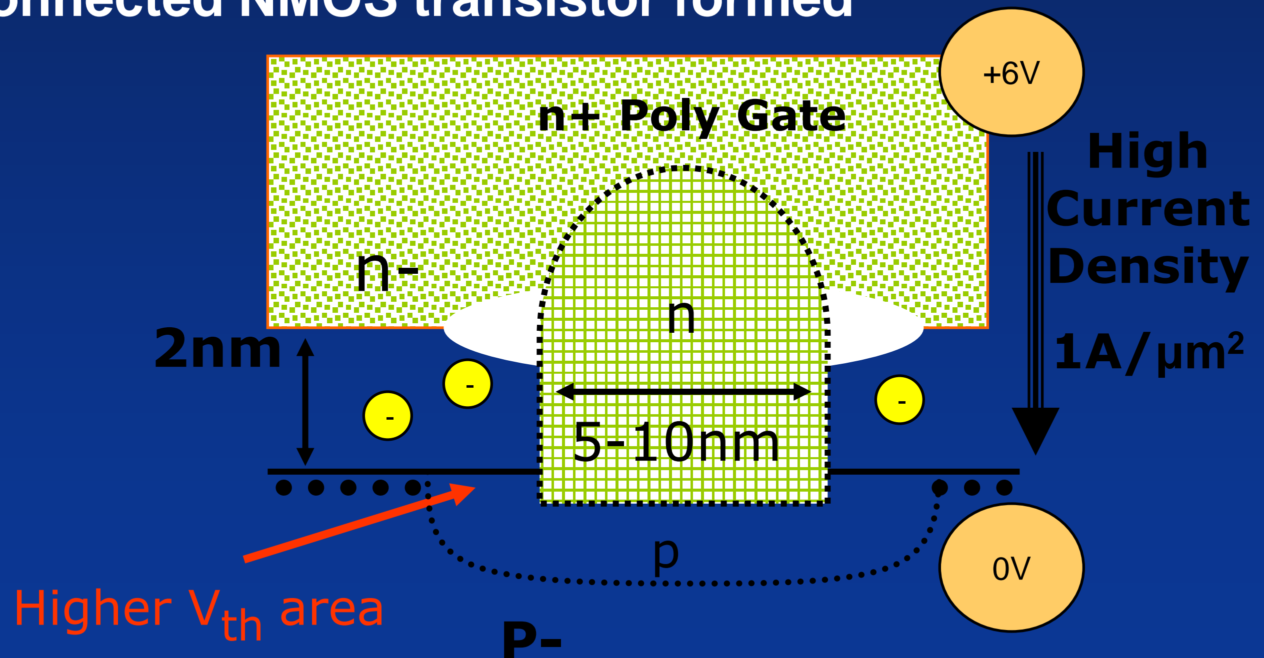
- 1T-Fuse OTP Overview
- Oxide Breakdown Mechanism
- 1T-Fuse Bit Cell
- Scaling
- Performance
- Reliability
- Security
- 1T-Fuse OTP Summary

1T-Fuse OTP Overview

- The bit cell is antifuse-based
- Programmed by predictable, irreversible gate oxide breakdown
- Basic technology around for about 20 years
- Oxide breaks down at ~5-8V
- Gate current increases up to 10,000x
- Standard logic CMOS processes
  - No additional masks or process steps

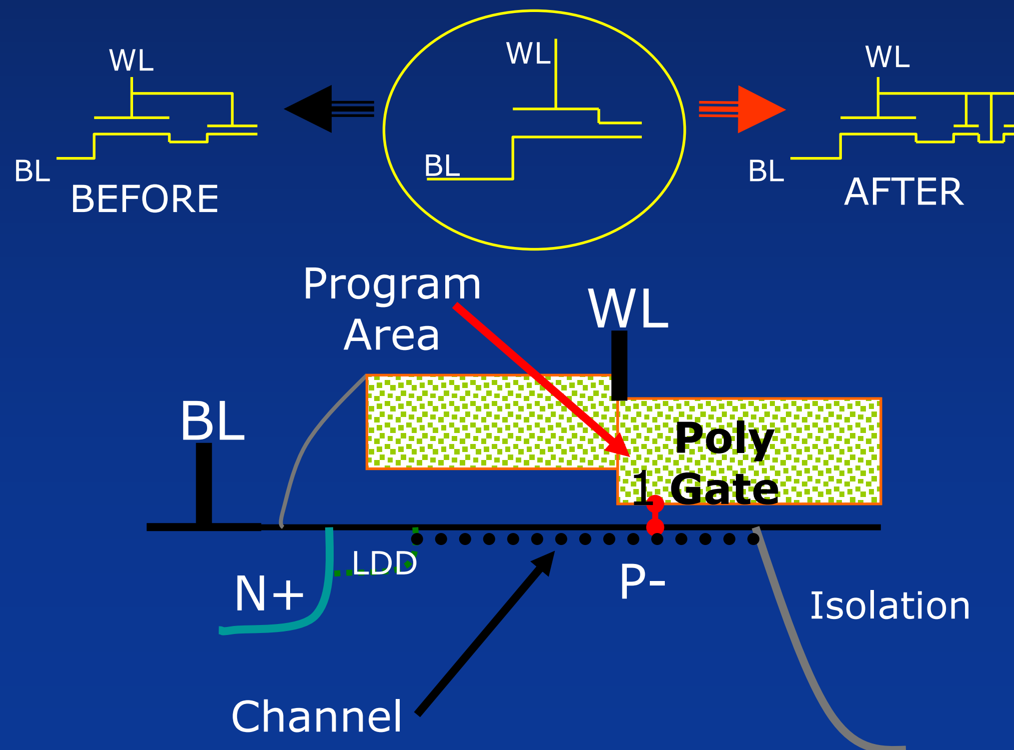
Oxide Breakdown – Nano-Scale Crystallization

- Positive gate voltage → High E field across gate
- Tunneling current → Current increases
- Oxide melts in breakdown region (~1mA/mm^2) in <100ns
- Nanoscale diode-connected NMOS transistor formed



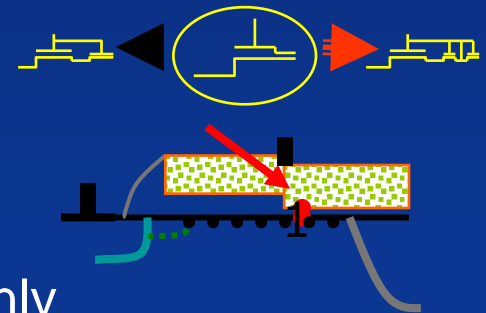
Split-Channel 1T-Fuse™ Bit Cell

- Solution: - remove LDD from breakdown area
  - 1T-Fuse breaks only in the channel area
    - → No channel tail
    - → no dependence on foundry-specific "tweaks"



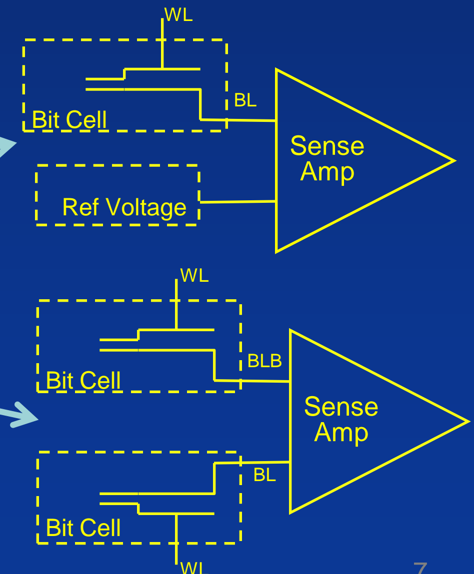
Scaling

- Typical NVM Cell Scaling Problems
  - Process node and foundry dependence
  - Minimum poly gate size
  - Additional fabrication steps
- 1T-Fuse Solution
  - No process node or foundry dependence
    - No LDD or threshold adjustments
  - No critical poly lithography
  - Predictable programming voltage
    - Function of effective oxide thickness only

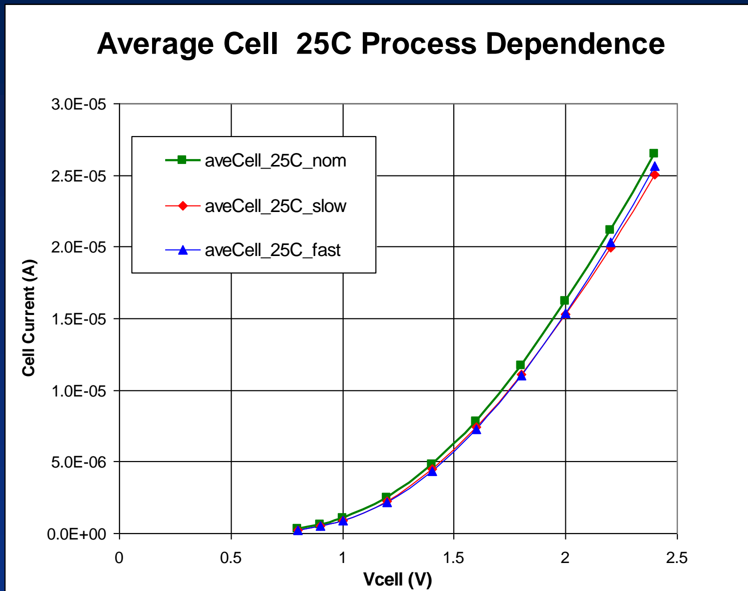


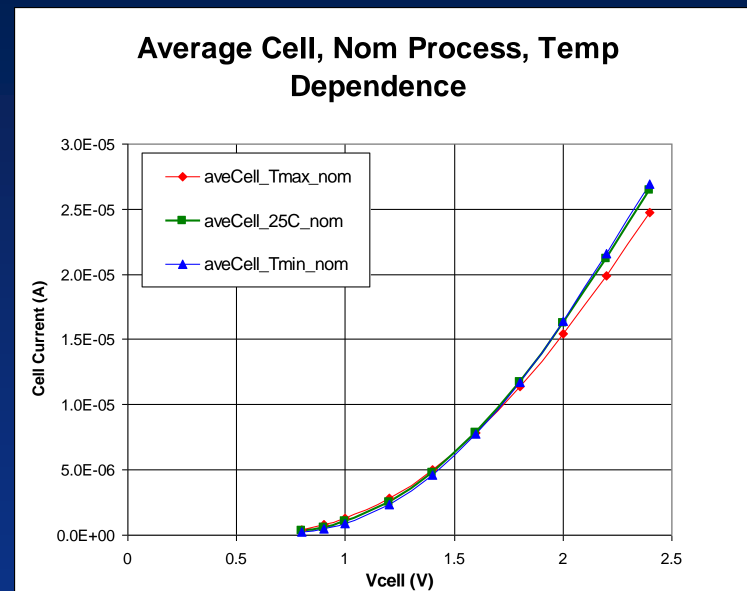
Performance

- Typical NVM Problems:
  1. Temperature Range
  2. Read Power
  3. Area
  4. Speed
  5. Voltage Range
- 1T-Fuse Solutions
  1. No Temperature sensitivity
  2. Minimal read power, no cell current flow
  3. Single-ended read = Small Area
  4. Differential = Fast Access
  5. Differential = Wide Voltage Range



Process/Temperature Sensitivity





No Fast/Slow Process Sensitivity

No Temperature Dependence

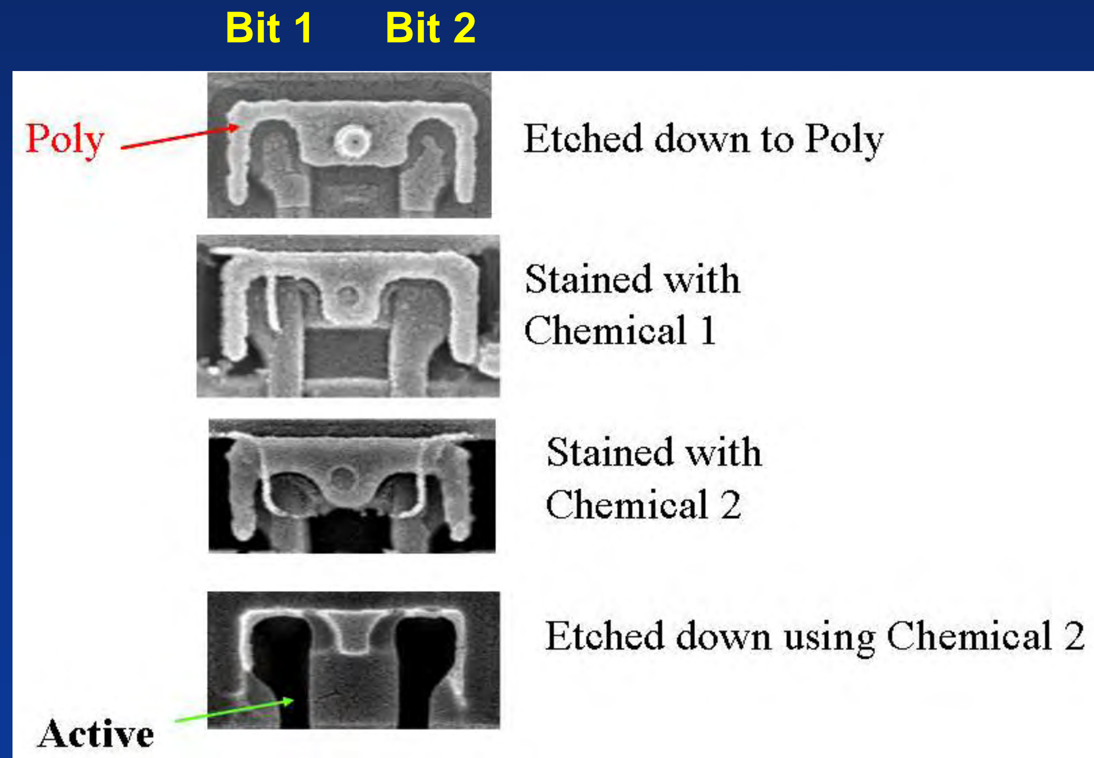
Reliability

- Typical NVM problem
  - Retention at High Temp
- 1T-Fuse Results
  - Multiple Foundries and Nodes
    - **125C AHTOL – 4 ½ million Mbit-**hours PASS (no failures)
    - **150C HTS – 4 million Mbit-**hours PASS (no failures)
  - **TDDB** testing used to predict retention
    - > 20 years at maximum read voltage at 125C with 50% duty cycle
    - > 100 years at 150C in differential mode

What About Bit Cell Security?

- 1T-Fuse:
  - Does not depend on charge storage
  - Extremely difficult to reverse engineer

Bit 1 **Bit 2**



1T-Fuse OTP Summary

- Very small, fast and reliable OTP bit cell
- Programming mechanism is irreversible oxide breakdown
- No additional masks or process steps needed
- Broad foundry and process node coverage
- Scalable to 32/28nm and below