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GRANDIS
Pioneer in STT-RAM Technology

Non-volatile STT-RAM: A True Universal Memory

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Outline

- Grandis Corporation Overview
- Current Flash Challenges
- What is Grandis STT-RAM*?
- Grandis STT-RAM Chip
- Memory Technology Comparison
- Grandis STT-RAM Roadmap
- Summary

***STT-RAM: Spin Transfer Torque Random Access Memory**

Grandis Corporation Overview

- **Grandis develops and licenses STT-RAM proprietary NVM solutions**
  - Grandis' STT-RAM enables a wide variety of low-cost and high-performance memory products at the 45 nm technology node and beyond
- Headquarters: Silicon Valley, California
- R&D Offices: California, Japan, S. Korea
- Strong & broad STT-RAM patent portfolio and know-how
  - 50 Granted U.S. Patents
  - > 46 U.S. Patents Pending

Our mission is to establish Grandis STT-RAM as the #1 choice for memory solutions beyond 45 nm

Grandis Milestones in STT-RAM

- **2002:** Grandis files first key patents in STT-RAM
- **2004:** Grandis reports world's first STT switching in MTJs
- **2005:** Renesas Technology licenses Grandis' STT-RAM technology
- **2007:** Grandis receives Technology Innovation Award from Frost & Sullivan
- **2008:** Hynix Semiconductor licenses Grandis' STT-RAM technology

  Grandis wins large DARPA grant to develop STT-RAM chips
- **2009:** Grandis upgrades MTJ Fab to handle 300 mm customer wafers

  Grandis awarded 9 key patents, taking U.S.-granted patent total to 48

Grandis Development Partners

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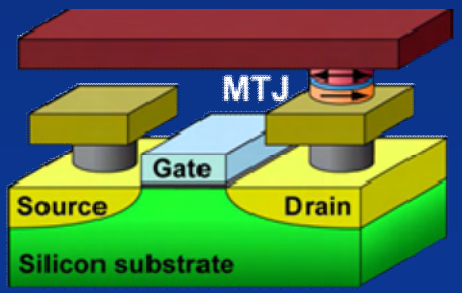
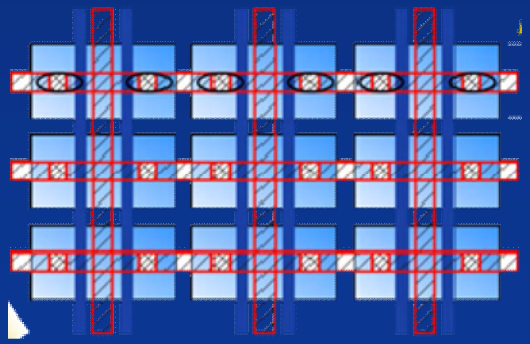
Grandis STT-RAM IP Position

- Strong & broad STT-RAM IP coverage
  - Fundamental patents
  - Practical implementation patents
  - Intensive and in-depth know-how and trade secrets

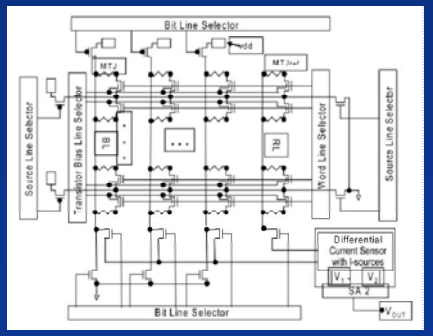
>96 patents filed, 50 patents granted since 2002



Innovative MTJ materials, stacks and cell architecture



STT-RAM array architecture and memory design



Circuit design and system applications

Current Flash Challenges

- Flash memory evolution
  - High capacity and low cost, 2, 3 & 4 bit MLC
  - Large page size, increased resource for block management
  - Aggressive scaling, reduced performance and reliability
  - Meeting endurance target becomes more difficult

  These problems create an opening for an alternative, high density Non-Volatile Random Access Memory

- Grandis STT-RAM will be the solution within 2 years
  - Initially, embedded SRAM & low power mobile RAM replacement
  - In medium term, NOR flash & DRAM replacement
  - Ultimately, a storage class memory that can replace NAND & HDD

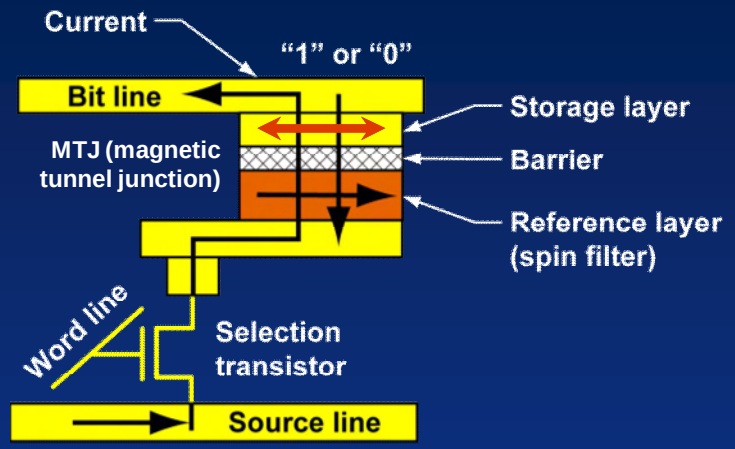
What is Grandis STT-RAM?

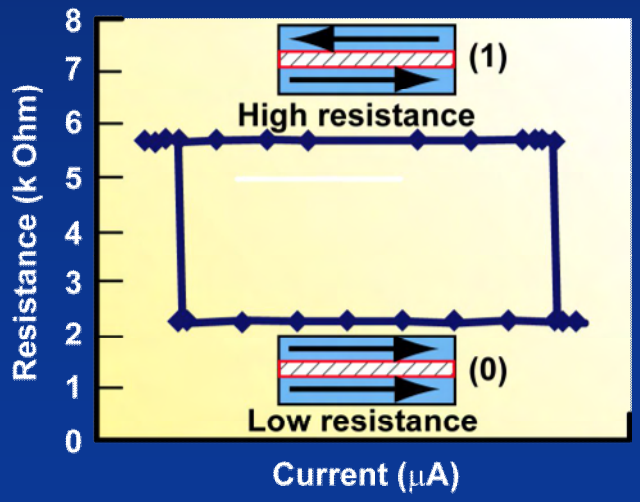
- An evolution in magnetic storage from disk drives to solid-state semiconductor memory
  - Uses spin-polarized current ("spintronics") to write magnetic bits
  - Non-volatile, random-access memory with no moving parts
  - Key building block is the magnetic tunnel junction (MTJ)

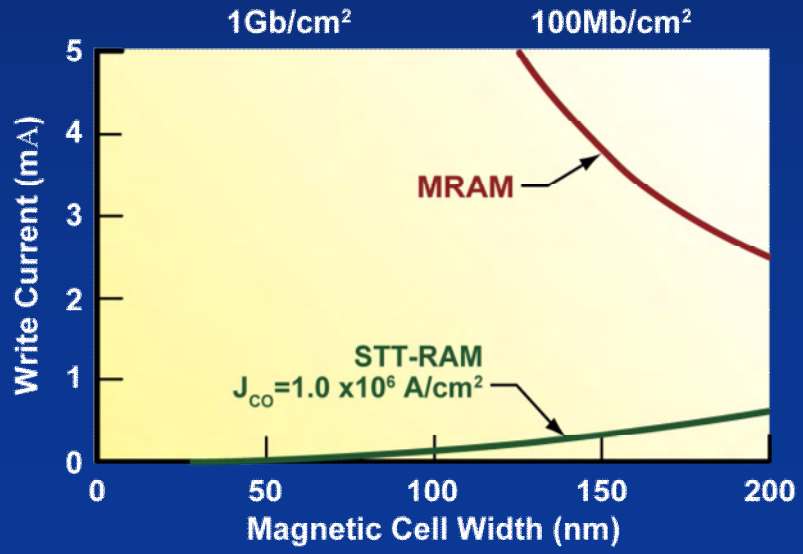
Grandis has been the pioneer in STT-RAM development since its founding in 2002

STT Write Mechanism

- Spin-transfer torque writing
  - Uses spin-polarized current instead of magnetic field to switch magnetization of storage layer
  - Has low power consumption and excellent scalability

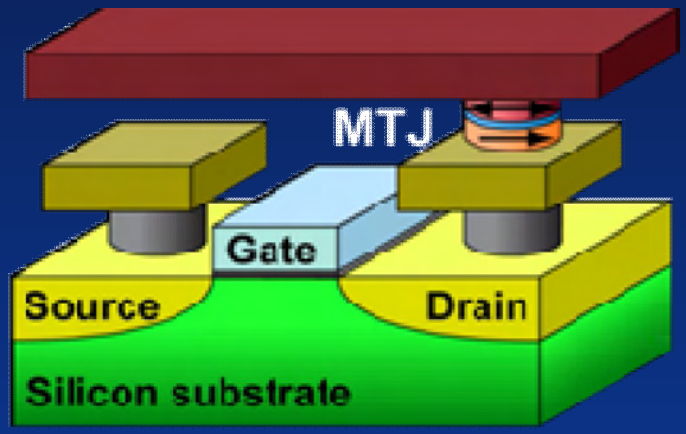






STT-RAM Universal Memory

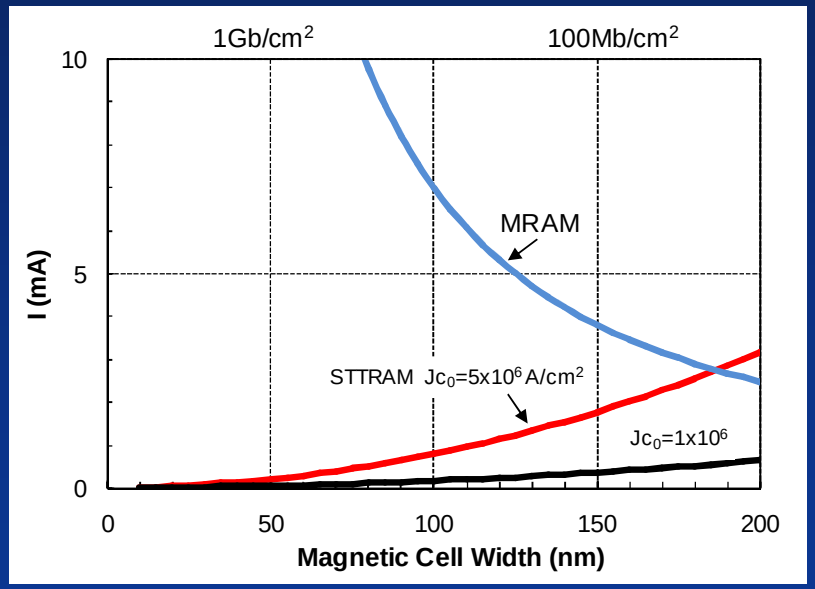
- STT-RAM characteristics
  - Non-volatile
  - Highly scalable
  - Low power consumption
  - SRAM read/write speed
  - Unlimited endurance
  - DRAM & Flash density (6 F2)
  - Multi-level cell capability

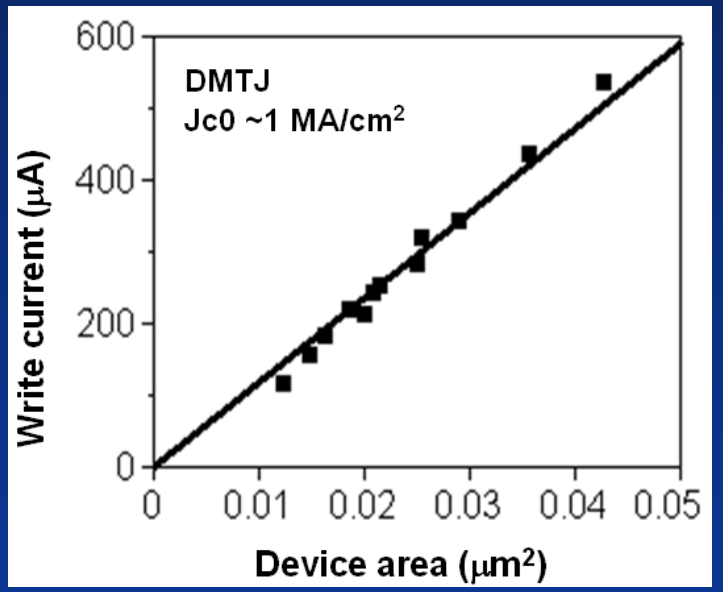


STT-RAM uses existing CMOS technology with 2 additional masks and less than 5% cost adder

STT-RAM Scalability

- Compared to conventional MRAM, STT-RAM cuts write current by more than one order of magnitude (>10×)

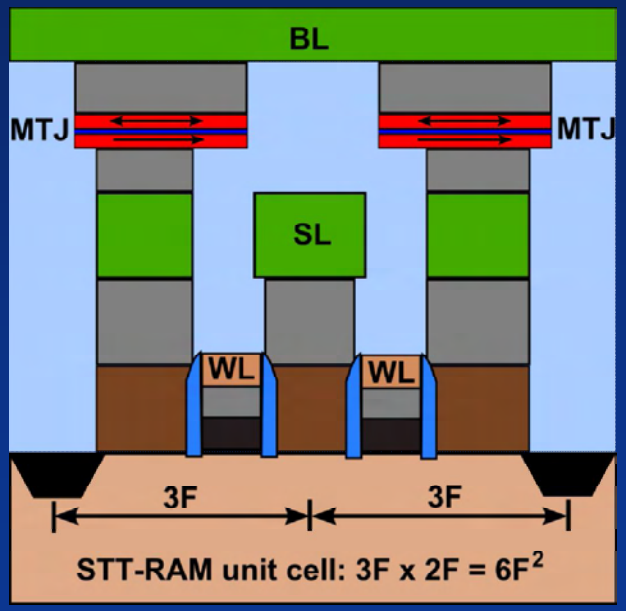


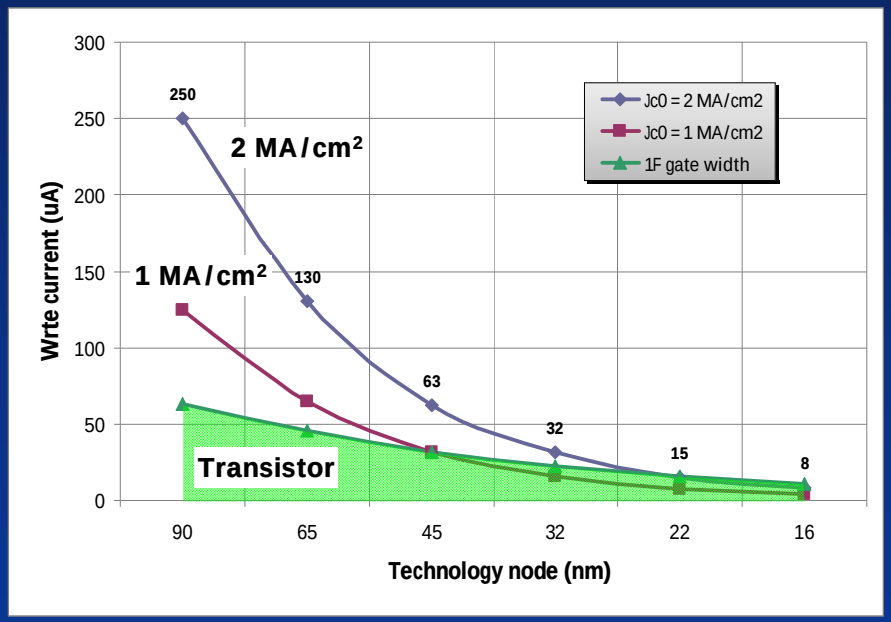


- STT-RAM write current scales linearly with device area
  - <150 μA write current at 90 nm, <50 μA at 45 nm

STT-RAM Minimum Cell Size

- 6 F^2 minimum cell size with shared source line architecture
  - Minimum 1 F gate width transistor can drive 6 F^2 cell beyond 45 nm





- Future multi-level cell and cross-point architectures will enable further scaling beyond 6 F^2

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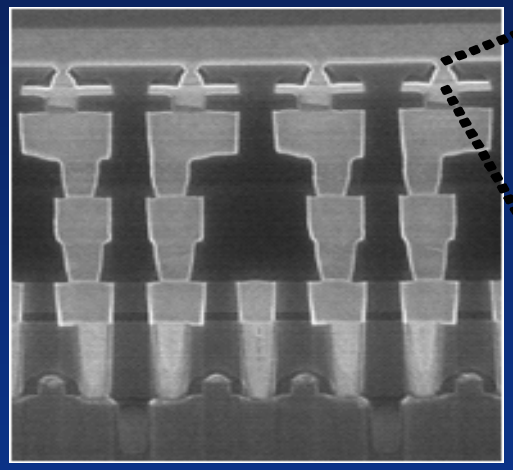
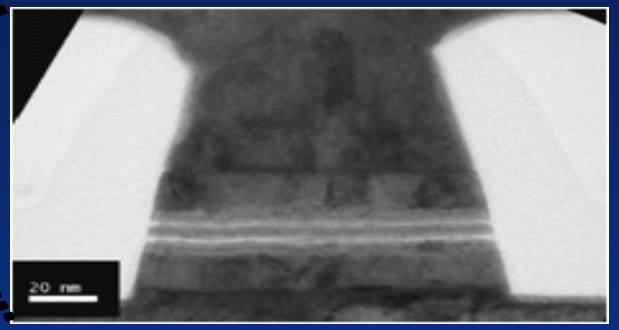
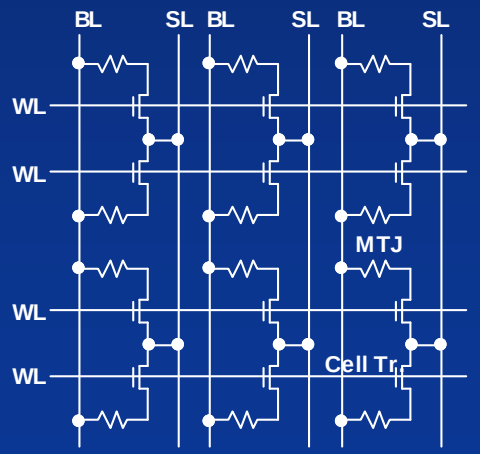
Grandis STT-RAM Chip

- The most advanced STT-RAM prototype chip in the industry

- **Fully-functional**
- **256 kbit capacity**
- **90 nm CMOS**
- **4 Cu metal process**
- **LP high reliability CMOS**
- **Write current <200 µA**
- **Write/read speed 20 ns**
- **Endurance >10^{13}**



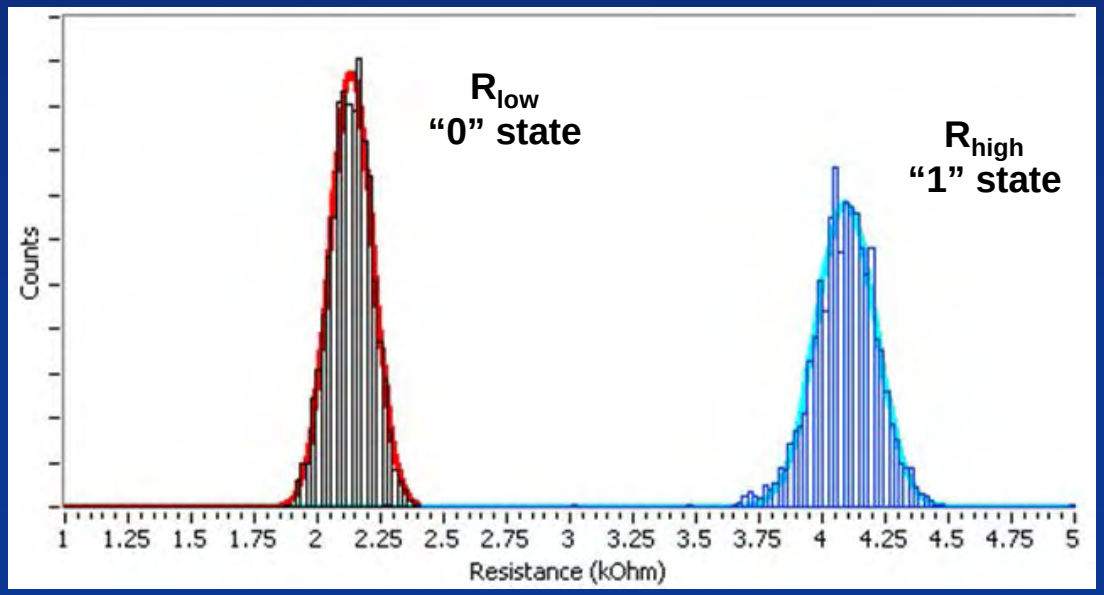




- Higher density chips at 54 nm & beyond are in development

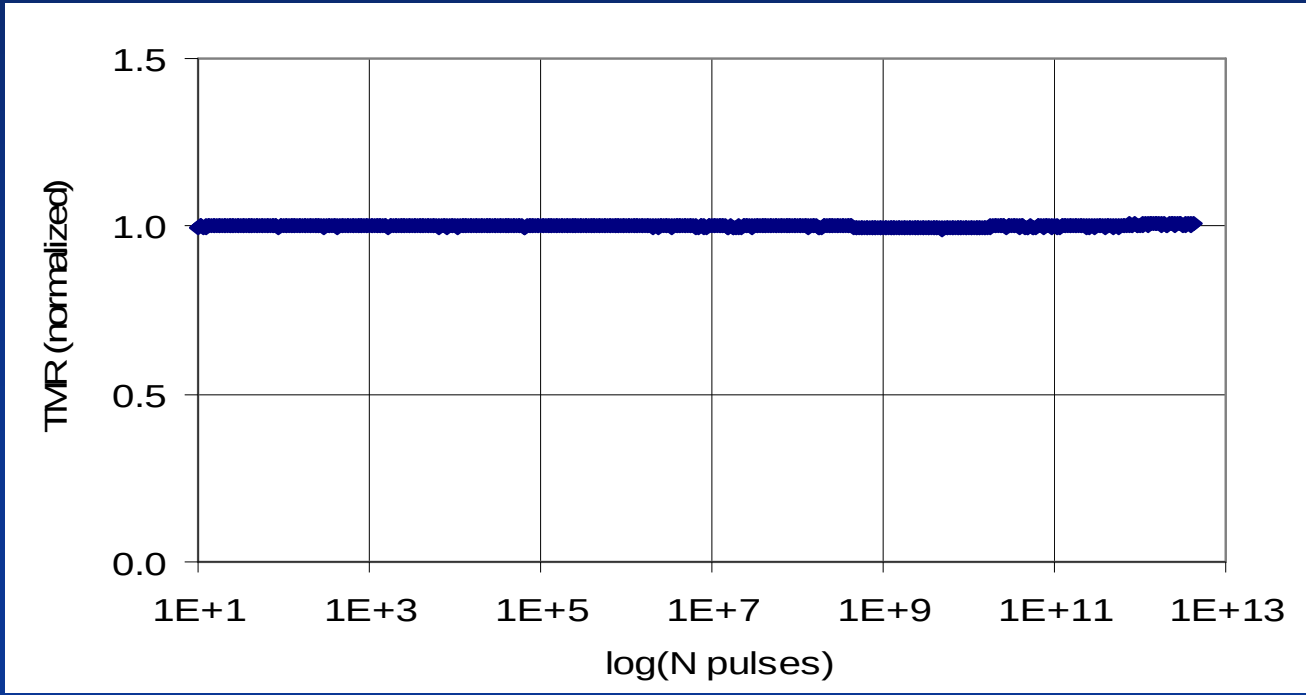
STT-RAM Resistance Distribution

- Large separation between resistance states and small process distribution provide excellent read characteristics
  - TMR (Tunneling Magnetoresistive) signal ~100%
  - Rlow distribution sigma 4% (1σ), Rhigh distribution sigma 3% (1σ)
  - Rhigh – Rlow separation = 20σ



STT-RAM Unlimited Endurance

- Unlimited (>10^{15}) write endurance projected from TDDB tests with stressed voltage and temperature
  - 10^{13} endurance demonstrated to date under real operating conditions



Memory Technology Comparison

	SRAM	DRAM	Flash (NOR)	Flash (NAND)	FeRAM	MRAM	PRAM	RRAM	STT-RAM
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Cell size (F^2)	50–120	6–10	10	5	15–34	16–40	6–12	6–10	6–20
Read time (ns)	1–100	30	10	50	20–80	3–20	20–50	10–50	2–20
Write / Erase time (ns)	1–100	15	1 μs / 10 ms	1 ms / 0.1 ms	50 / 50	3–20	60 / 120	10–50	2–20
Endurance	10^{16}	10^{16}	10^5	10^5	10^{12}	$>10^{15}$	10^8	10^8	$>10^{15}$
Write power	Low	Low	Very high	Very high	Low	High	High	Low	Low
Other power consumption	Current leakage	Refresh current	None	None	None	None	None	None	None
High voltage required	No	3 V	6–8 V	16–20 V	2–3 V	3 V	1.5–3 V	1.5–3 V	<1.5 V
	Existing products						***Prototype***		

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Intensified interest in STT-RAM

- **Apr. 2008:** Hynix licenses Grandis' STT-RAM technology, expects to sample 1 Gbit STT-RAM in 2010

hynix

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- **Jun. 2008:** Toshiba announces plans to develop 1 Gbit STT-RAM, expects it to replace DRAM by 2015

TOSHIBA
Leading Innovation

- **Jun. 2008:** Korea Government invests $50M in Hynix, Samsung and local university alliance for STT-RAM development

hynix

SAMSUNG

- **Oct. 2008:** Grandis wins large DARPA grant from U.S. government to develop STT-RAM chips

BRIDGING THE GAP
DARPA
50 YEARS
POWERED BY IDEAS

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- **Oct . 2008:** Toshiba presents data from 50 nm perpendicular MTJS, expects STT-RAM to achieve 6F2 cell size (same as DRAM)

TOSHIBA
Leading Innovation

- **Oct . 2008:** Samsung presents 512 Mbit STT-RAM in 90 nm process, expects it to replace DRAM at sub-30 nm in 2012

SAMSUNG

- **Dec. 2008:** IBM–TDK alliance reports statistical study of MTJs for high-density STT-RAM at IEDM conference

IBM

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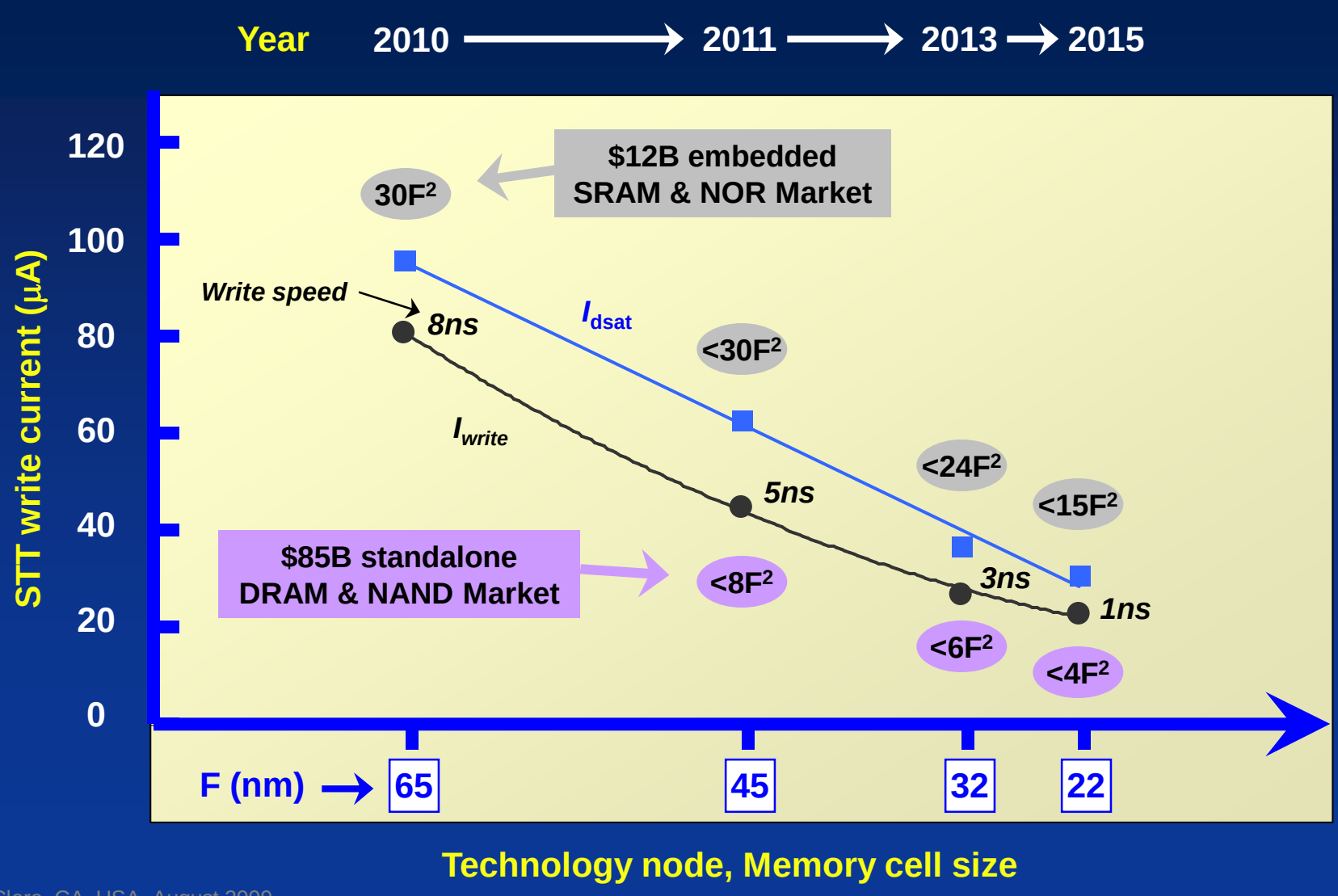
Grandis STT-RAM Roadmap



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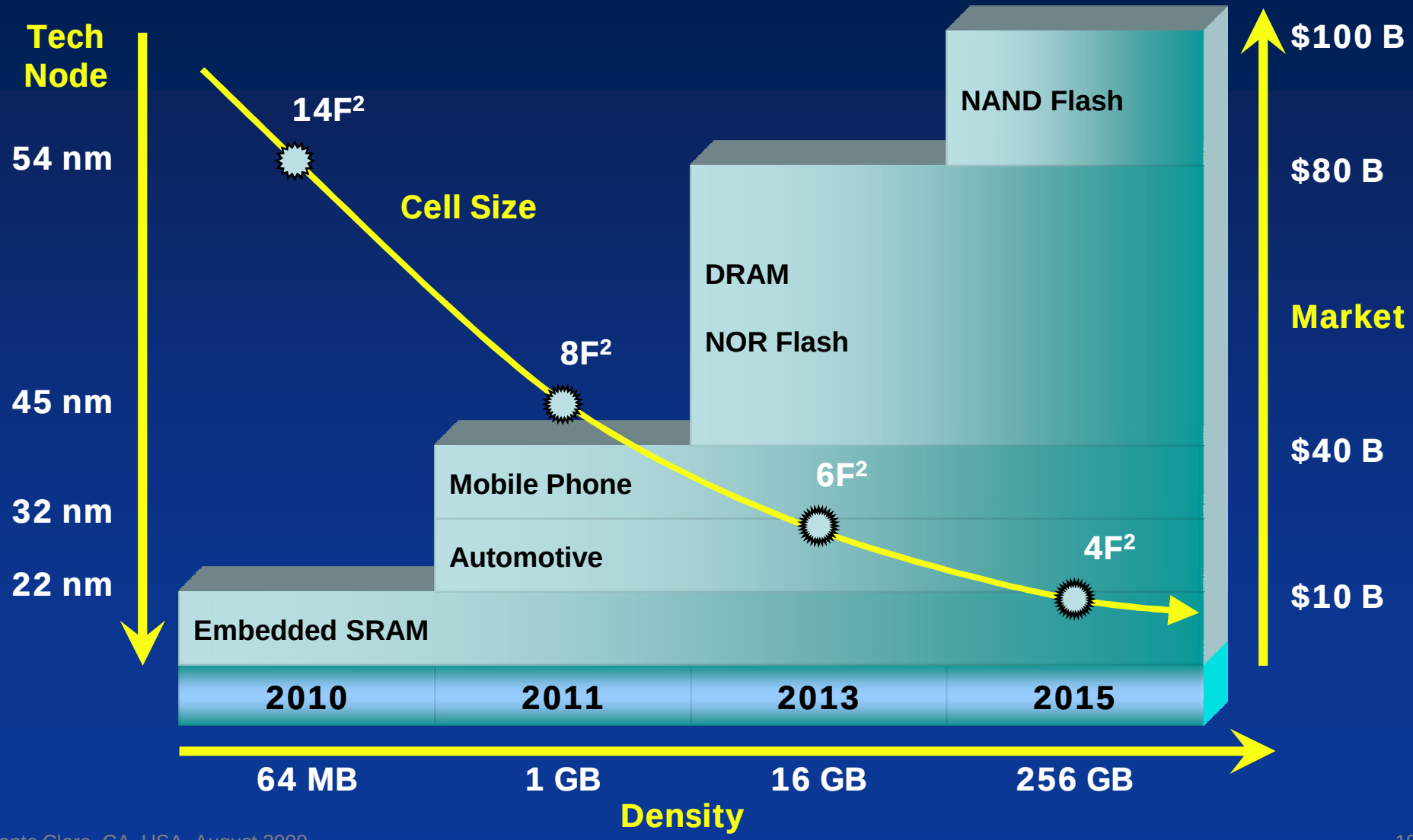
STT-RAM Evolution and Market



Challenges for STT-RAM

- Grandis is working with its partners to address key challenges for STT-RAM
  - Proving technology reliability for large scale manufacturing
  - Tuning cell design for different application requirements

- But to fully exploit STT-RAM's characteristics, a fundamental rethink of computing system architecture will be required
  - STT-RAM can enable revolutionary advances in latency, bandwidth, reliability and power-efficiency for data-intensive applications, and other applications not yet envisaged

The return on investment towards reducing overall system cost and added system functionality well justifies the effort to meet the above challenges

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Summary

- Spintronics (spin electronics) is a rapidly emerging field
  - It will have a significant impact on technology in the 21st century
- STT-RAM is the world's first truly universal, scalable memory technology
  - It will enable a new era of instant-on computers and high-speed portable devices with extended battery life
- STT-RAM has a huge potential market
  - It can replace eSRAM & eFlash, at 45 nm, DRAM at 32 nm, and ultimately replace NAND & HDDs as a storage class memory at 22 nm and beyond

Grandis is the pioneer in STT-RAM with a strong & unique IP position, an experienced and dedicated team, and early partnerships in product development with key semiconductor memory players

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Thank You !

Please visit

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