A Novel Embedded OTP Memory Bit Cell Based on Oxide Breakdown

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Summary Statement

Some of the most useful and profitable ideas have been ones that have taken a perceived deficiency in one product and used it to great advantage in another. A classic example is the 3M Post-it note, which uses cement that was originally developed as a strong adhesive but was not strong enough.

The semiconductor industry has its own version of a shortcoming turned into an advantage – the deployment of oxide breakdown as a non-reversible, reliable and secure programming mechanism for non-volatile memory bits. Deliberate oxide breakdown is the mechanism behind an OTP bit cell that offers several collective advantages over floating gate and other OTP/MTP architectures.

This paper will describe a split-channel OTP bit-cell architecture based on predictable and irreversible thin-oxide breakdown that is at the heart of a field-programmable, very small, highly secure, and very reliable embedded memory that does not require any additional masks or process steps when implemented in a standard-logic CMOS process. The bit-cell is scalable down to 40nm and below.

Author Biography

Jim Lipman is Director of Marketing at memory IP provider Sidense. Prior to Sidense, Jim worked at Cain Communications as Vice President of Client Services, TechOnLine as Content Director, and at EDN Magazine as ASIC and EDA Editor. He also was employed by VLSI Technology, where he held various training, marketing and public relations positions, and has done chip designs at both Hewlett-Packard and Texas Instruments earlier in his career.

Jim received his BSEE and MSEE degrees from Carnegie-Mellon University in Pittsburgh and his Doctorate in Electrical Engineering from Southern Methodist University in Dallas. He also has a Masters of Business Administration from Golden Gate University in San Francisco. Jim is a senior member of the IEEE.