Five Key Steps to High-Speed NAND Flash Performance and Reliability

Presenter

Bob Pierce

cādence®

NVM Performance Trend

Performance (vertical axis)

Device Cost (horizontal axis)

PCM

ONFi 2
Toggle
DDR SLC

ONFi 2
Toggle
DDR MLC

Async SLC

Corrected NAND

MMC

Async MLC

cādence®
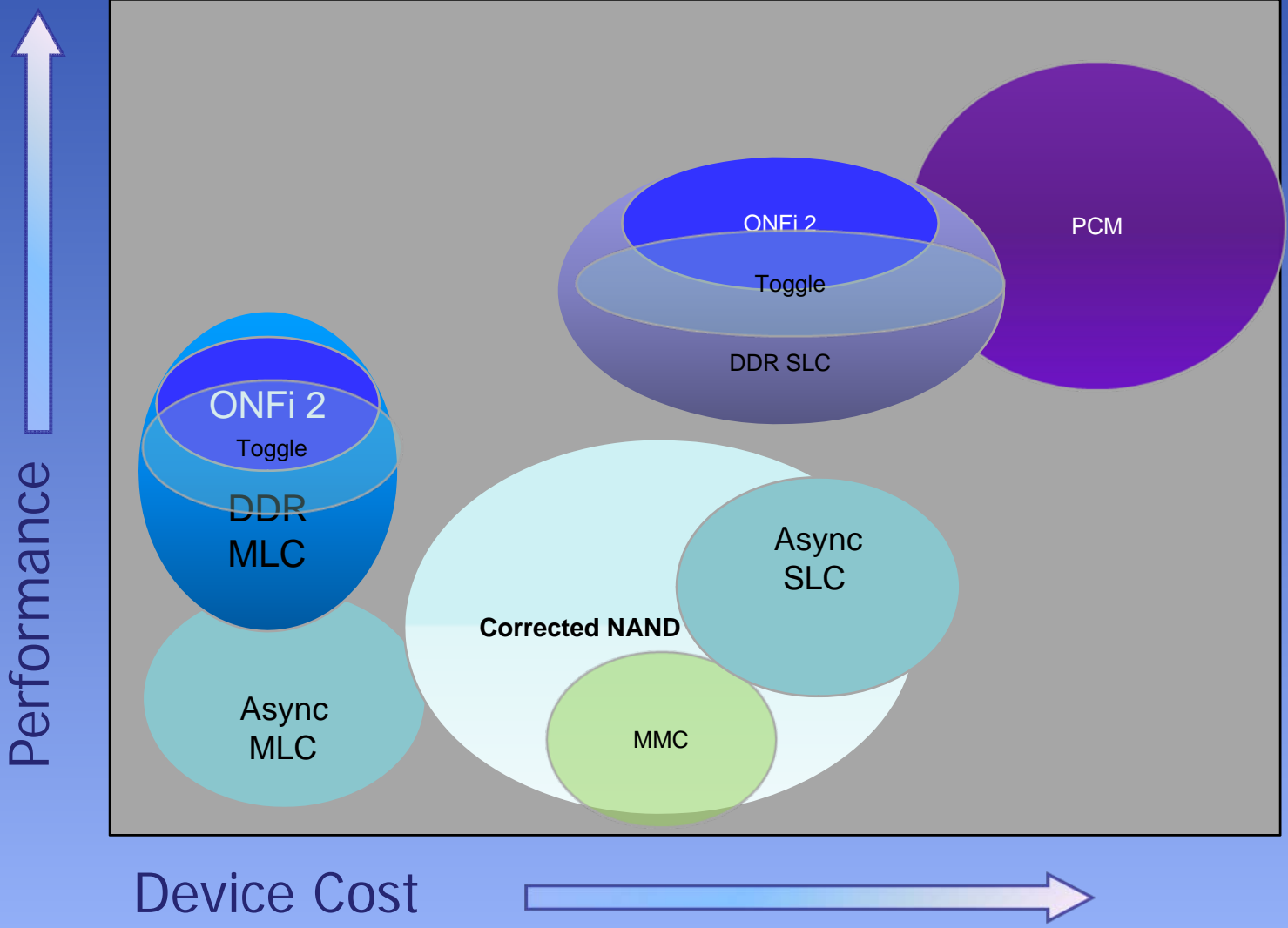
Five Keys to obtaining NAND Reliability and Performance

1. Device commands and parameters
2. Interface
3. Error correction
4. Architecture
5. Software, hardware tradeoffs

Keys to Flash Device Performance

- Page Size increases
  - 2,4,8 K page size What is the impact to bit growth and addressing?
- Read, Write Cycles have been pretty stable
  - From 30 to 6 nsec range
- Key Timing Parameters
  - Trc, Twc, Tprog, Tr, Tbers

cadence®

Critical Timing of NAND Flash

Timing Trend of NAND Flash
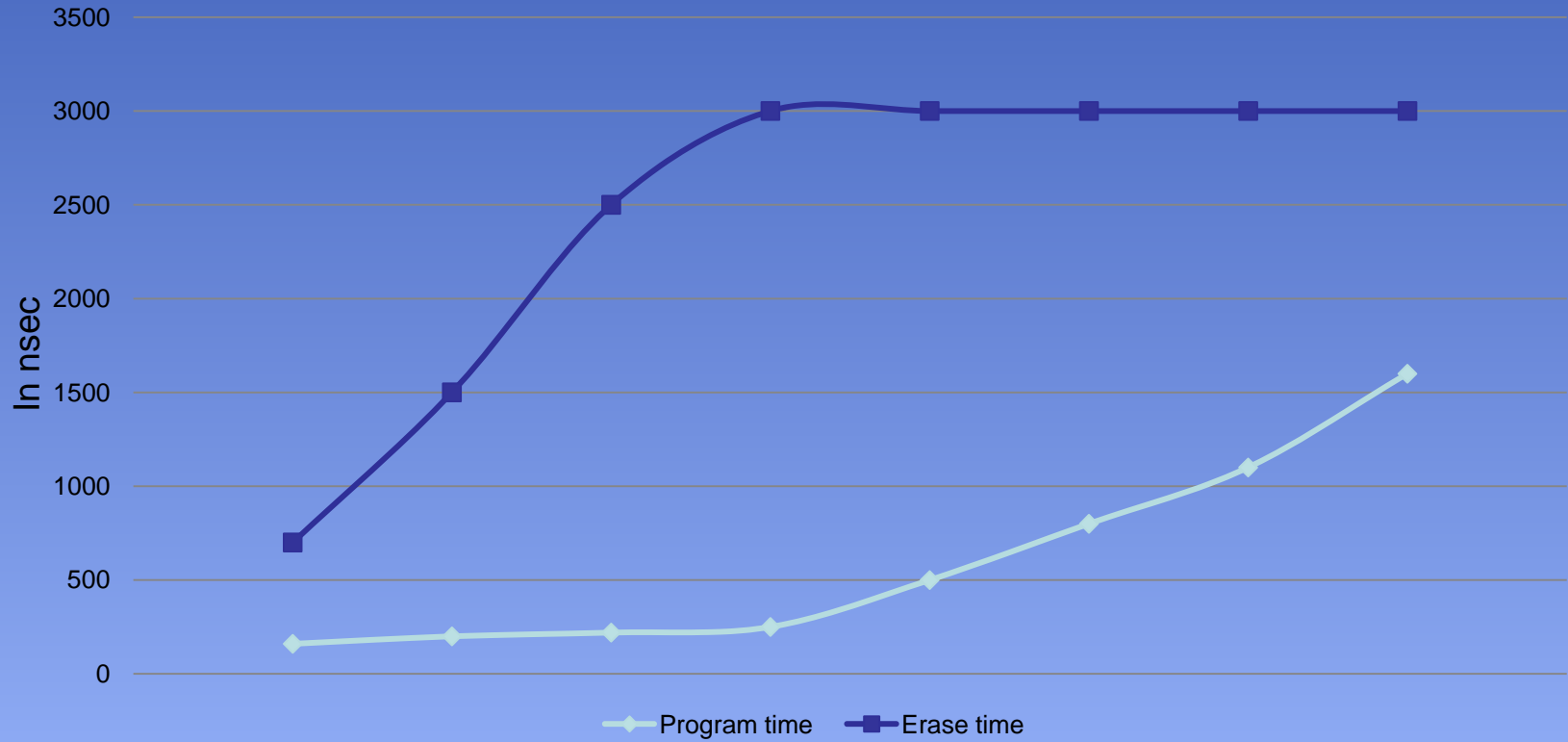
Command and Architecture Improvements

- Multi Plane
- Bus turn-around time
  - Ability to transfer data
  - Multi device switch performance
- LUN Addressing
- Multiple Access capability
  - LUN addressing
  - Volume Support

- Cache Read
- Cache write
- Pipeline read
- Pipeline write
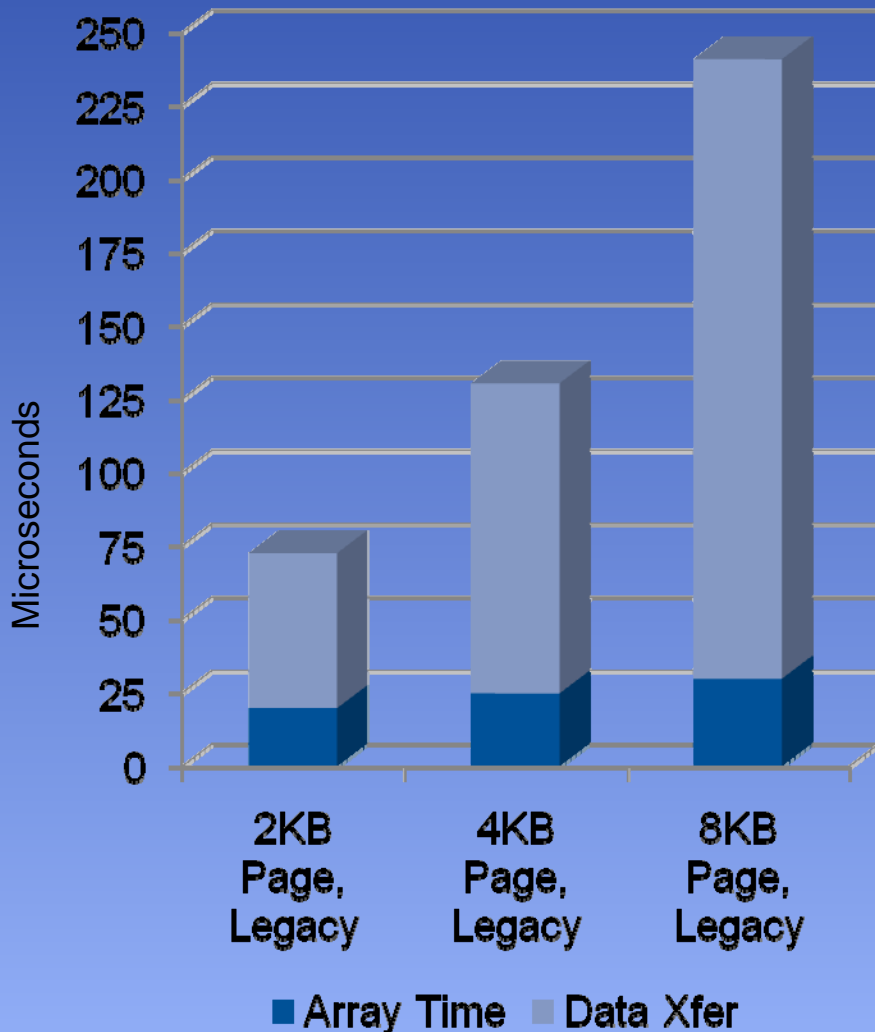- Enhanced commands
- Higher Bus Speed (Toggle, ONFi 2)

cādence

- **Enhanced commands**
  - Small Data Move command if supported, allows the host to transfer data to the page register in increments that are less than the page size of the device for both Program and Copy back operations.
- **Bandwidth**
  - Ability to utilize the larger page sizes
- **Reducing read and write page access cycles**
- **Command pipe lining**
- **Improving read modified write operation**

cādence

- **Sequential operation typical applications**
  - Card Based solutions USB, MMC etc
  - Storage of data, pictures, videos, boot image
- **Random Operations**
  - Embedded Systems
  - SSD's
  - Caching
  - Storage of data, active memory access and storage.

cadence®

Challenges: Latency Increases as Lithography Shrinks

Microseconds

2KB Page, Legacy   4KB Page, Legacy   8KB Page, Legacy

■ Array Time ■ Data Xfer

Data supplied by Micron

- NAND component performance is determined by two elements:
  - NAND array access time
  - Data transfer across the bus
- I/O time for NAND Page (tRC=20ns)
  - 2K page: 42μs
  - 4K page: 86μs

- For legacy reads, performance is artificially limited to 40 MB/s
  - Today for SLC NAND the I/O time is 2-4x the array transfer time

- As NAND page sizes increase, latency becomes large
  - Especially for small reads
- NAND array read transfer time
  - SLC: tR time is normally 20-25μs MAX
  - MLC: tR time is normally 50μs MAX
- I/O performance must be less than or equal to array performance for maximum sustained read throughput

cadence®

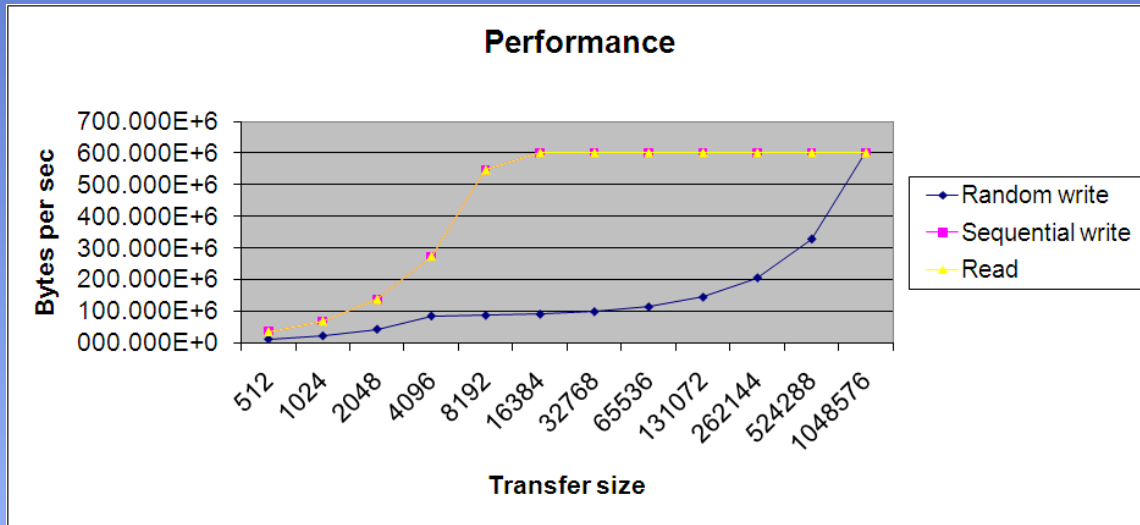# System Performance

Performance

Performance

SLC _Asynchronous_ Devices

8 Chip enables per channel

10 Channels or Flash controllers

4K Page size

- Sequential Read 360MBps
- Sequential Write 360MBps
- Random Write 52MBps @8K transfer
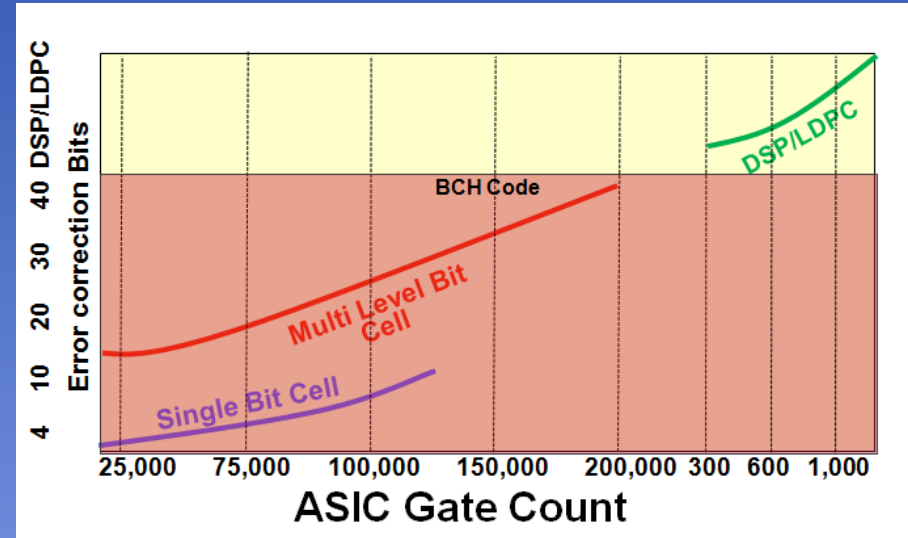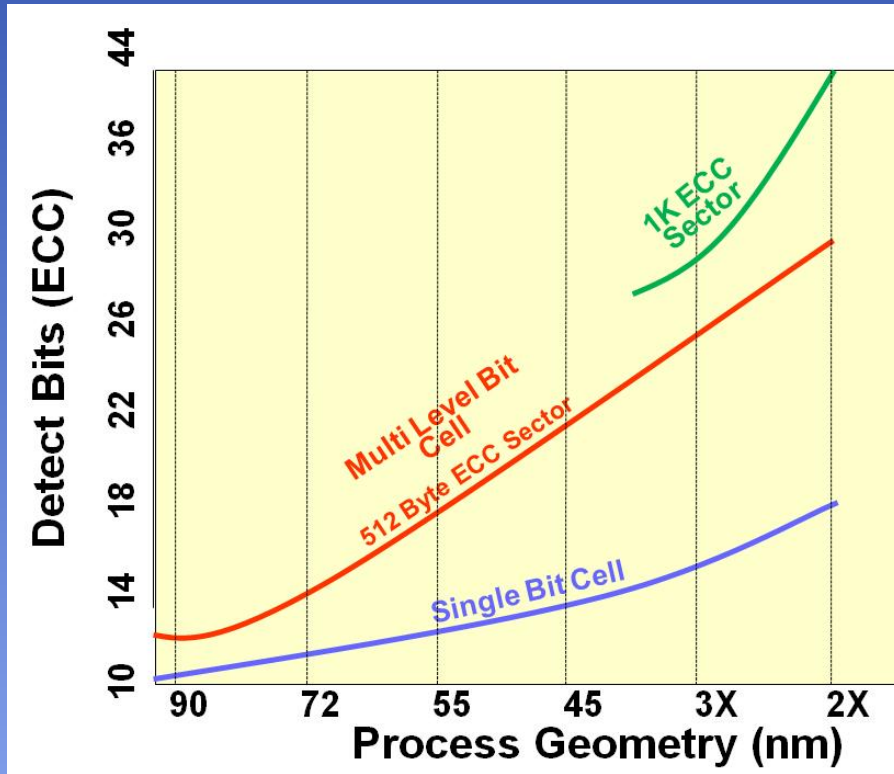
SLC _Synchronous_ Devices

8 Chip enables per channel

5 Channels or Flash controllers

4K Page size

- Sequential Read 600MBps
- Sequential Write 600MBps
- Random Write 86MBps @8K Transfer

- Typical Controller use more than one type of Error Correction i.e. 8 and 30bits
- DSP and LDPC are typically high latency Solutions
- BCH should be close if not at Line rate.

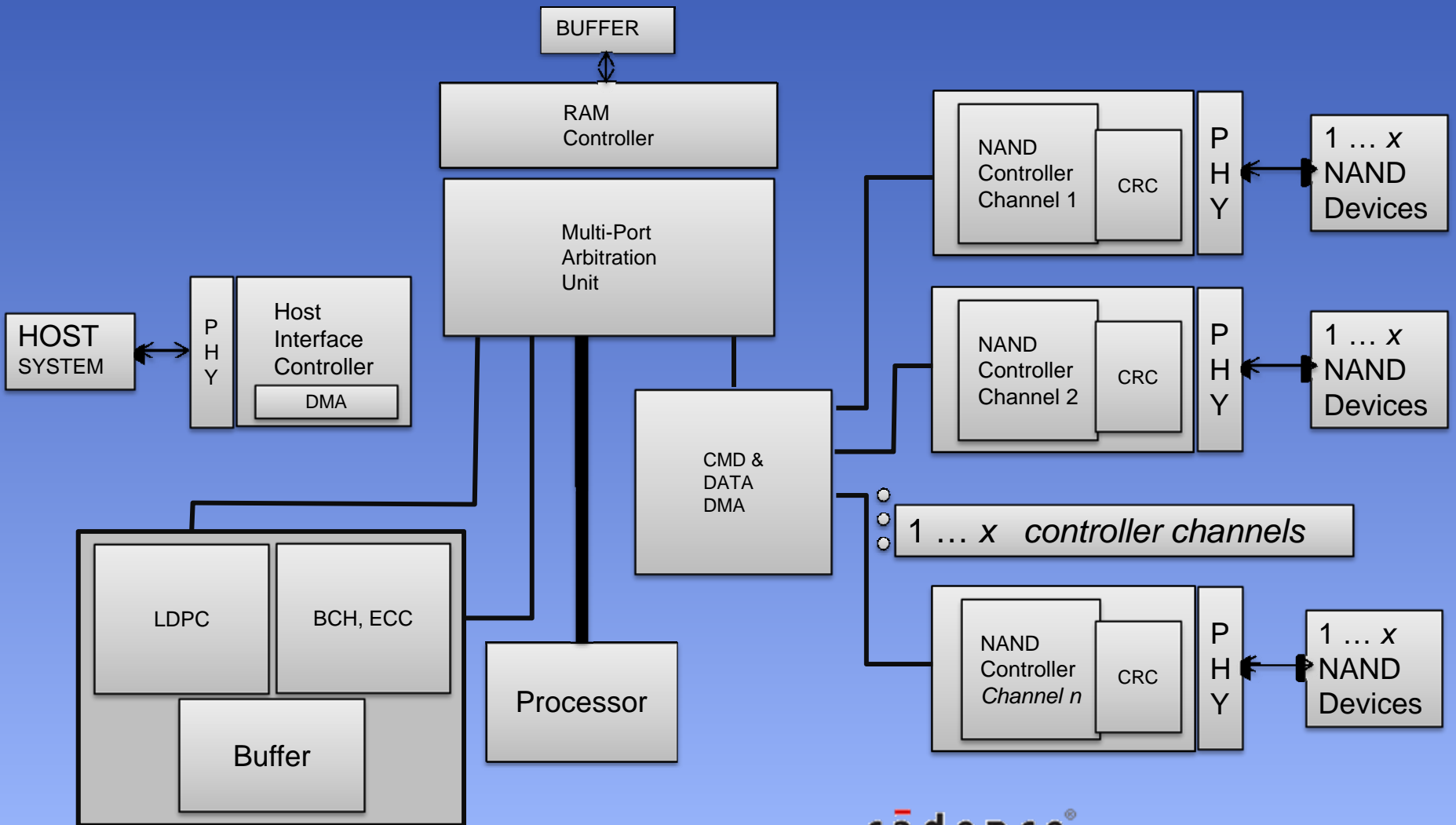|	BCH	Long BCH	LDPC
Latency	Low	Medium	High
Decoder Throughput	Very High	High	Medium
Gate Counts	Small	Medium	Large
Overhead Size	Very Small	Small	Small
Error Correction Capability	Limited	Better	Best

Cadence Nand Controller w PHY Support
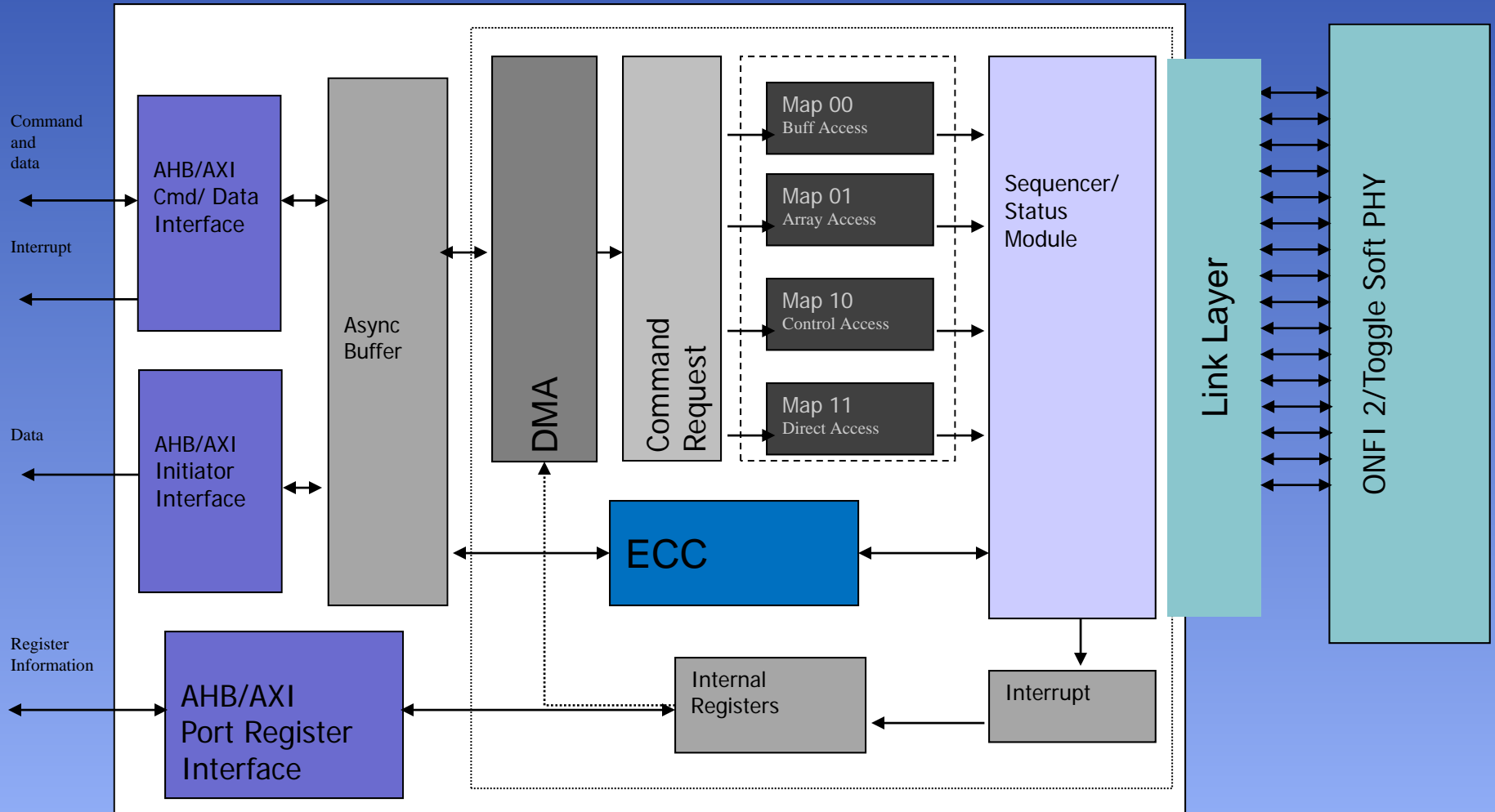
Centralized LDPC Hardware Architecture
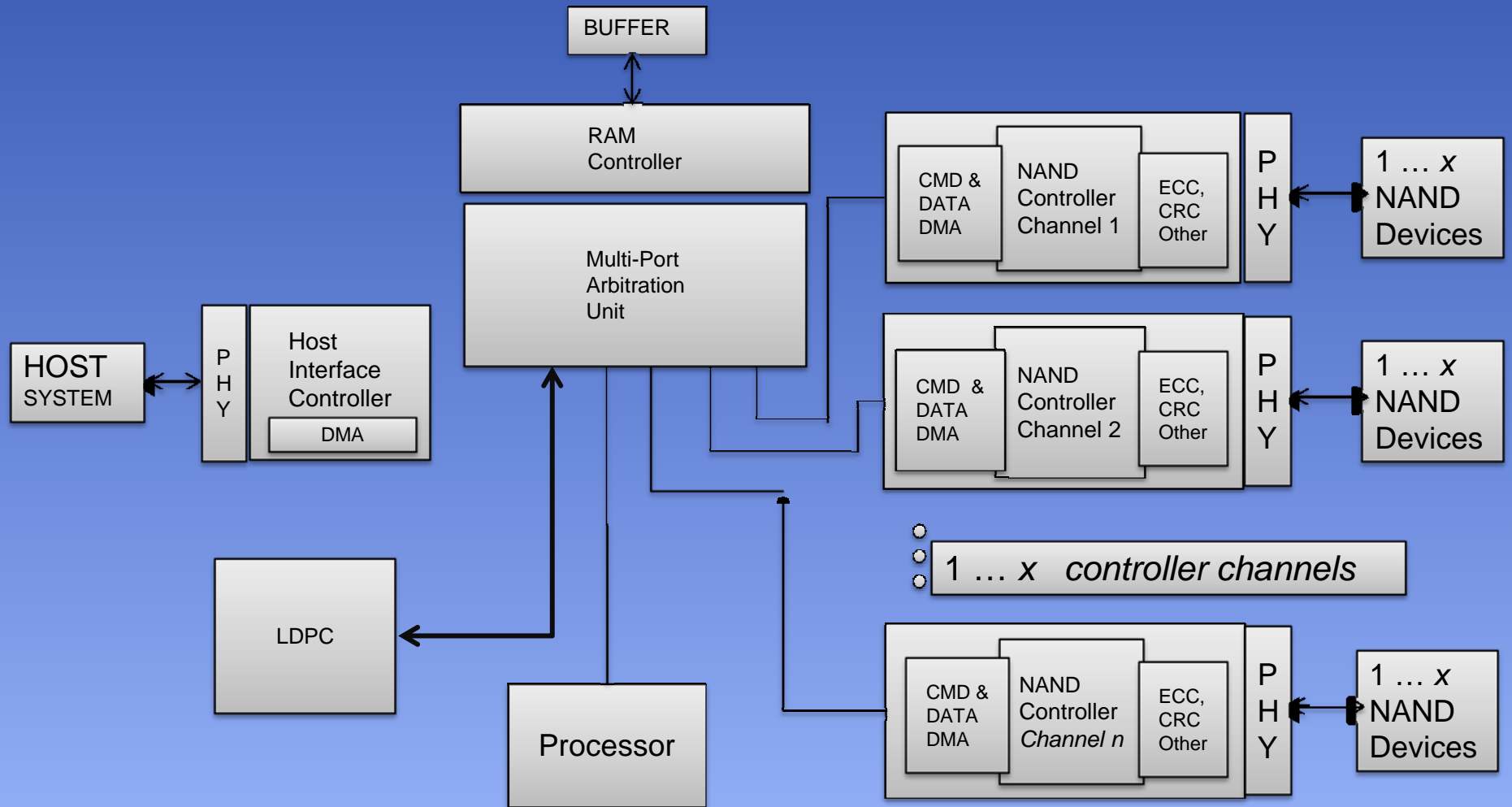
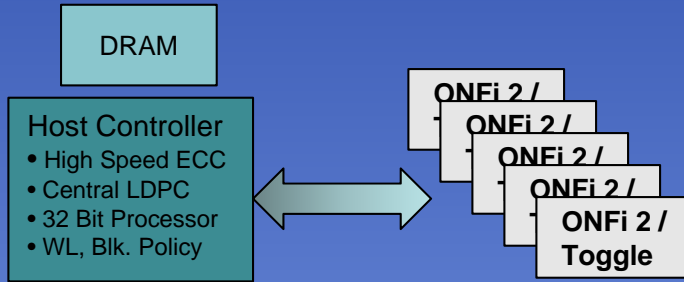# Centralized ECC Hardware Architecture

Key Aspects to System Performance Improvements

- Increase the number of commands to the flash device
  - Maximizes the number of transactions that a device can do
  - Toggle NAND is capable of 125% more Read bandwidth over typical asynchronous devices
- Fast error correction and identification of errors
  - Improves block management throughput
  - Reduces processor overhead
- Reduce Interrupts to processor
  - Improves the number of transactions, address translation
  - Improves ECC performance
  - Improves background process operation
  - Removes software timer requirements

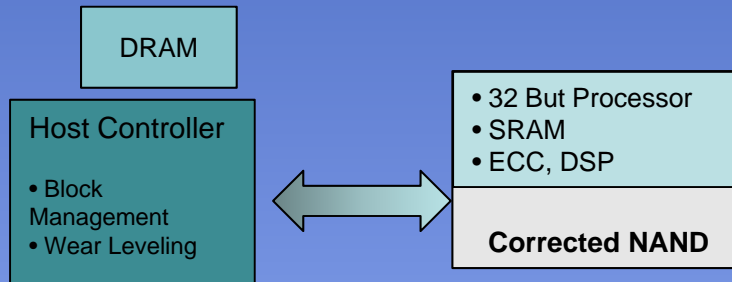cādence®

Performance System Architecture

Applications

- **SSD Controller**
- **UFS**
- **Cache Controller**
- **Enterprise**

DRAM

Host Controller
- High Speed ECC
- Central LDPC
- 32 Bit Processor
- WL, Blk. Policy

ONFi 2 /
ONFi 2 /
ONFi 2 /
ONFi 2 /
**ONFi 2 /
Toggle**

- Highest Performance
- Most flexibility for Block Policy
- Architectural Flexibility
- Highest Error Correction Solution
- Command Q to maximize Bus utilization

- **SSD Controller**
- **HS USB 3.0**
- **Cache Module**

DRAM

Host Controller

- Block Management
- Wear Leveling

- 32 But Processor
- SRAM
- ECC, DSP

Corrected NAND

- Reduced HOST Resources
- Known good Data
- Higher data latency
- Easier to keep up with shrink Path
- Less flexible for block policy

- **Card based**
- **USB 2/3**
- **MMC**

Host Controller

- 16 bit Controller
- Wear Leveling
- Min. Block Mgr.

SRAM
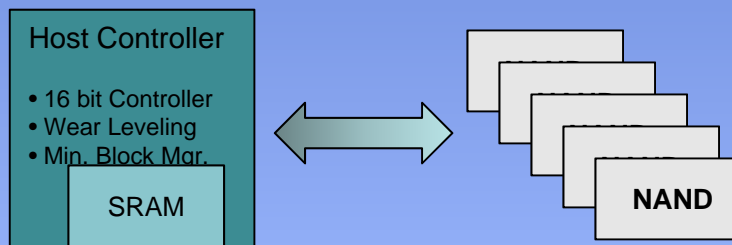
NAND

- High Latency
- Poor Random performance
- Block management slow
- Hard to keep up with HS Flash
- Basic ECC operation
- Low write count

cādence®

Five Trends to watch

1. Nand Device architectures and commands have to continue to improve

2. ECC Solutions are getting tougher to improve data reliability and improve Block Policy management

3. New controller architectures must continue to evolve based on system requirements. (One size not fit all)

4. Interface performance must continue to go faster (higher transfer rate)

5. Software complexity to utilize new error correction methods will become more complex

cādence®