

## LEC<sup>™</sup> Lyric Error Correction

## for Flash Memory

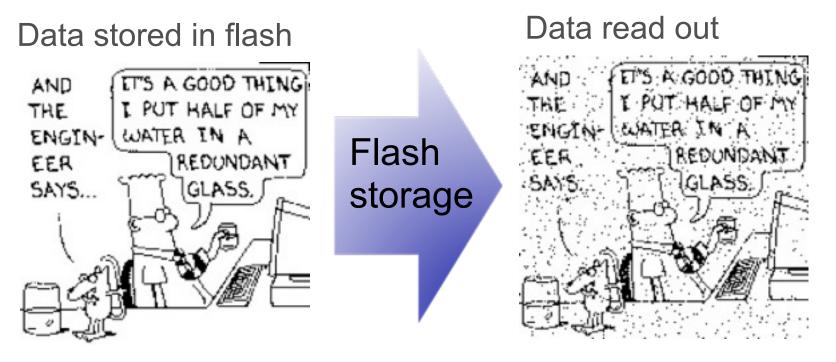
## Ben Vigoda, CEO

### Bit errors are key barrier to flash growth

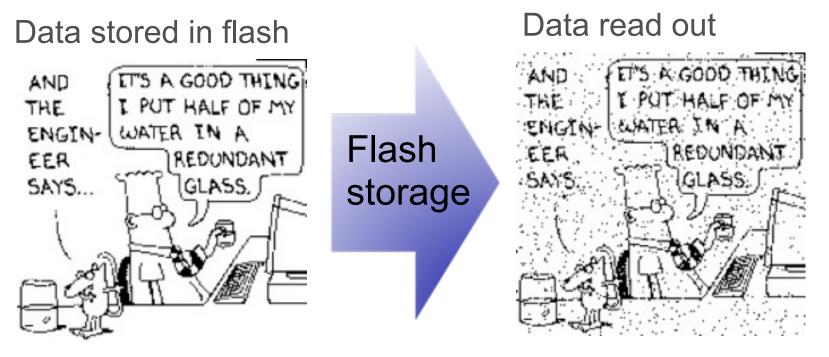
Lyric Semiconductor, Inc.

#### Data stored in flash





#### 1 bit wrong in every 100 stored!



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Causes of bit errors:

- Shrinking flash cell size
- Multi-level cells (MLC, TLC, etc.)
- Program-erase (P/E) cycles

# LDPC (Low Density Parity Check) is the solution for bit errors

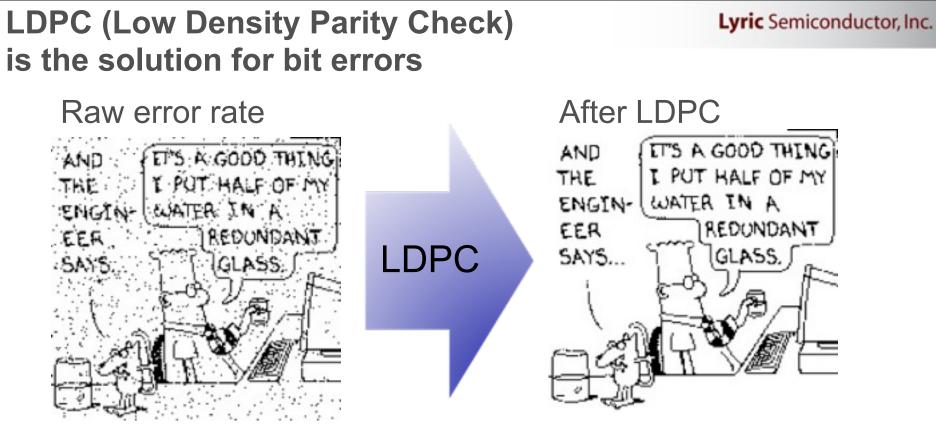
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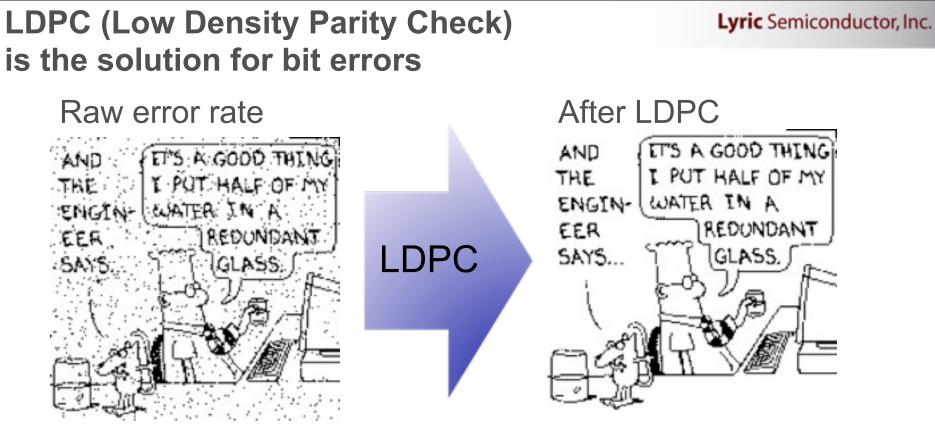
### Raw error rate



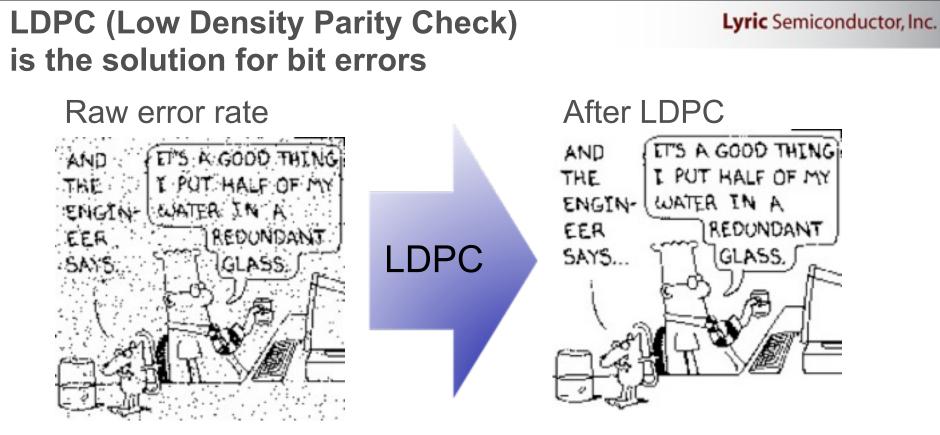
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1 bit wrong in every 1e15 (1000 trillion) stored!



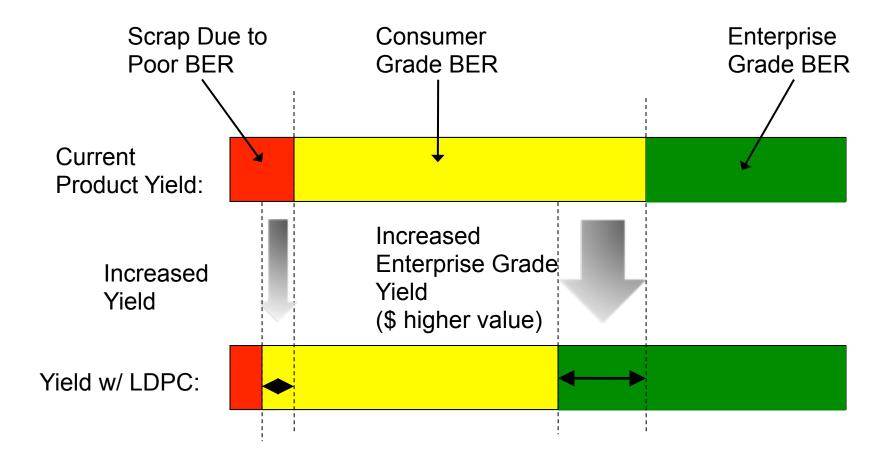
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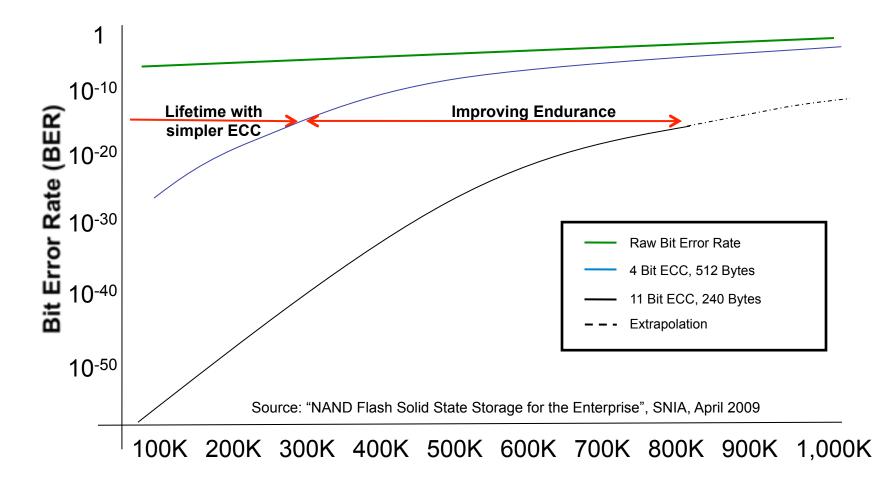
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- HDD has already begun to use LDPC
- SSD still needs LDPC (or related soft iterative decoding)

## **LDPC Enriches NAND Product Mix**



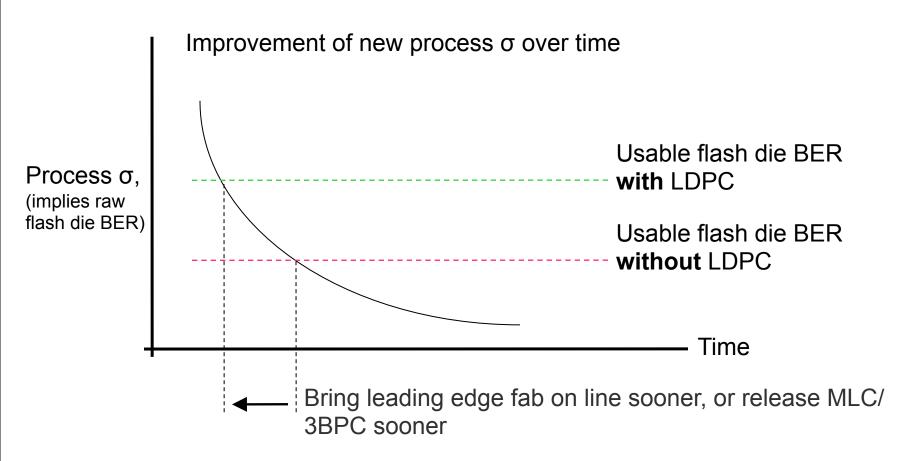
LDPC can convert low margin Flash into high margin flash by combating errors



#### **Program/Erase Cycles**

#### LDPC can combat increasing BER due to wear-out from Program/ Erase cycles

## LDPC Improves Time to Market for Next Gen Products



# Use MLC or TLC (3BPC) in new fab sooner – accelerate cost advantage

## LEC<sup>™</sup> Lyric Error Correction Lyric Semiconductor, Inc. is the smallest, lowest power, fastest LDPC

LDPC error correction implemented in digital





#### LDPC error correction using LEC technology

Lyric	Lyric	Lyric	Lyric	Lyric
PECS.0	PECAR	PECAR	PECAR	PECAR
STOP	STOP	STOP	STOP	STOP
OP10	GETE	GETE	GETE	GETE
Lyric	Lyric	Lyric	Lyric	Lyric
FECS.0	PECSO	PECSO	PECSO	PECSO
STOP	STOP	STOP	STOP	STOP
GEID	OFIC	OFIC	OFIC	OFIC
Lyric	Lyric	Lyric	Lyric	Lyric
PECS.0	PECLO	PECLO	PECLO	PECLO
STUTP	STOP	STOP	STOP	STOP
OP10	OPIO	OPIO	OPIO	OPIO
Lyric	Lyric	Lyric	Lyric	Lyric
PECS.0	PECLO	PECLO	PECLO	PECLO
STYP	SVVV	SVVV	SVVV	SVVV
0010	0010	0010	0010	0010
Lyric	Lyric	Lyric	Lyric	Lyric
Fectar	FECSO	FECSO	FECSO	FECSO
Strip	STOP	STOP	STOP	STOP
Offic	GETO	GETO	GETO	GETO
Lyric	Lyric	Lyric	Lyric	Lyric
FECS.0	Pecso	Pecso	Pecso	Pecso
STOP	Ster	Ster	Ster	Ster
OFIS	Gelo	Gelo	Gelo	Gelo

# LEC is built out of Lyric's probability processing circuits

## Higher performance LDPC

- 30X smaller at 1Gbps
- 70X smaller at 6Gbps
- 12X lower power
- 4X I/O bandwidth between flash and controller

# LEC<sup>™</sup> Lyric Error Correction Lyric Section Lyric Section

LDPC error correction implemented in digital



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Lyric Semiconductor, Inc.

## LEC gives you MORE LDPC

## Advanced error correction implemented in digital

Digital



LDPC using LEC technology



- Flash is high speed and low power, its LDPC should be too
- Pack more error correction into flash products

## LEC gives you MORE LDPC

## Advanced error correction implemented in digital





## LDPC using LEC technology

Lyric	Lyric	Lyric	Lyric	Lyric
PEC3.0	PECAN	PECAR	PECAD	PECAR
SWYF	SWF	STOP	SVIV	STOP
Geto	GEID	GETE	OPID	OPID
Lyric PECSA SWIT GEID	Lyric Fecto Stree	Lyric PECSO STOP OFIC	Lyric PECSO STOP OFIC	Lyric PECSO STRF GEID
Lyric	Lyric	Lyric	Lyric	Lyric
FECSA	PECAO	PECLO	PECLO	PECSO
SWIT	SVVV	STOP	STOP	STOP
GEIS	Geto	OPIO	OPIO	OPIO
Lyric Store	Lyric PECAN SVVV OPIN	Lyric PECLO SVVV 0010	Lyric PECLO SVVV 0010	Lyric Fecalo Store Gete
Lyric	Lyric	Lyric	Lyric	Lyric
FECSA	PECAO	FECSO	FECSO	Fecato
SWIFF	STOP	STOP	STOP	Store
GEIS	OPIO	Geto	Geto	Geto
Lyric	Lyric	Lyric	Lyric	Lyric
PECSA	PECAO	PECSO	PECSO	PECSO
STITE	AVVI	STOP	STOP	STOP
OFIO	OFIO	OFIC	OFIC	OFIC

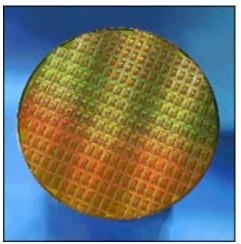
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- Pack more error correction into flash products

#### Mobile



Lower power, longer drive life, smaller form factor

#### Foundry





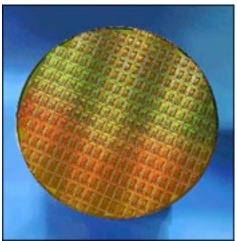
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- Extended longevity
- Lower latency

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Improve effective quality of flash silicon



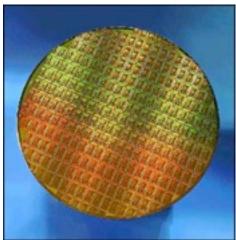
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- Improve effective quality of flash silicon
- Use MLC and TLC for high value applications



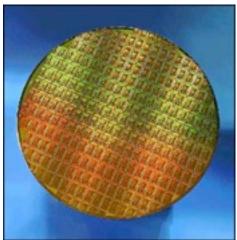
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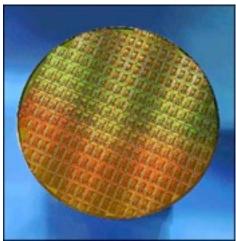
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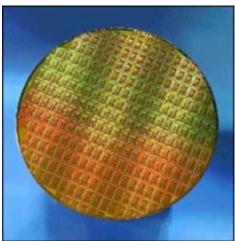
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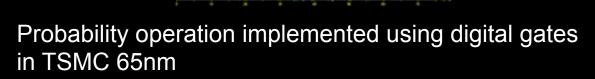


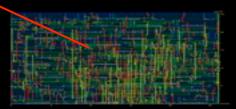


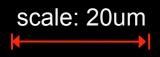
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- EZ-NAND: embed LEC with flash itself output just the right bits

# Core operations for LDPC are smaller using LEC technology

Probability operation implemented using digital gates In TSMC 180nm







Wednesday, August 25, 2010



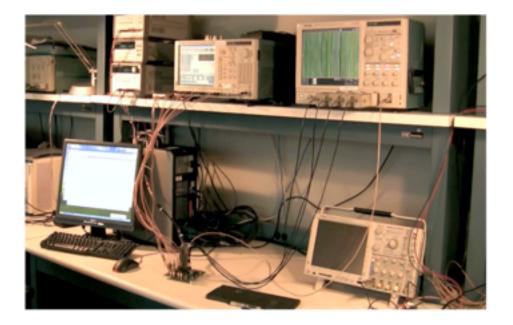
Power and area beats 45nm digital implementation

Lyric's Bayesian gate in TSMC 65nm



Power and area beats 15nm digital implementation

## **LEC Demonstration**

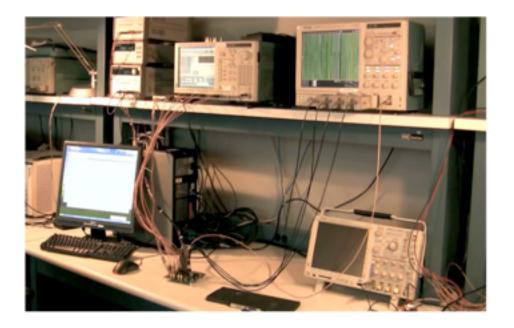


#### Working with a top-tier flash manufacturer:

- 1. Encoded data with parity bits
- 2. Stored in NAND flash
- Baked in oven to simulate aging (raw BER approx. 10e-2)
- Read out data including soft information
- Processed this data through our LEC silicon
- BER rates are the same as benchmark digital implementations

#### Lyric Semiconductor, Inc.

## LEC is Available Now



- Second generation LEC running on the bench at Lyric
- Technology is currently available for license
- Using Lyric's proprietary EDA flow, port to the preferred foundry and tailor to other specific needs

