LEC™ Lyric Error Correction

for Flash Memory

Ben Vigoda, CEO

Bit errors are key barrier to flash growth

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Data stored in flash

Flash storage

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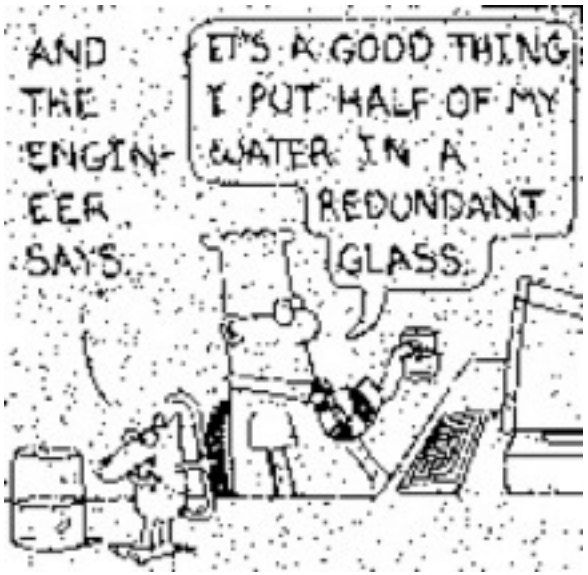
Data read out



1 bit wrong in every 100 stored!

Bit errors are key barrier to flash growth

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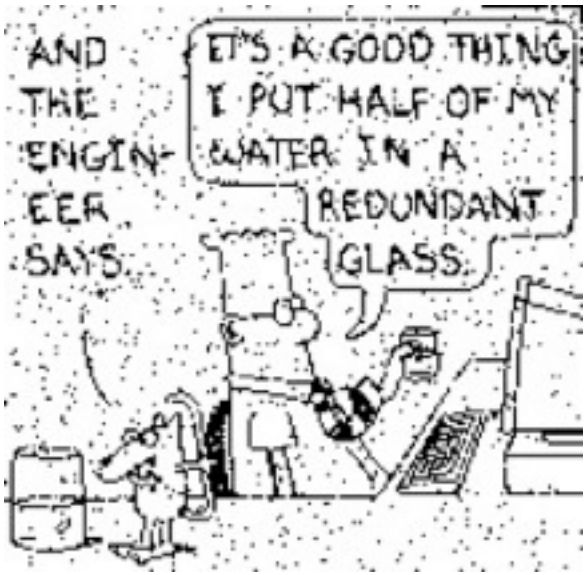

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Causes of bit errors:

- Shrinking flash cell size
- Multi-level cells (MLC, TLC, etc.)
- Program-erase (P/E) cycles

LDPC (Low Density Parity Check) is the solution for bit errors

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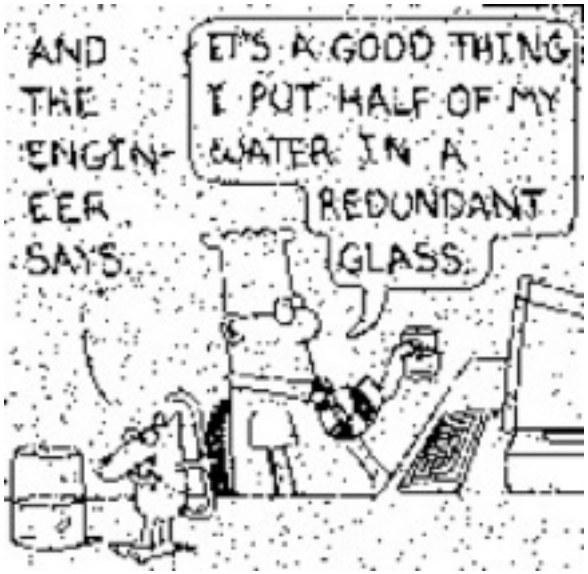
Raw error rate



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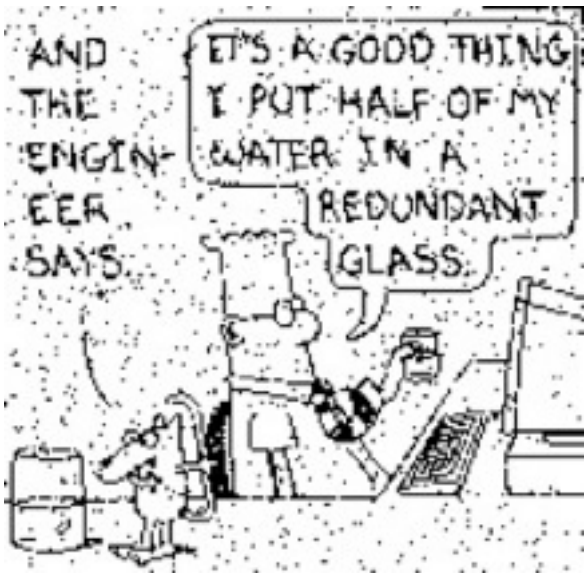

LDPC

After LDPC

1 bit wrong in every 1e15 (1000 trillion) stored!

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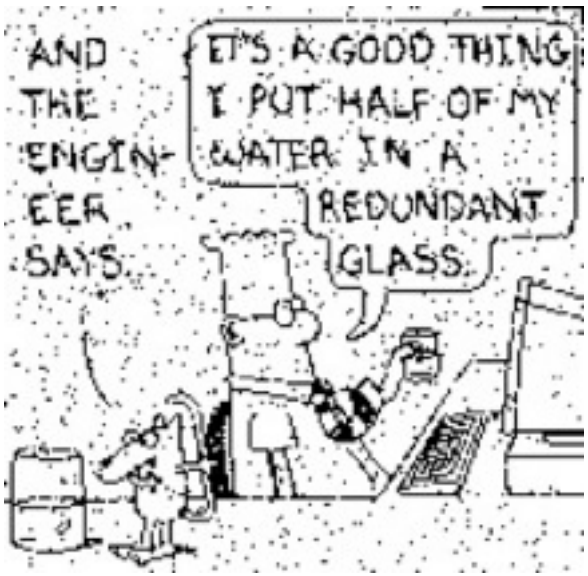

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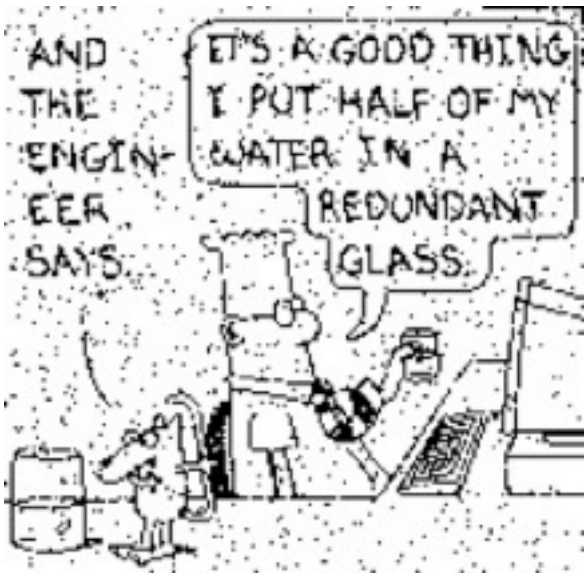

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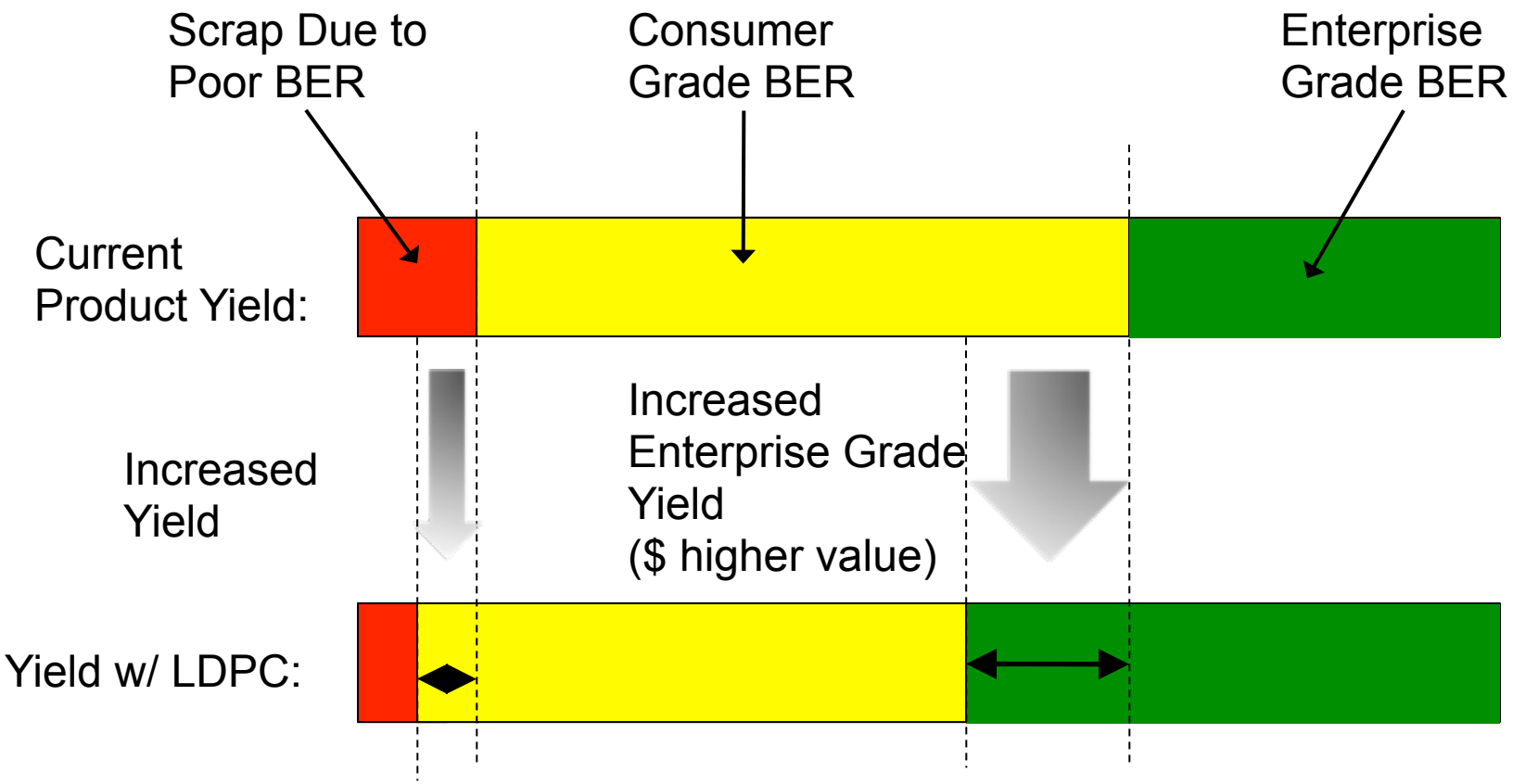
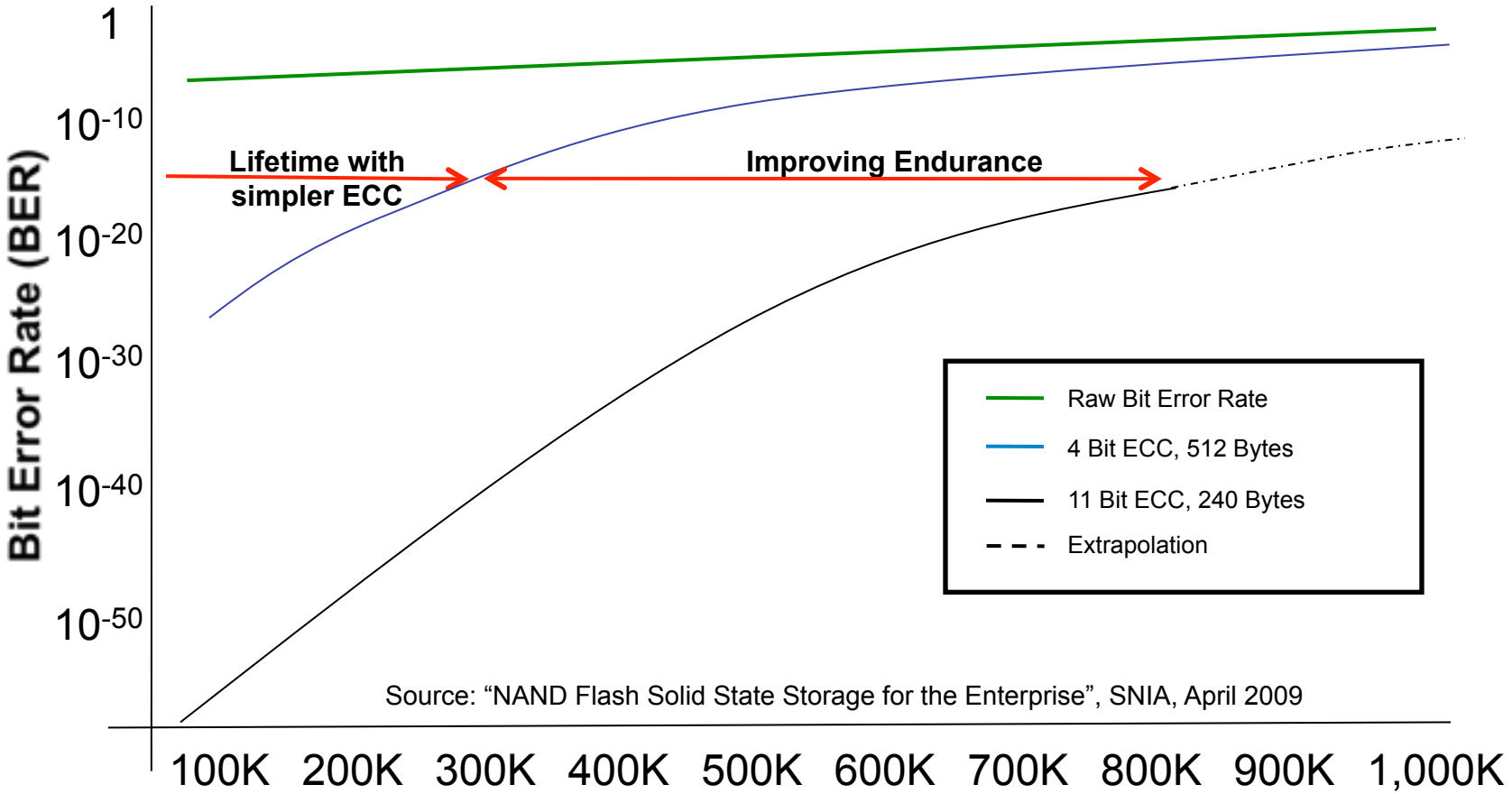
- **HDD has already begun to use LDPC**
- **SSD still needs LDPC** (or related soft iterative decoding)

LDPC Enriches NAND Product Mix



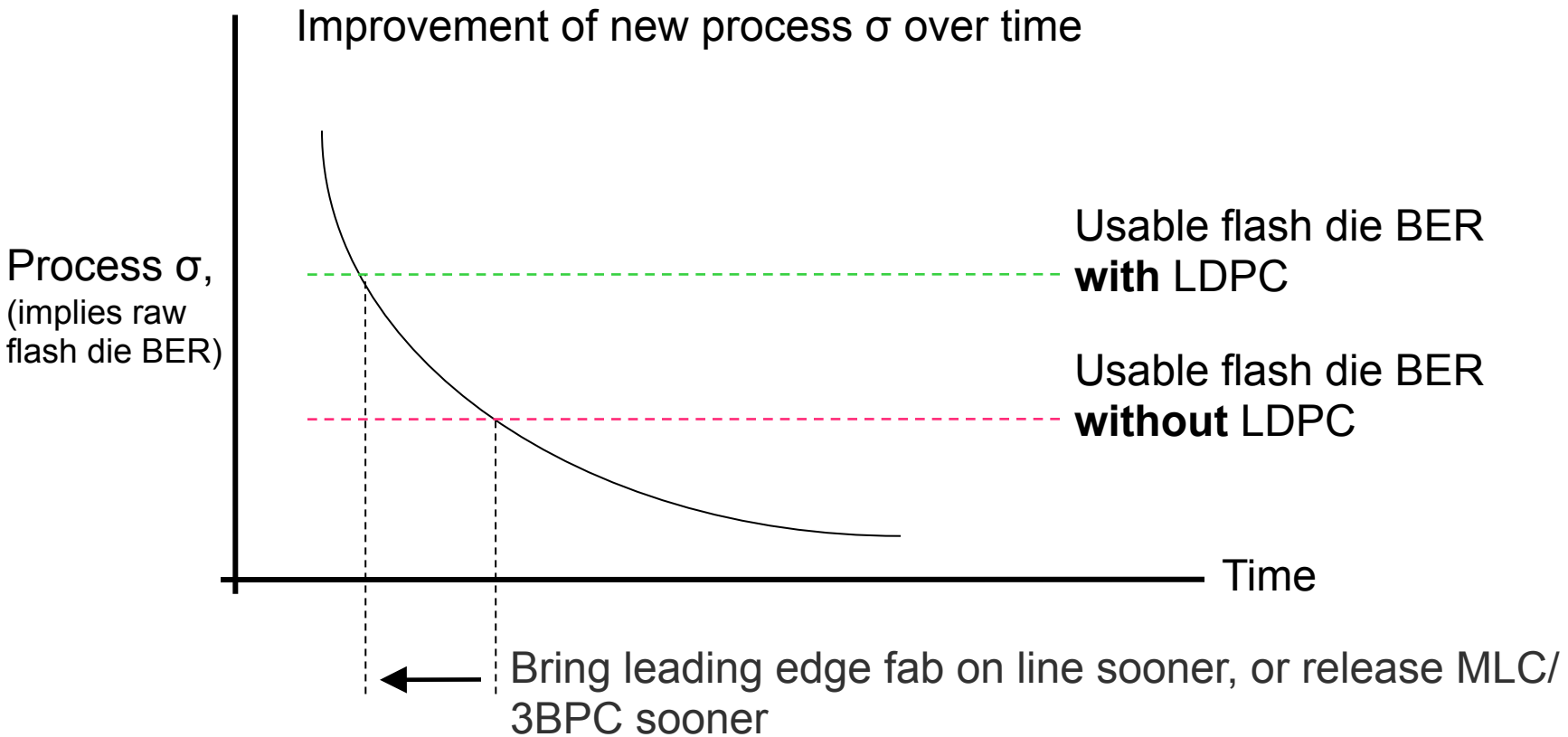
LDPC can convert low margin Flash into high margin flash by combating errors

LDPC Extends NAND Endurance



LDPC can combat increasing BER due to wear-out from Program/ Erase cycles

LDPC Improves Time to Market for Next Gen Products



Use MLC or TLC (3BPC) in new fab sooner – accelerate cost advantage

LEC™ Lyric Error Correction is the smallest, lowest power, fastest LDPC

LDPC error correction implemented in digital

LDPC error correction using LEC technology

LEC is built out of Lyric's probability processing circuits

Higher performance LDPC

- **30X smaller at 1Gbps**
- **70X smaller at 6Gbps**
- **12X lower power**
- **4X I/O bandwidth between flash and controller**

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LEC gives you MORE LDPC

Advanced error correction implemented in digital

LDPC using LEC technology

- **Flash is high speed and low power, its LDPC should be too**
- **Pack more error correction into flash products**

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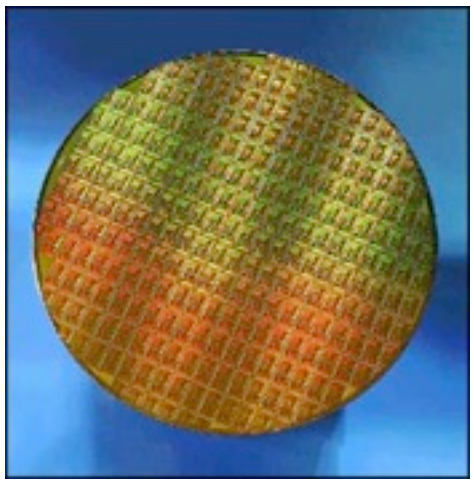
LEC applications

Mobile

Lower power, longer drive life, smaller form factor

Foundry



Enterprise

- Improved IOPs per Watt and $/IOPs
- Extended longevity
- Lower latency

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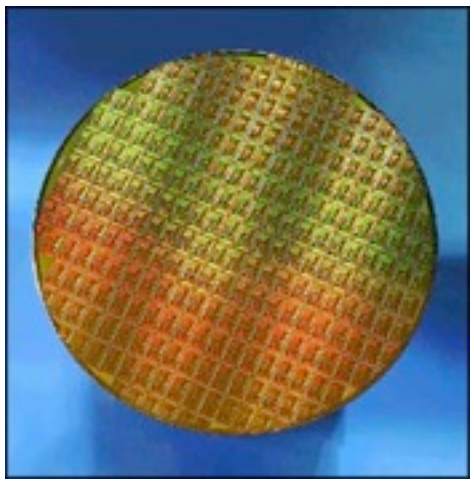

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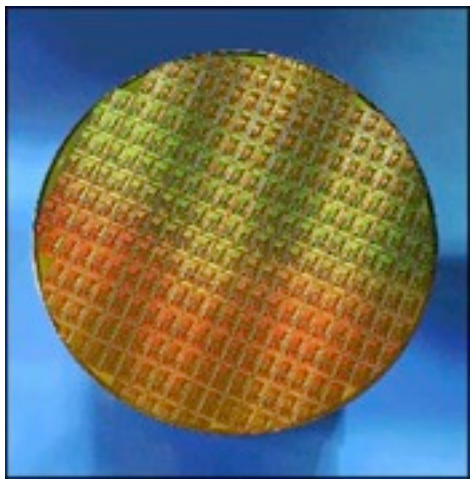

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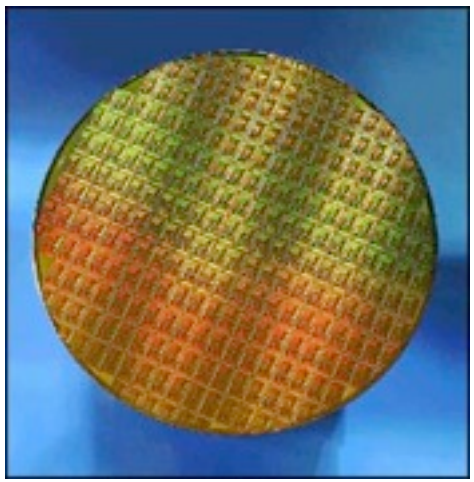

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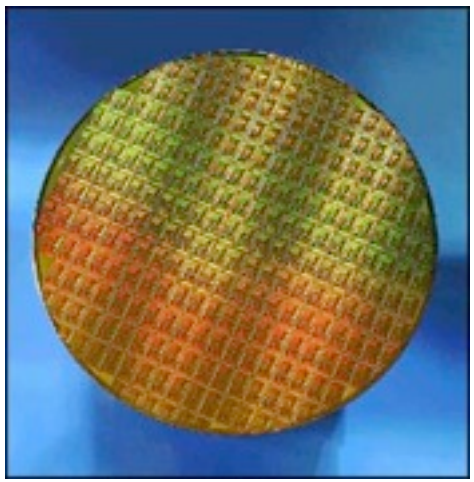

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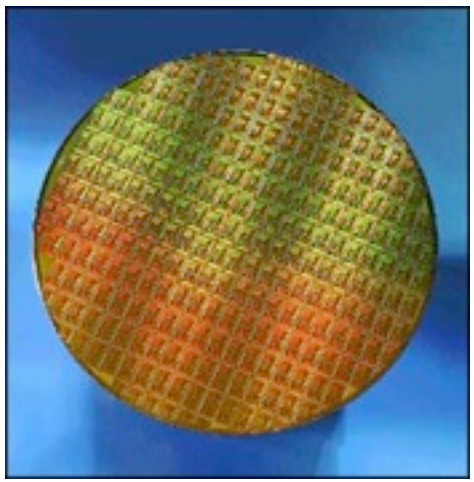
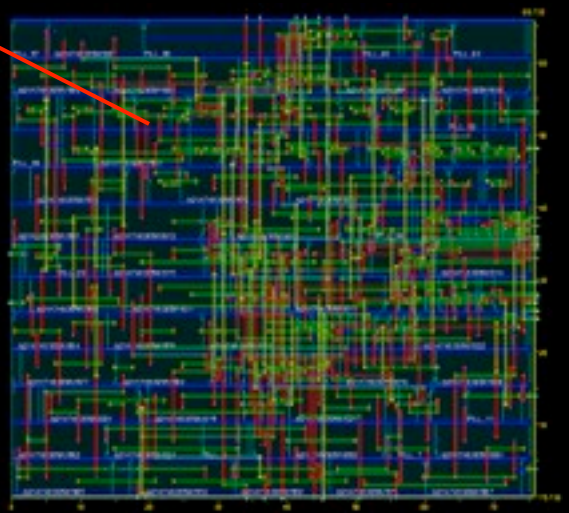


- Improve effective quality of flash silicon
- Use MLC and TLC for high value applications
- Get to MLC and TLC into new nodes faster
- Better threshold detection for MLC, TLC, and beyond
- EZ-NAND: embed LEC with flash itself – output just the right bits

Core operations for LDPC are smaller using LEC technology

Lyric Semiconductor, Inc.

Probability operation implemented using digital gates In TSMC 180nm



Probability operation implemented using digital gates in TSMC 65nm

scale: 20um

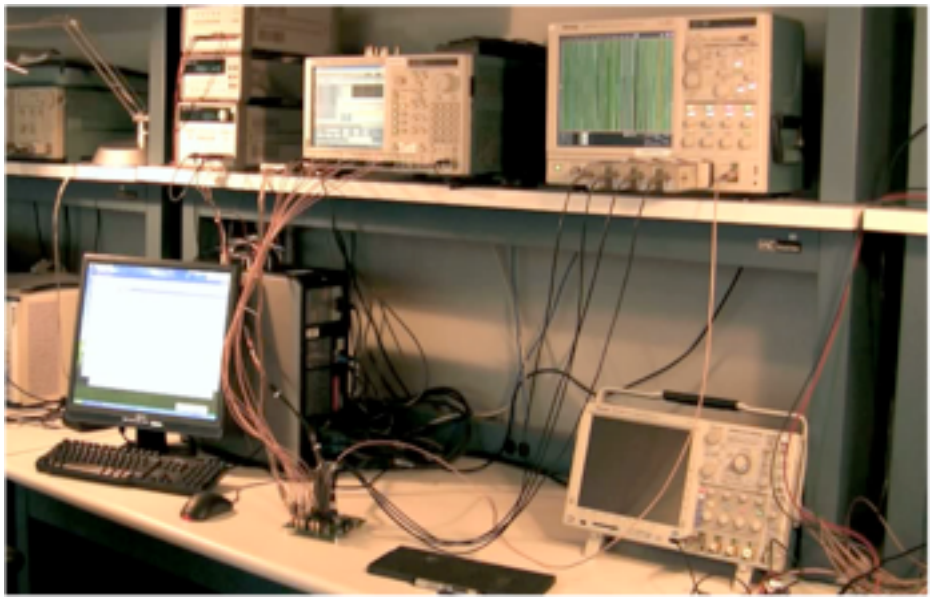
Lyric's Bayesian gate in TSMC 180nm

Power and area beats 45nm digital implementation

Lyric's Bayesian gate in TSMC 65nm

Power and area beats 15nm digital implementation

LEC Demonstration

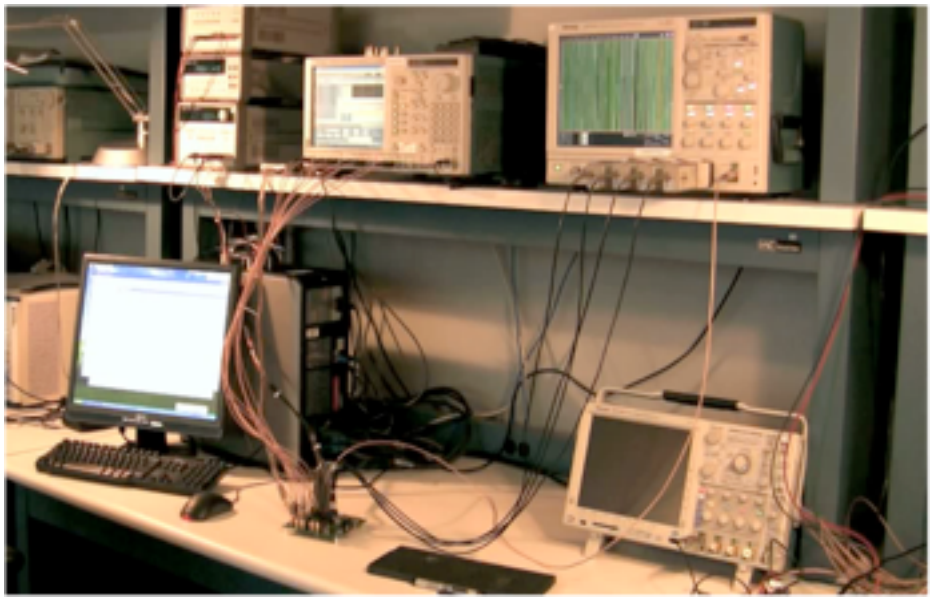


Working with a top-tier flash manufacturer:

1. Encoded data with parity bits
2. Stored in NAND flash

- Baked in oven to simulate aging (raw BER approx. 10e-2)
- Read out data including soft information
- Processed this data through our LEC silicon
- BER rates are the same as benchmark digital implementations

LEC is Available Now



- Second generation LEC running on the bench at Lyric
- Technology is currently available for license
- Using Lyric's proprietary EDA flow, port to the preferred foundry and tailor to other specific needs


Lyric