Looking Ahead to Higher Performance SSDs with HLNAND

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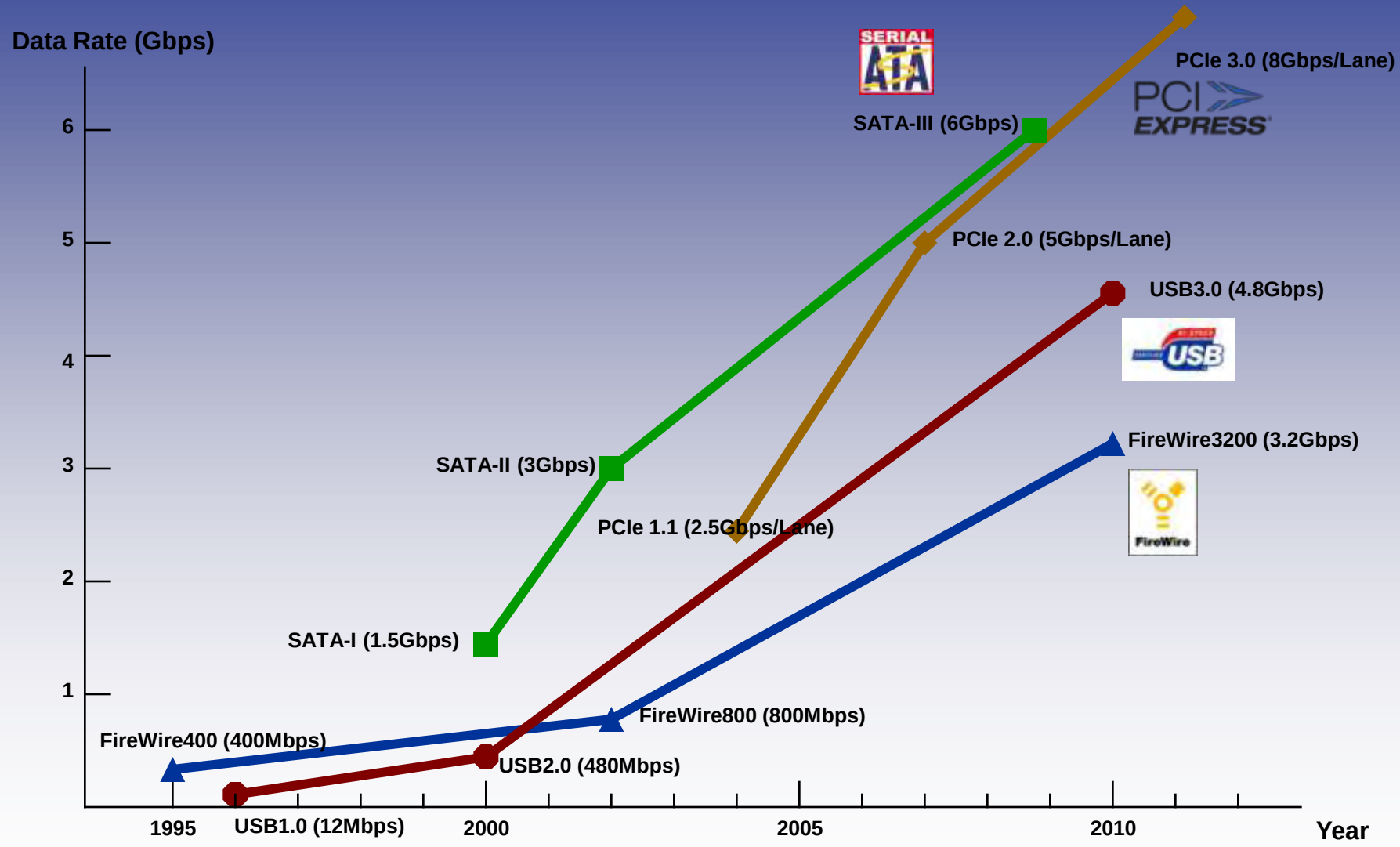
Infrastructure - Interface Progression



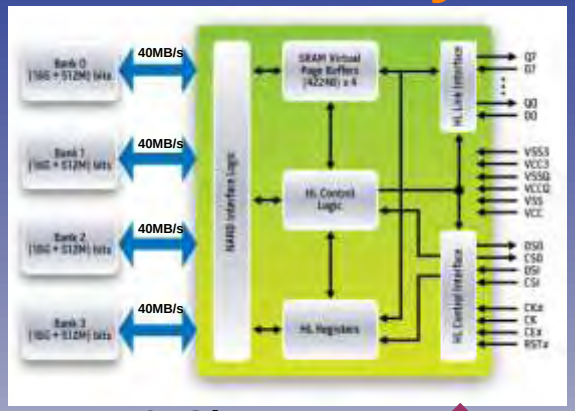
SSD Performance History

- 2007 ~ 2008: 1st Gen SSD
  - 4 channels and 4-way interleave
  - 30 ~ 80MB/s Read/Write performance
  - SSDs realized no tangible performance benefit over HDDs
- 2008 ~ 2009: 2nd Gen SSD
  - 8 ~ 10 channels
  - 200+ MB/s Read performance and 150MB/s Write performance becomes commonplace
  - SSD performance advantage established over HDDs
  - Consumer SSDs becoming commodity parts
- 2009 – 2010: 3rd Gen SSD
  - SATA 6Gbps adopted
  - 355MB/s Read / 215MB Write performance achieved

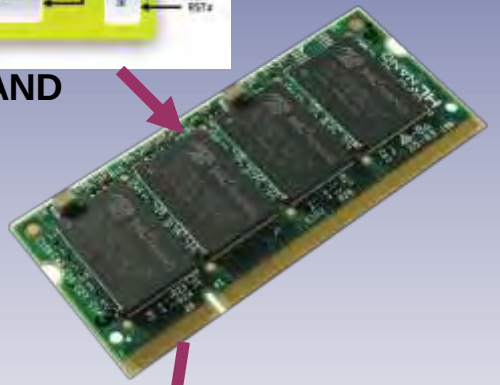
HLNAND SSD Prototype

HLNAND SSD Flash Anatomy

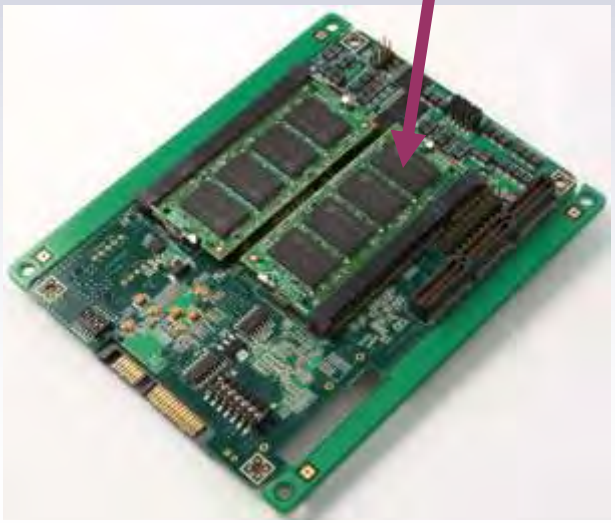
- 128GB on a single channel of HLNAND MCPs
- 133MHz, DDR266 HyperLink interface
- 16 MCP, 64 independent banks
- Data addressable 512B – 4KB virtual page size
- Concurrent Read & Write capability



64Gb HLNAND



64GB HLDIMM



HLNAND SSD System Anatomy

- Controller developed by INDILINX
- Virtex5 - 75MHz Core Frequency
- SATA 2 host interface
  - NCQ support
- Single HLNAND Channel @ 150MTs
- 64MB External SDRAM

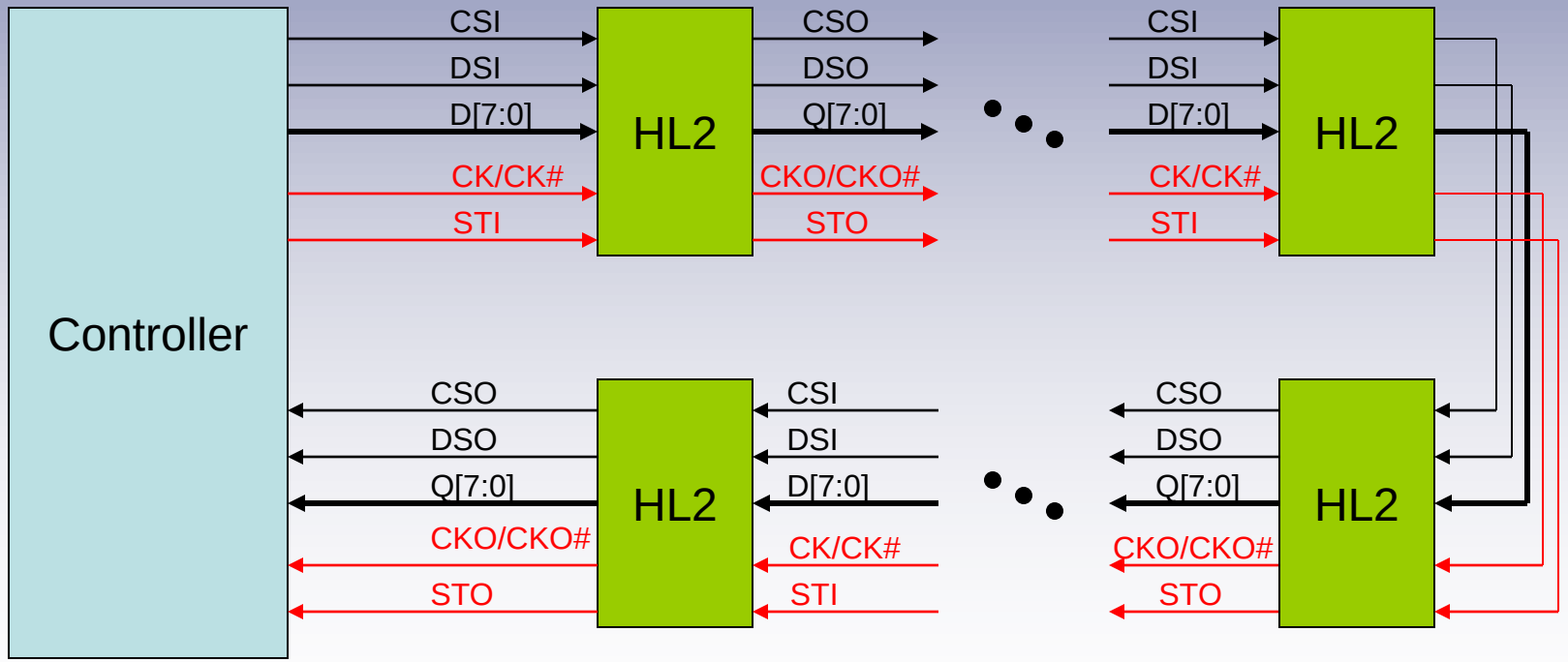
HLNAND SSD performance

- @ 75MHz (FPGA limit)
  - 120MB/s/ch. seq. read
  - 73MB/s/ch. seq. write
- @ 133MHz, translates to:
  - 212MB/s/ch. seq. read
  - 130MB/s/ch. seq. write
- 8 Ch. HL SSD capable of 1.7GB/s seq. read
- Further tuning will bring rates close to the 266MB/s/ch. Maximum, or 2.1GBps/ch.

Single Channel Performance

Introducing HLNAND2

- Source synchronous clocking
- JEDEC HSUL_12 interface up to DDR800
- Independent automatic status bus

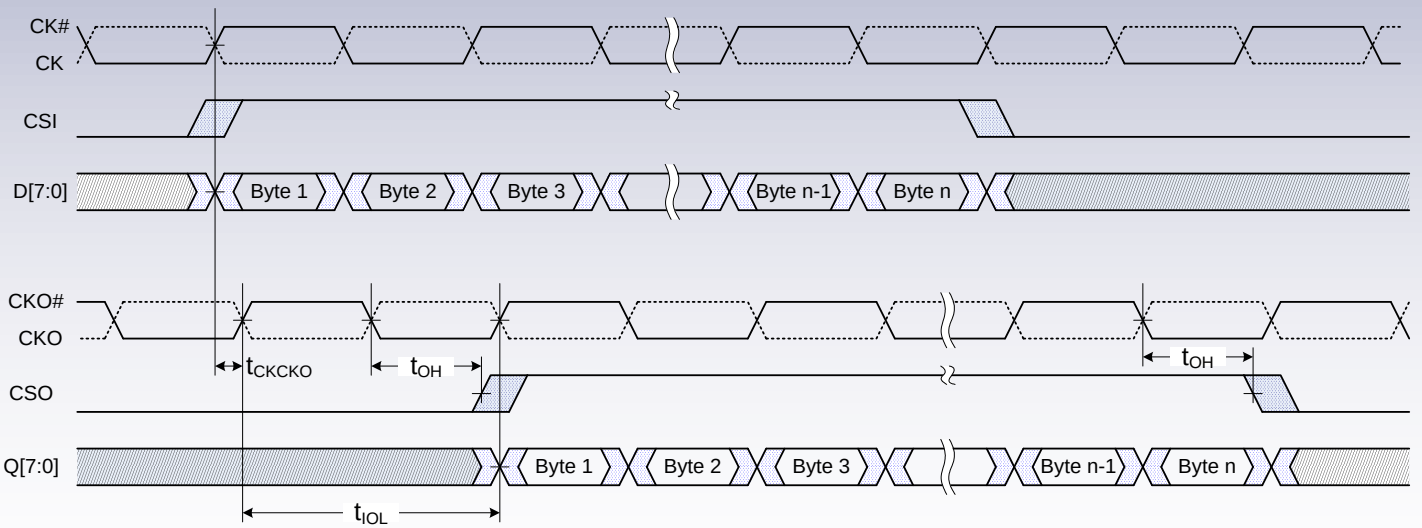


HLNAND2 Features

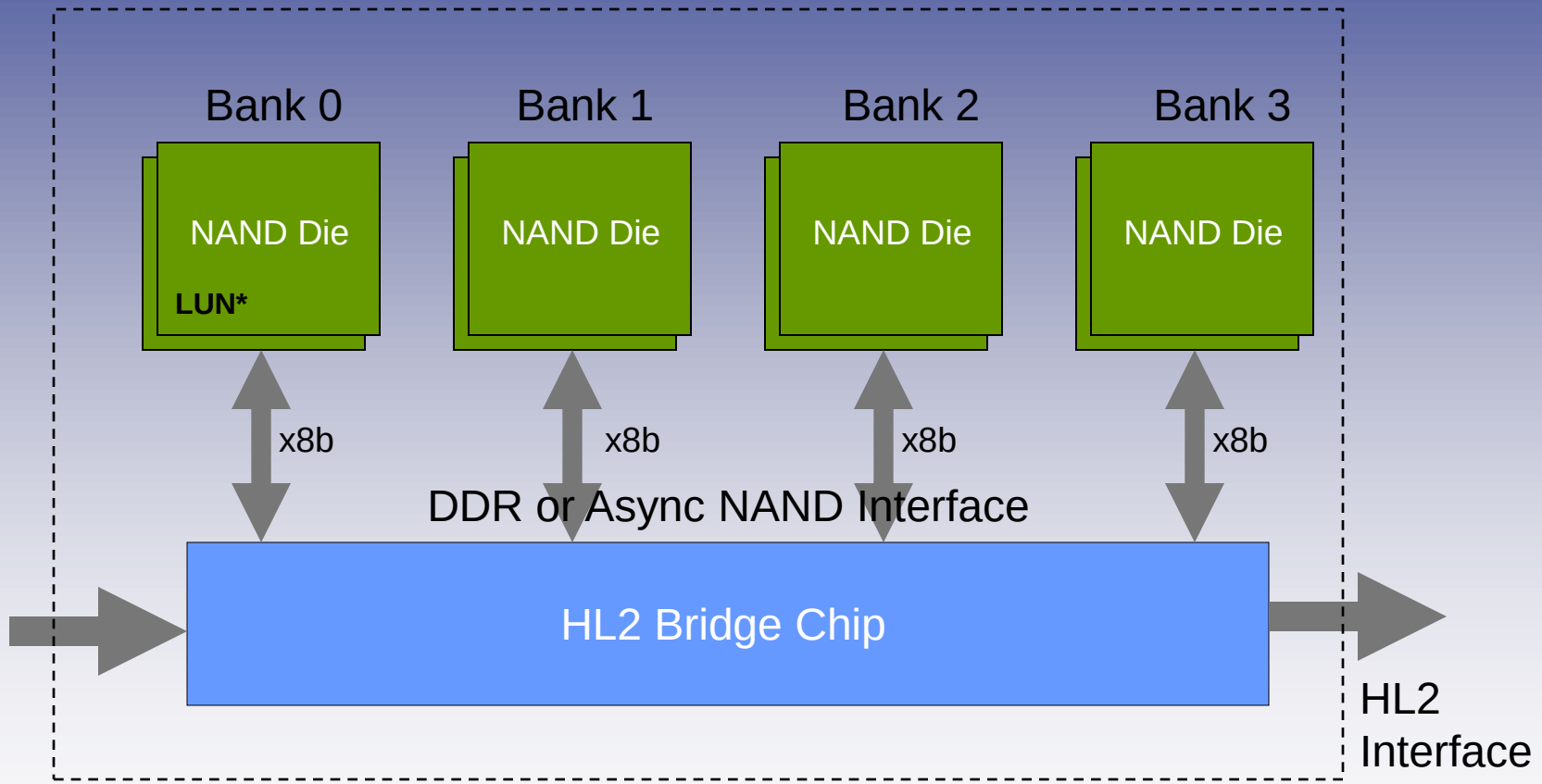
- DDR533 / DDR667 / DDR800
- JEDEC 1.2V HSUL_12 Interface Signaling
- Source Synchronous Clock CK & CK#
- Four bank architecture
- Fully independent 8 die operation
- Built-in EDC (Error Detection Code)
- DuplexRW™: Effectively 1600MB/s data throughput at DDR800, even with single HLNAND MCP
- Independent automatic status bus

HLNAND2 Clocking

- Point-to-point, source-synchronous clocking
- Input and output Data in phase with respective clocks
- Internal PLL shifts phase 90° to capture data
- Latency of 1 clock cycle from Data-in to Data-out



256Gb MLC HLNAND2 MCP

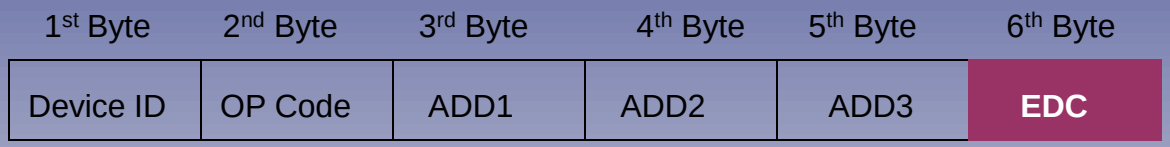


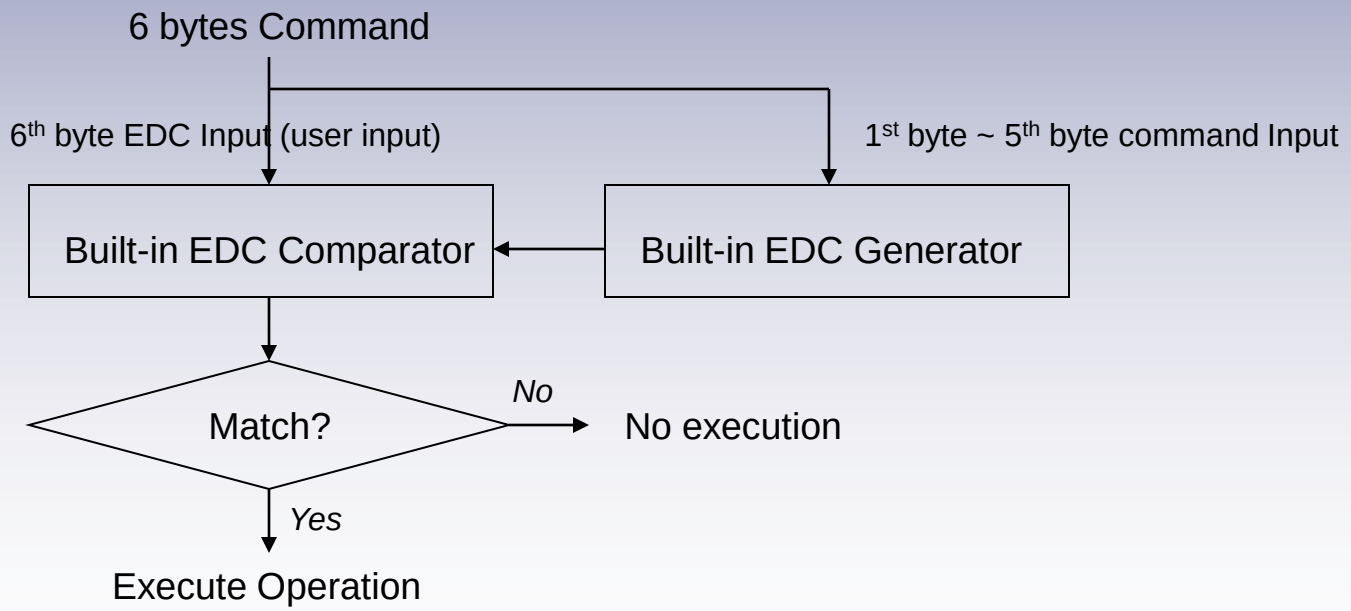
HL2-533/HL2-667/HL2-800

* LUN = Logical Unit

Built-in EDC (Error Detection Code)

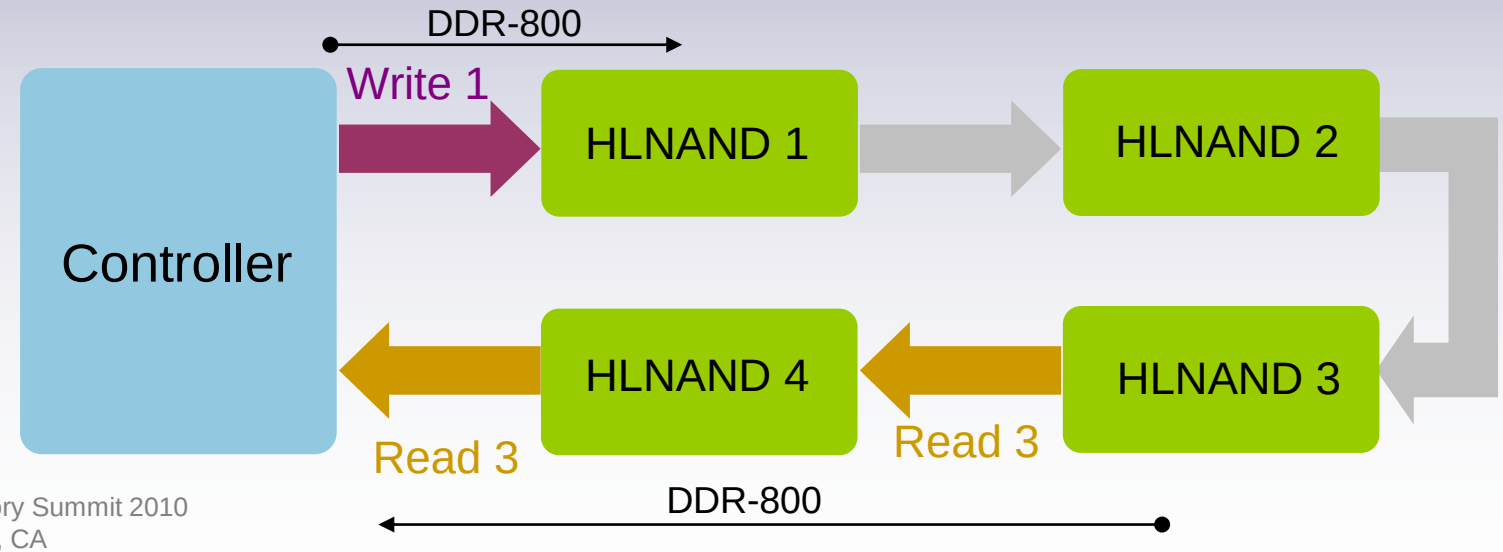
- 6 bytes Command Architecture





DuplexRW

- Once packet reaches addressed device the write data payload is truncated
- Simultaneous data transfer possible if write device is upstream of read device or the same device
- Effectively 1600MB/s data throughput, even with a single HLNAND MCP



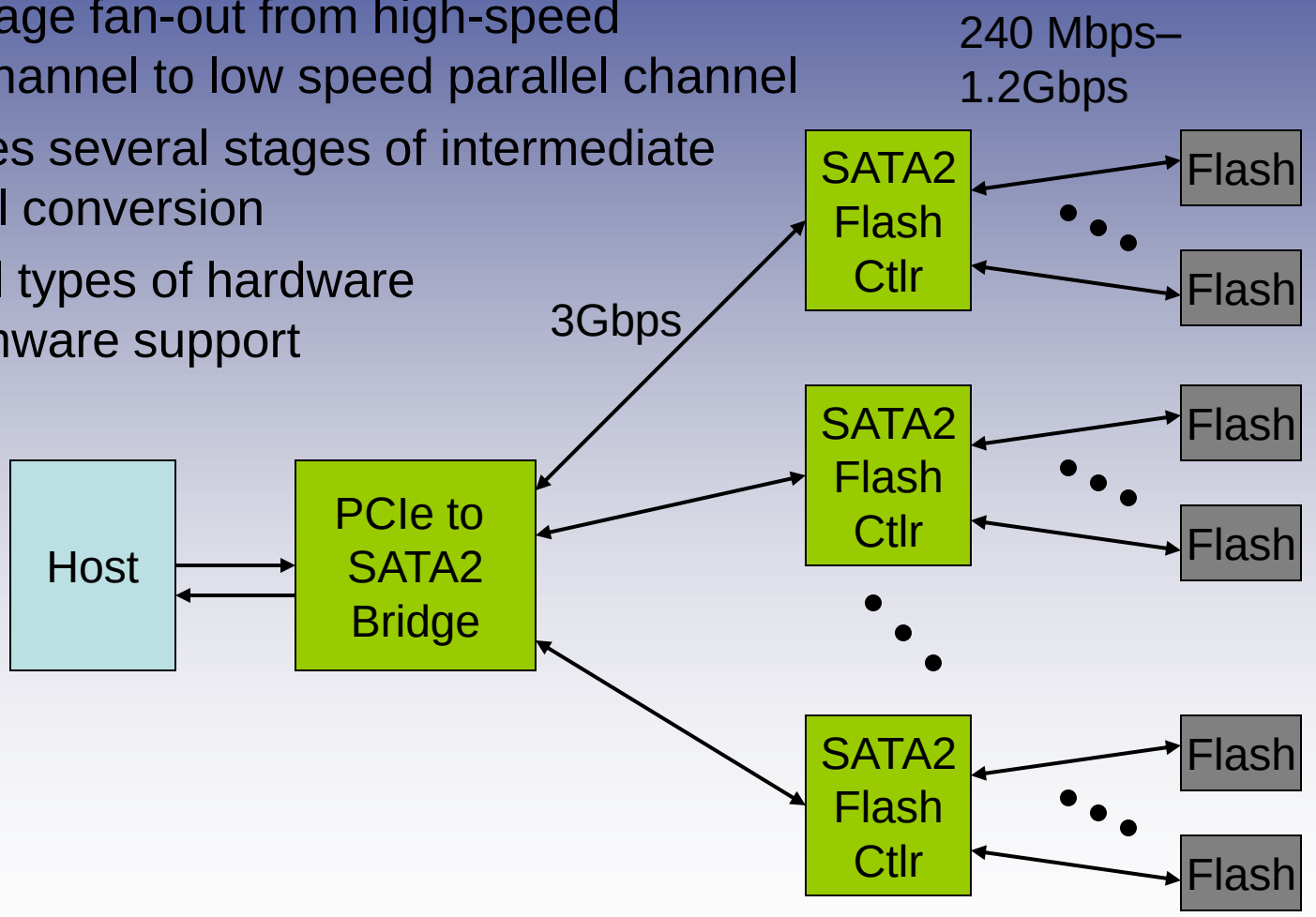
High-Speed NAND Comparisons

	HLNAND2	HLNAND	ONFi 2.0	Toggle-Mode
Synchronous IO	Yes	Yes	Yes	No
Transfer rate	800MT/s	266MT/s	166MT/s	133MT/s
Clock speed	400 MHz	133MHz	83MHz	67MHz (DQS)
# chips before roll-off	Limitless*	Limitless*	8	8

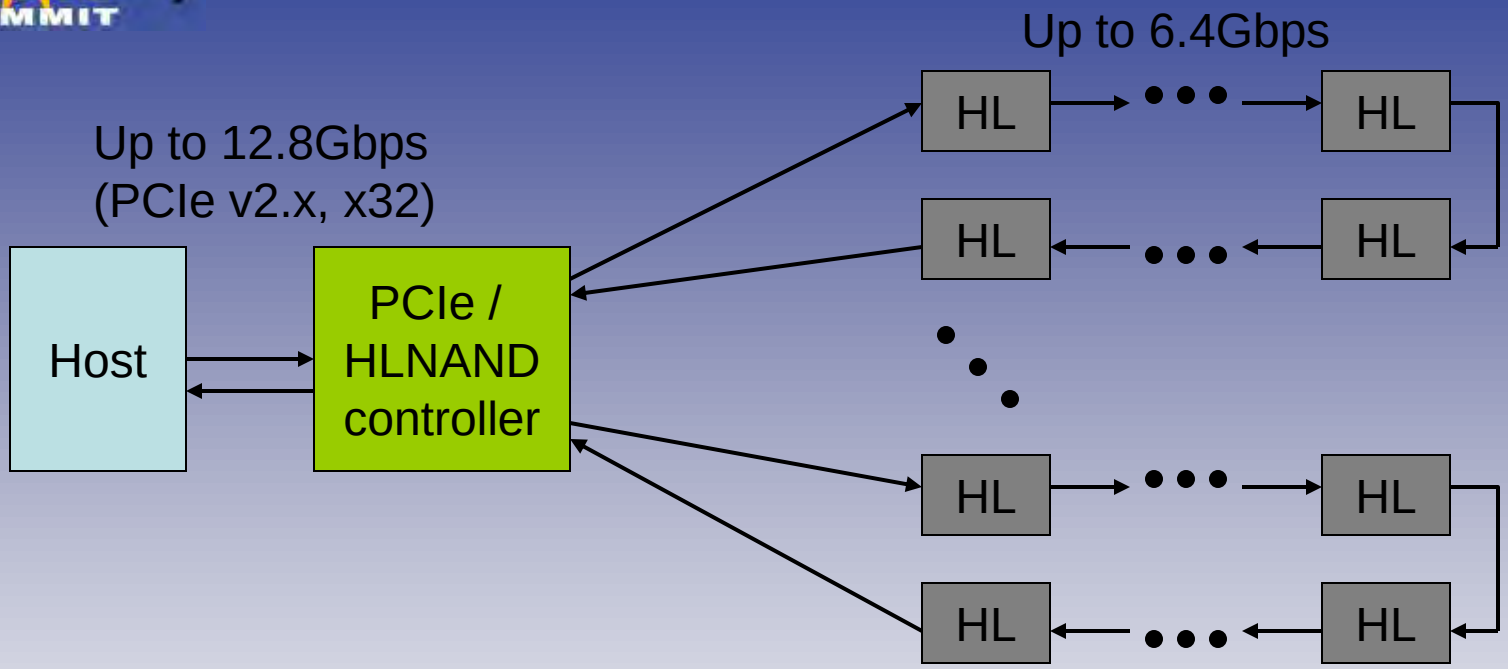
* Maximum addressable devices per ring is 255

Current High-Speed Enterprise Architecture

- Multi-stage fan-out from high-speed serial channel to low speed parallel channel
- Requires several stages of intermediate protocol conversion
- Several types of hardware and firmware support

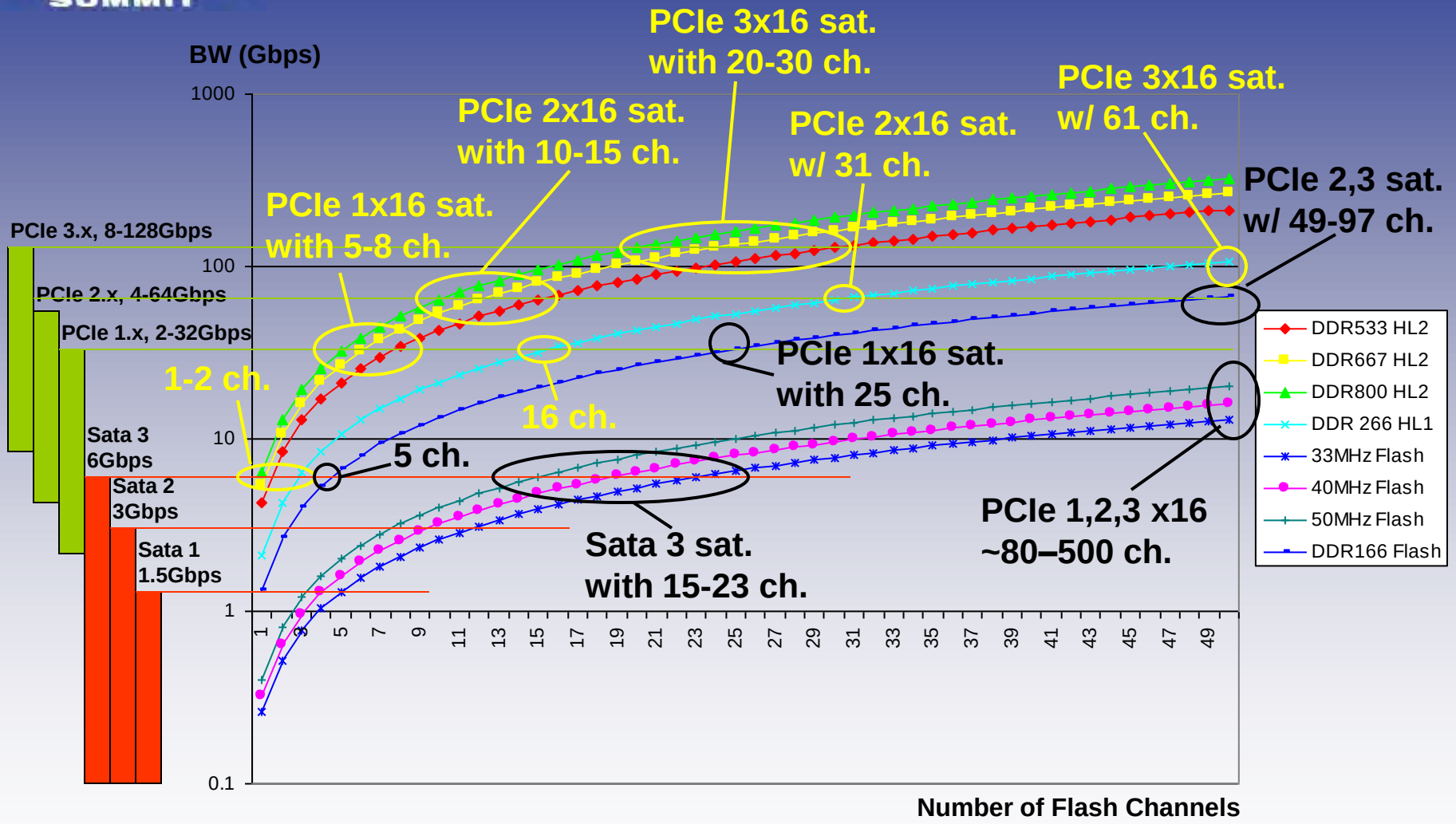


Simplification with HLNAND



- Requires fewer stages of protocol translation and fewer different devices
- Can implement host interface, controller, and flash interface in single ASIC
- HLNAND rings in RAID configuration
- Fewer channels to achieve maximum throughput; therefore lower ECC & IO costs

Bandwidth Growth with HLNAND



Summary

- Cutting edge is defined by enterprise space
- HLNAND2 provides 800MB/s/ch. transfer rate
- HLNAND2 throughput matched closely with high-speed system interconnect like PCIe 2.x & PCIe 3.0
- System design simplified with HLNAND
- Higher system throughput with less complexity
- Controller cost reduced through duplication reduction (ECC logic, IO)

Higher scalability in performance & capacity

Resource for HLNAND Flash

www.HLNAND.com