Progress and Prospect for MRAM

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Everspin Technologies, Inc.

Everspin Introduction

- Formed as Everspin in June 2008 – Previously part of Freescale Semiconductor
- The leading developer and manufacturer of integrated magnetic products
  - Industry-first MRAM supplier since June 2006
- Current MRAM products
  - Parallel interface products ranging from 256k-16Mb
    - Infinite endurance, >20 year data retention, 35 ns read & write speed
  - Serial interface products ranging from 256kb-1Mb
    - 40 MHz SPI interface, No write delay, infinite endurance

Everspin MRAM Technology
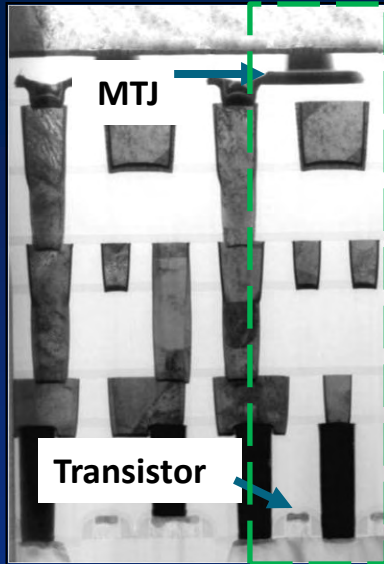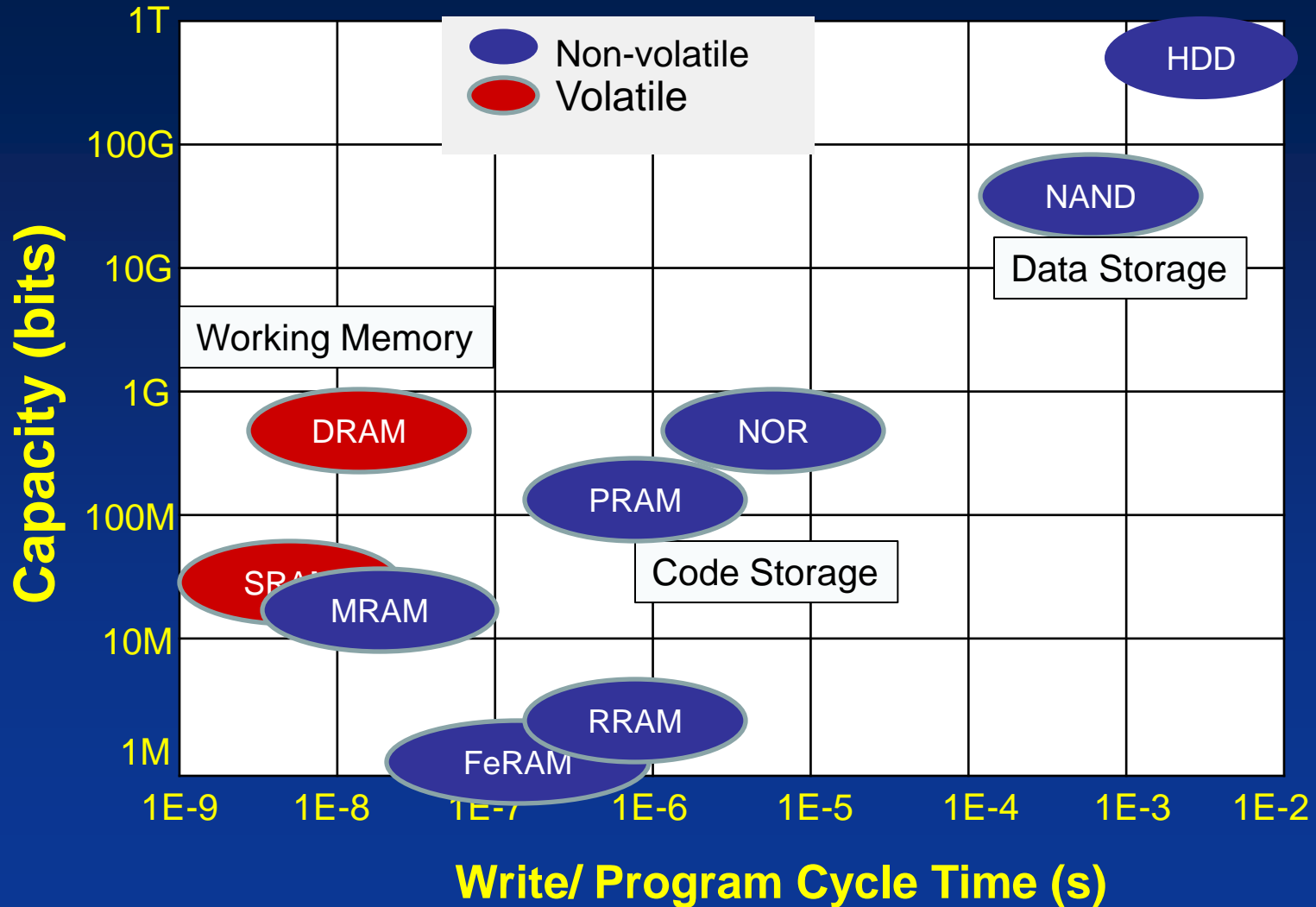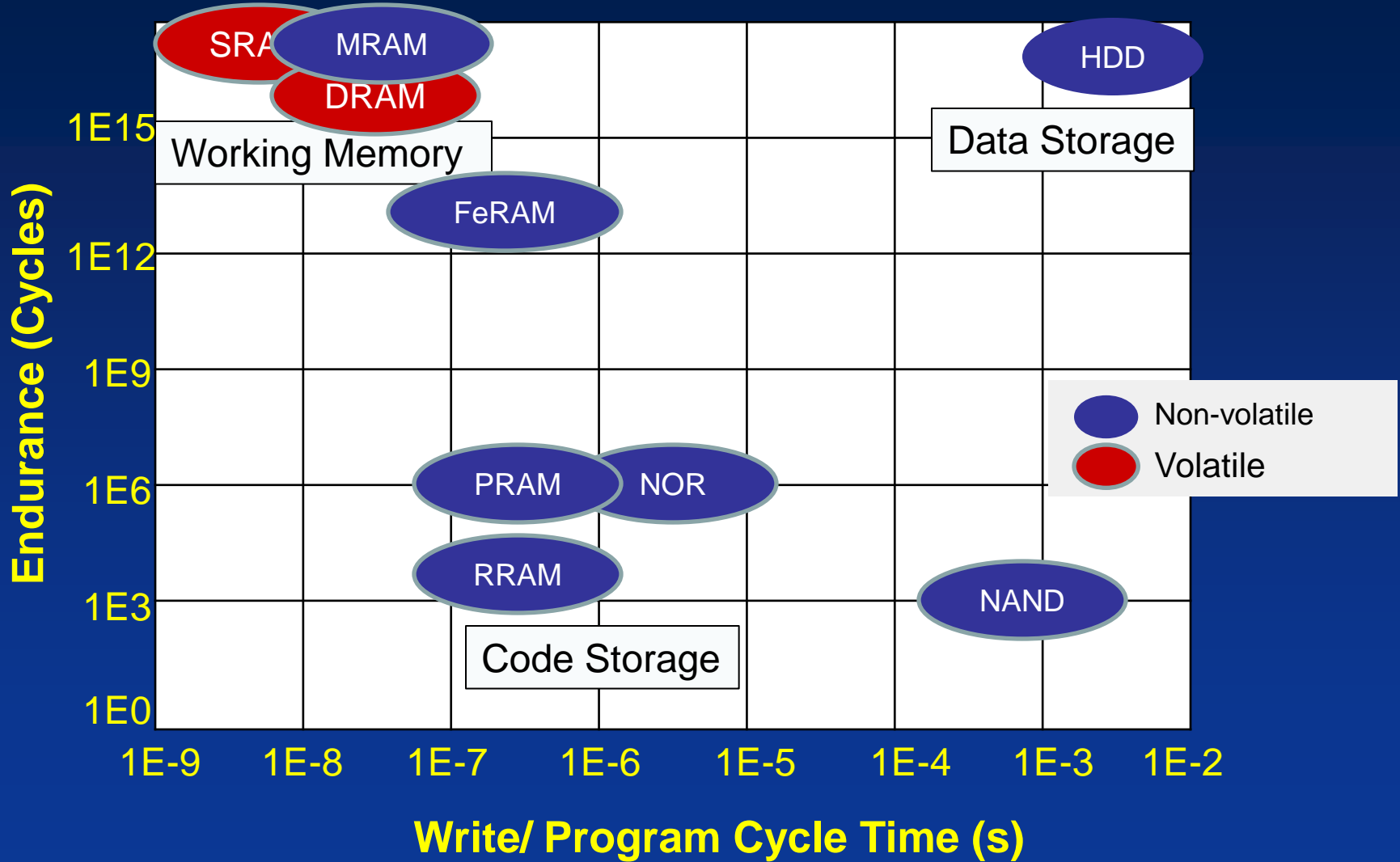

Cross-sectional view
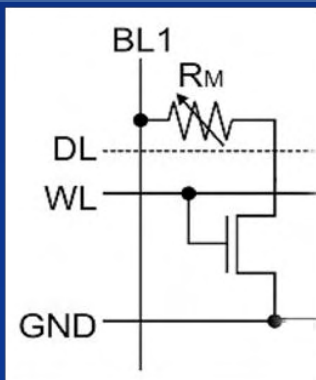
Circuit

- Simple 1 transistor + 1 MTJ memory cell
- Data stored in magnetic polarization, not charge
- State of bit detected as change in resistance
- Always non-volatile
- Non-destructive read, unlimited endurance
- Leverage CMOS semiconductor ecosystem
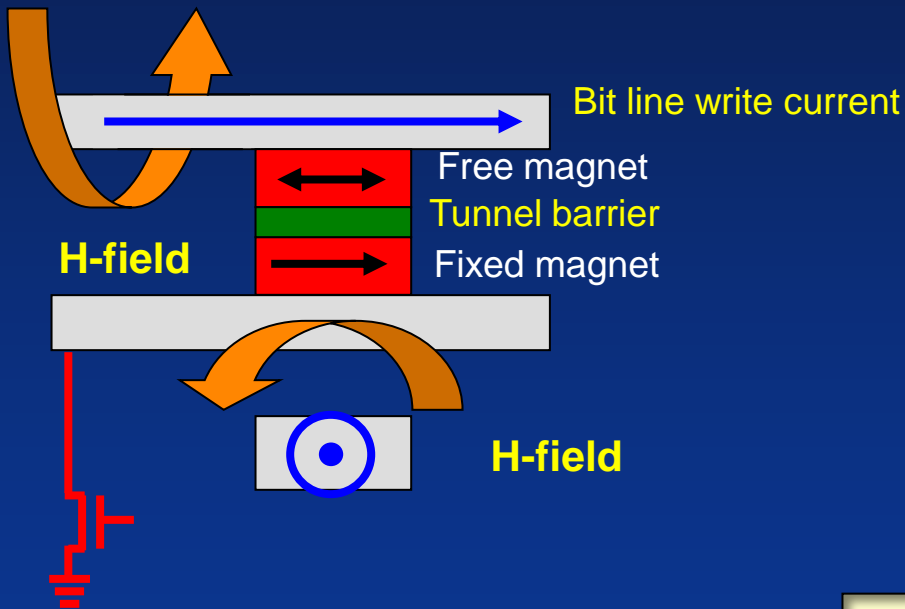- Everspin - "Electron spin is forever"

magnetic layer 1 (free layer)

tunnel barrier

magnetic layer 2 (fixed layer)

LOW RESISTANCE

HIGH RESISTANCE

Memory Capacity vs. Cycle Time

Memory Endurance vs. Cycle Time

Endurance (Cycles) vs. **Write/ Program Cycle Time (s)**

- SRAM
- MRAM
- DRAM
- HDD
- FeRAM
- PRAM
- NOR
- RRAM
- NAND

Working Memory
Data Storage
Code Storage

Legend:
- Non-volatile
- Volatile

Y-axis: 1E0, 1E3, 1E6, 1E9, 1E12, 1E15

X-axis: 1E-9, 1E-8, 1E-7, 1E-6, 1E-5, 1E-4, 1E-3, 1E-2

MRAM bit switching

Toggle-MRAM
in production

Bit line write current

Free magnet

Tunnel barrier

H-field

Fixed magnet

H-field

- Cross-point architecture
- Current along bit line and digit line to switch at intersection

ST-MRAM
in development

I_{DC}

Isolation transistor
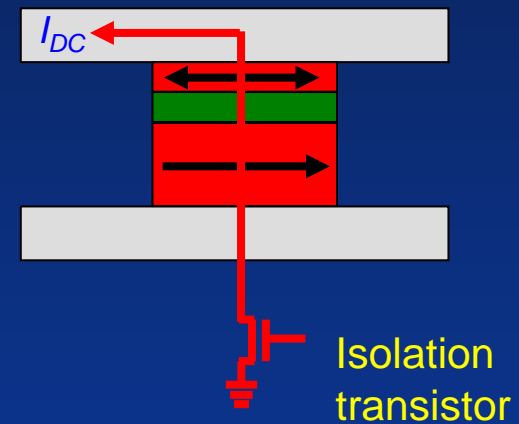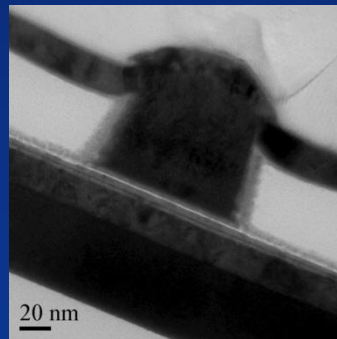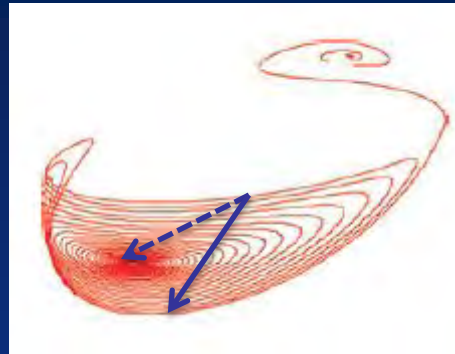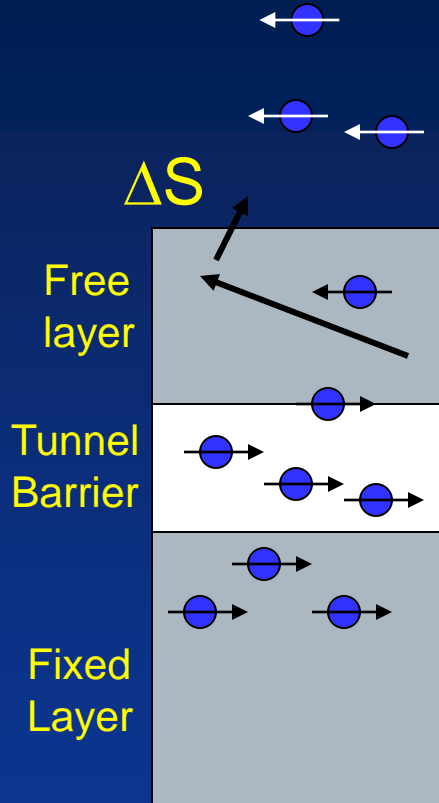
- Current I_{DC} flows through MTJ and transistor
- Fixed magnet polarizes I_{DC}
- Spin-transfer torque programs free magnet
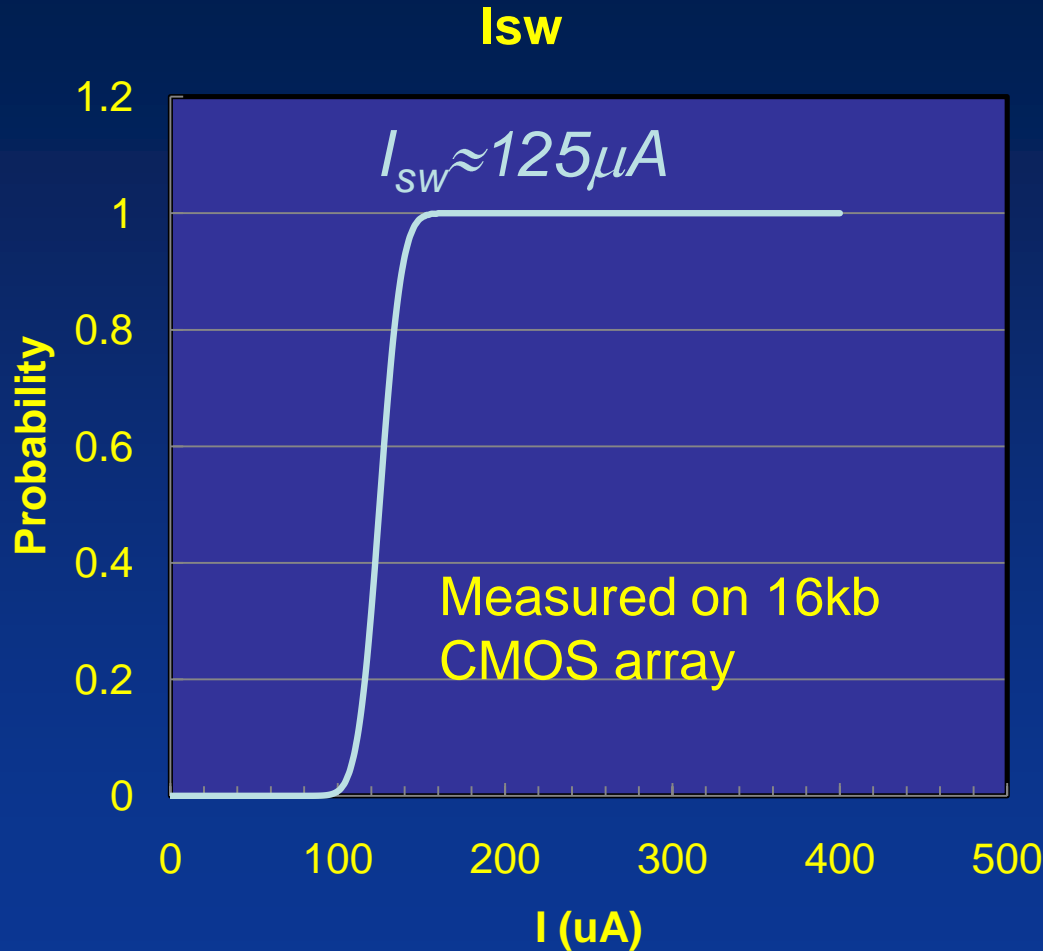 - Conservation of angular momentum

Spin Torque MRAM

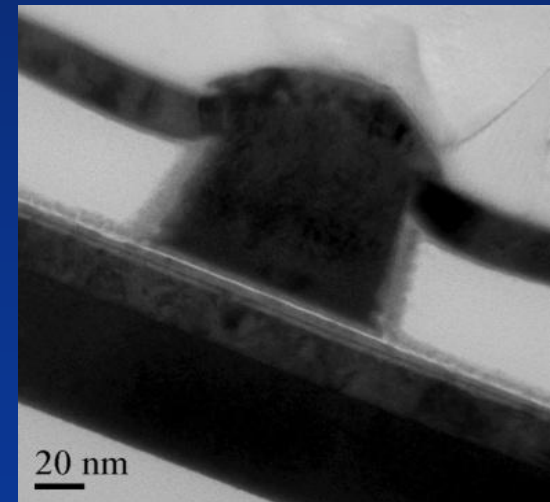Use spin momentum from current to change direction of *S, m.*

$$\frac{\Delta S}{\Delta t} = Torque$$

ΔS

Free layer

Tunnel Barrier

Fixed Layer

Rmax

Resistance (Ω)

MR

Rmin

Current (mA)

20 nm

Low Switching Current

Isw

$I_{sw}{\approx}125\mu A$
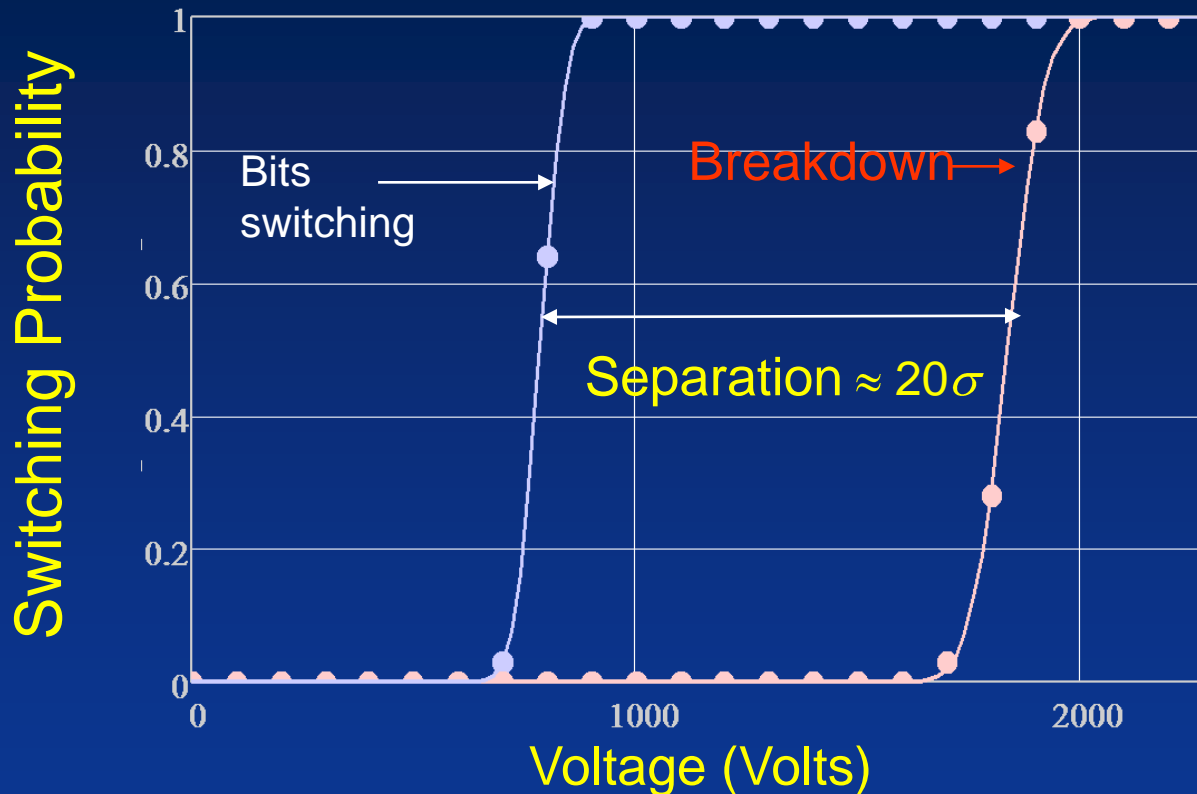
Measured on 16kb CMOS array
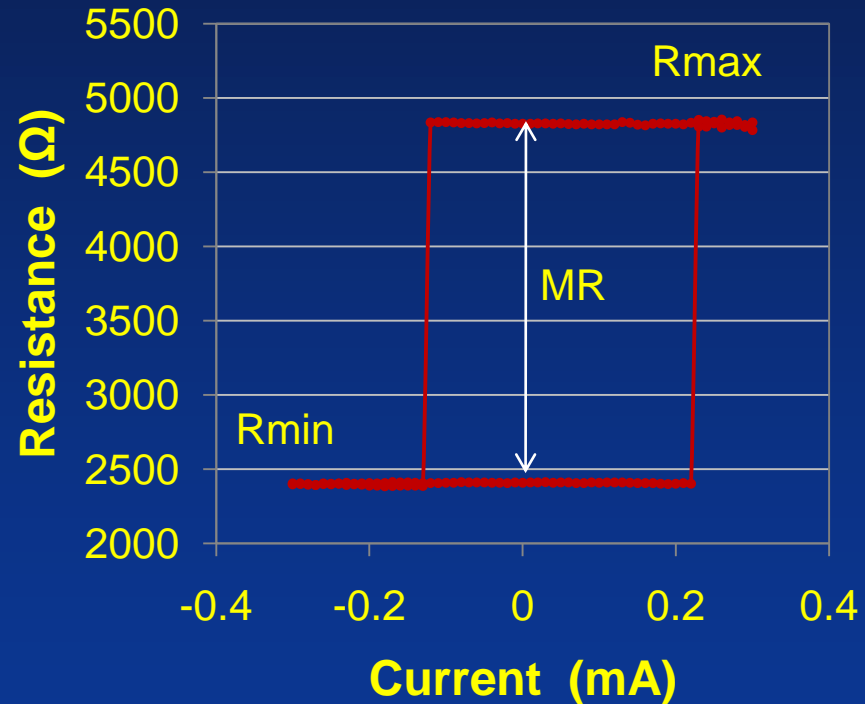
- Demonstration of low write current with 60nm bits
- Energy barrier = 60kT

20 nm
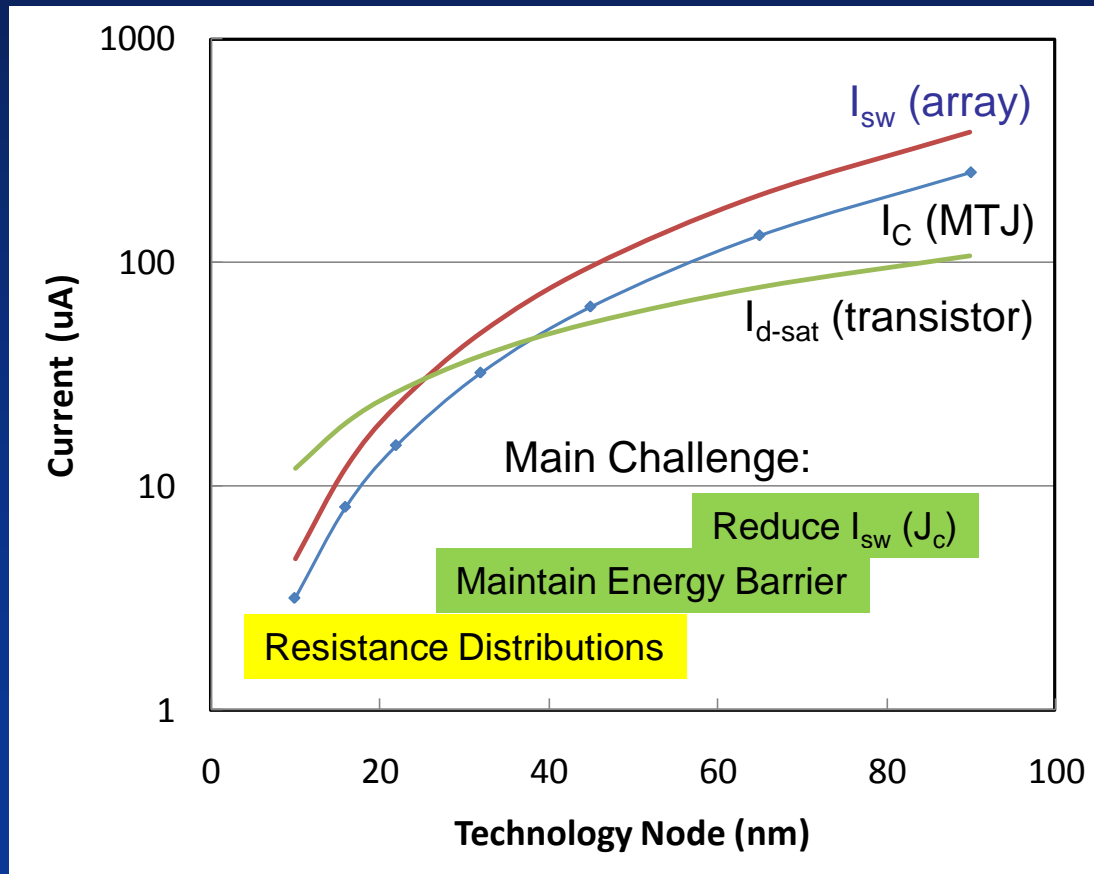
Large Separation of V_{sw} and V_{bd}

16kbit integrated CMOS arrays

- Excellent separation $\approx 20\sigma$, due in part to $\sigma_{sw} \approx \sigma_{bd} \approx 4\%$

Scaling ST-MRAM

- Today: Reduce J_c for reliability and smaller transistors
- Continued scaling: maintain energy barrier and manage resistance distributions

- ST-MRAM bits scale favorably to available current from transistor
  - Low Jc for reliability is the bigger issue
- Continued scaling requires innovative magnetic devices and materials
  - Enhanced energy barrier
  - Increased TMR

I_c calculated for J_c=2MA/cm^2

Summary

- MRAM is a highly reliable, high-performance, nonvolatile memory IC, with unlimited endurance

- MRAM has the unique characteristics of a working memory while providing non-volatility

- Current MRAM product densities range from 256kb-16Mb

- Higher density MRAM products in development will utilize Spin Torque switching and will maintain MRAM's unique characteristics