The Operation Algorithm for Improving the Reliability of TLC (Triple Level Cell) NAND Flash

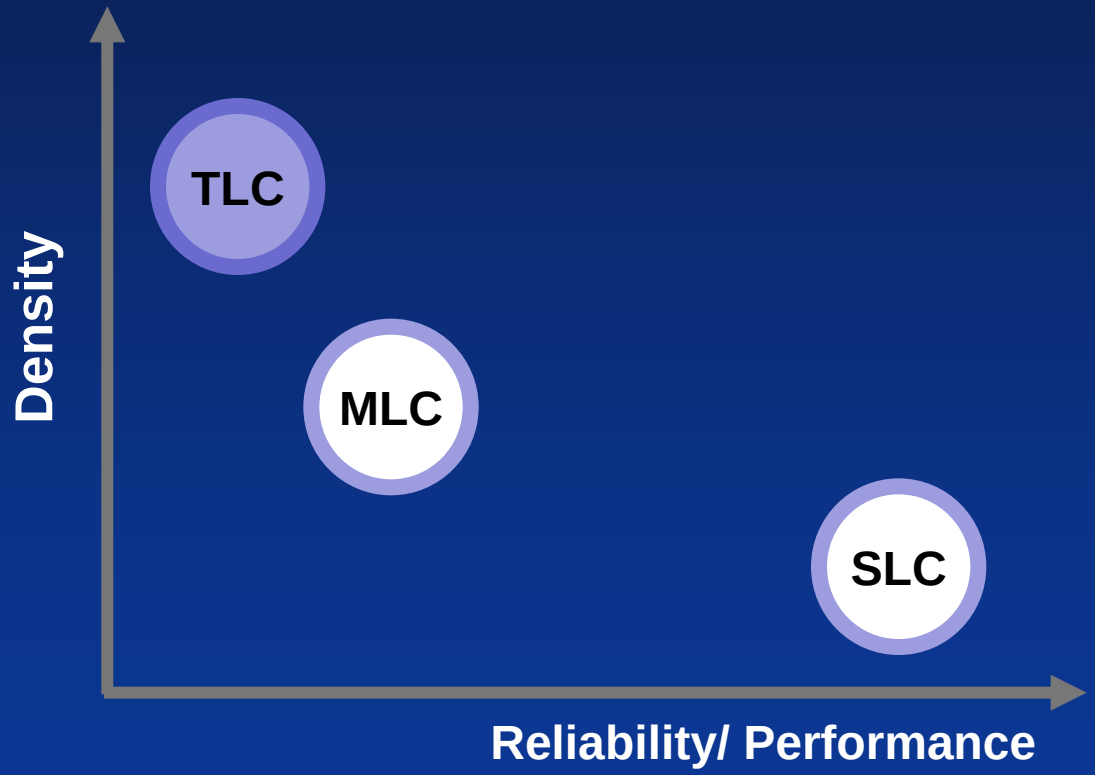
YeonJoo Jeong, Sukkwang Park,
Myoung Kwan Cho, Kun-Ok Ahn and Yohwan Koh
Hynix Semiconductor Inc.

Contents

- Introduction
- Read Operation : Moving Read
  Interference Cancellation
  Negative WL Bias
- Erase Operation : Alternative Erase and Verify
  Erase Pulse Optimization
- Program Operation : Data Randomization
  Controllable Bias for Each WL
  De-trapping Trapped Charges

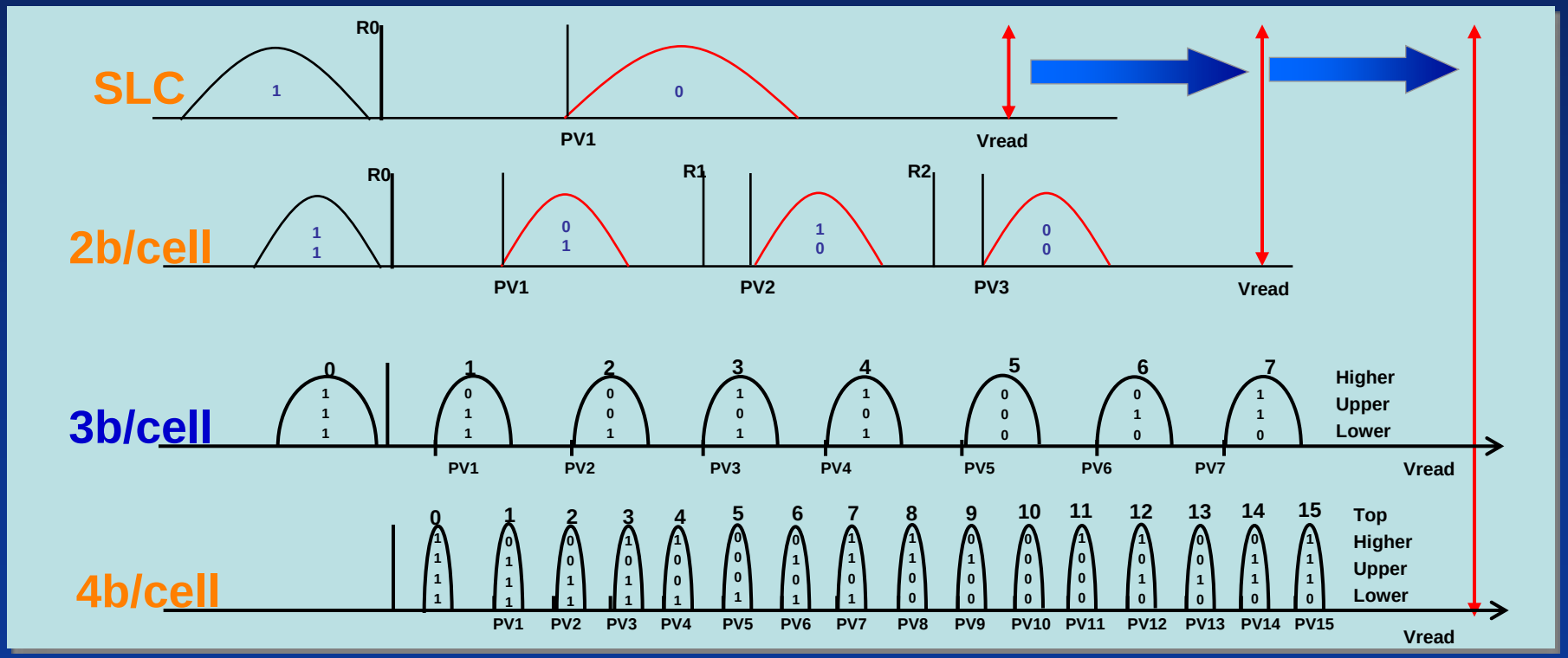
Introduction

- **Solution for Larger Density & Competitive Price**



Introduction

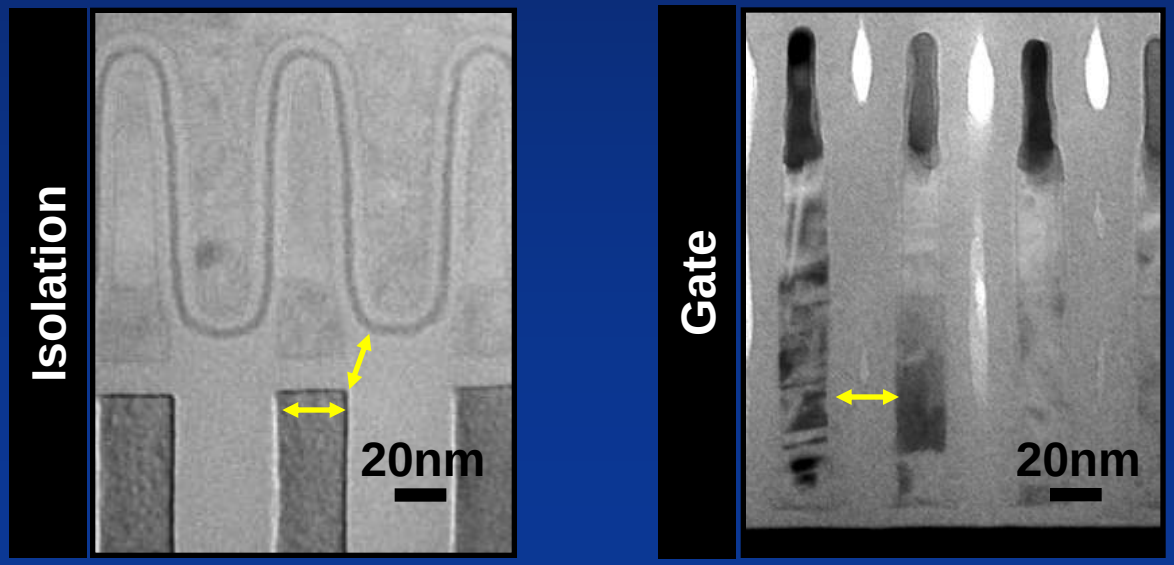
- TLC : To achieve the larger capacity of NAND Flash
- TLC has more levels of V_{th} distribution per cell than MLC
- The cell V_{th} distribution should be tightly controlled
- Operation conditions should be optimized for reliability



Scaling Barriers in NAND Flash

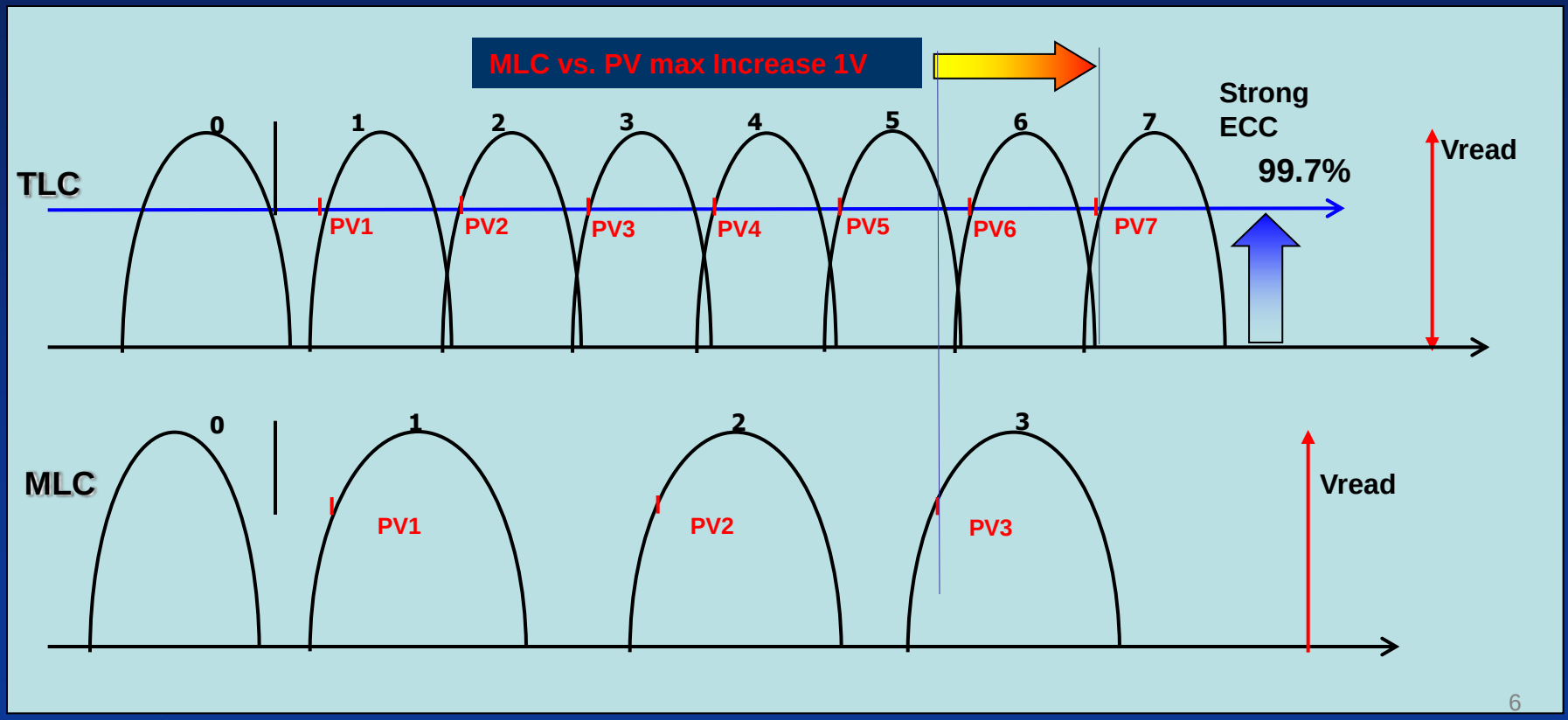
Geometry	Small Coupling Ratio, Small On Current
Narrow Operating Window	Interference, Disturbance, EW Stress
Process Sensitivity	Less Tolerance in Process Variation

[NAND Flash Structure]



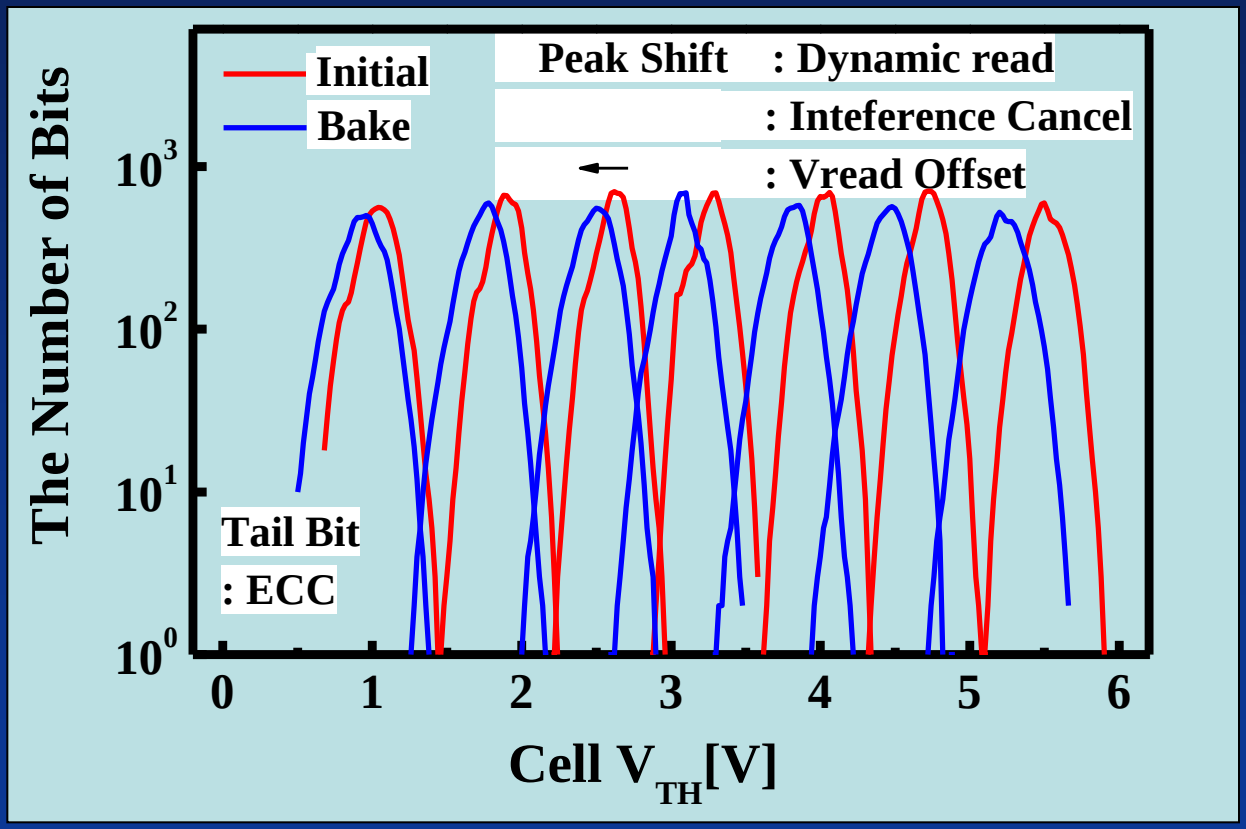
Narrow V_{th} Window

- In MLC : [PV3 (4V) – PV1 (0.4V)] / 3 Level ➔ 1800mV / Level
- In TLC : [PV7 (5V) – PV1 (0.4V)] / 6 Level ➔ 760mV / Level
  - Needs More tightly controlled V_{th} distribution



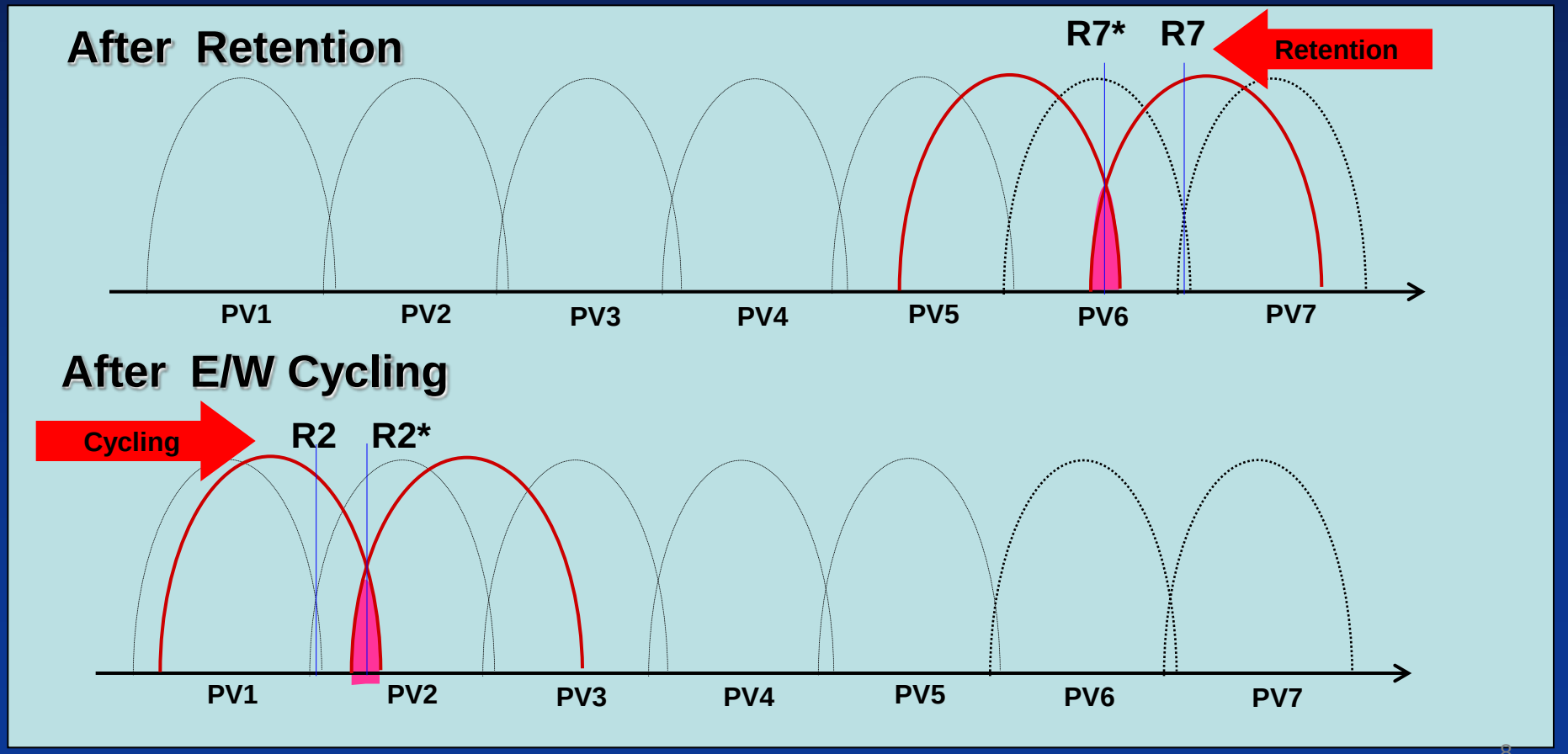
V_{th} Distributions in TLC

- Narrow V_{th} window in TLC
- Needs Moving read, Interference cancellation, Data Randomization and Reduce degradation in EW Cycles



Dynamic Read

- V_{th} distribution changes after E/W or Retention
- To find the minimum fail bits,
  read level changes interactively : R7 → R7* or R2 →R2*



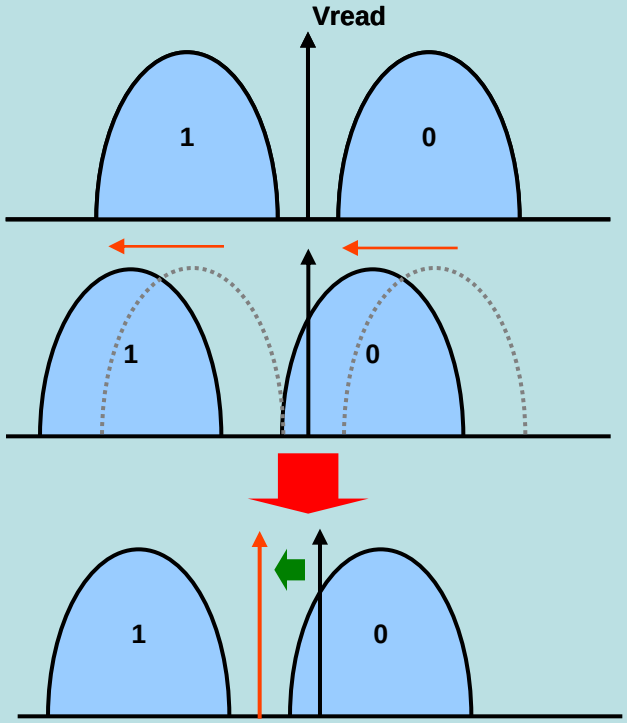
Dynamic Read

- Moving read algorithm motivated by changed V_{th} distribution
- Getting the distribution of every bits, we can use it at the error correction

Ideal state

After Stress

Changing Level



- ‘1’ : 2KB
- ‘0’ : 2KB

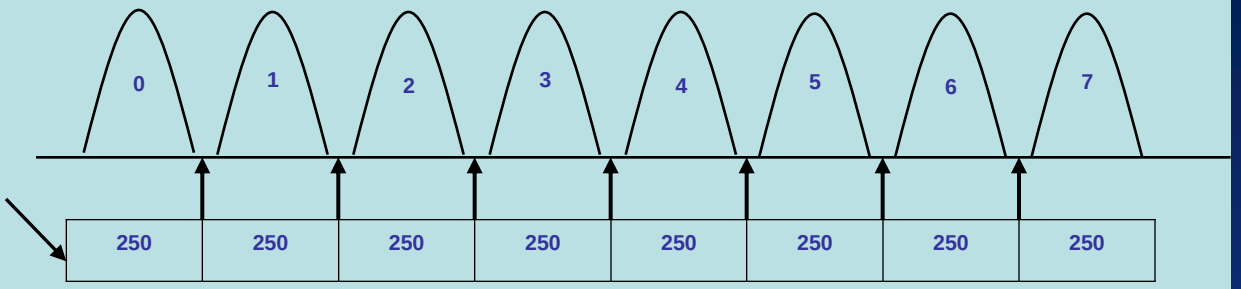
- ‘1’ : 2KB
- ‘0’ : 2KB - α

- ‘1’ : 2KB
- ‘0’ : 2KB

Dynamic Read

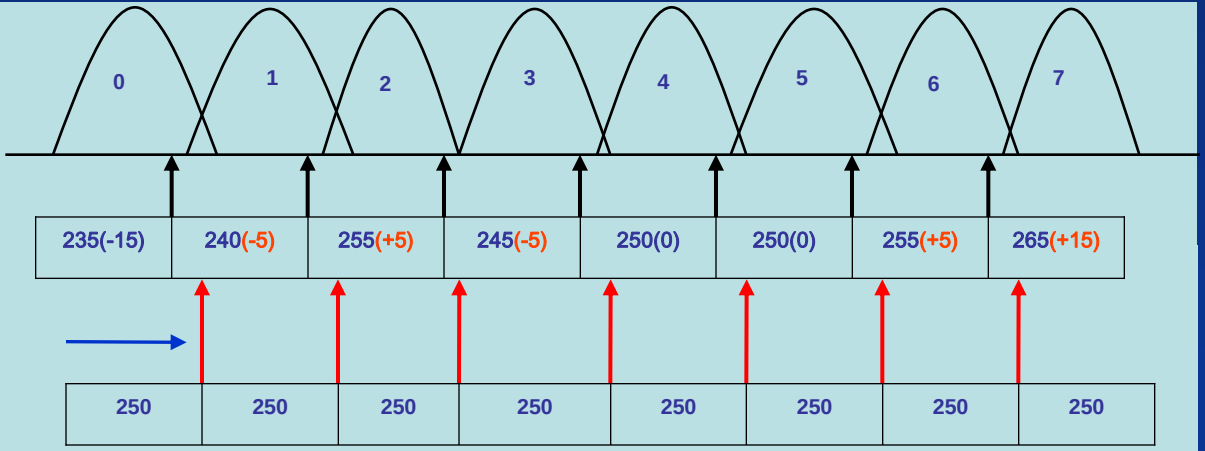
- In Ideal Randomized state, each cell distribution has 2K cells

Ideal state



After E/W Cycles, Retention,

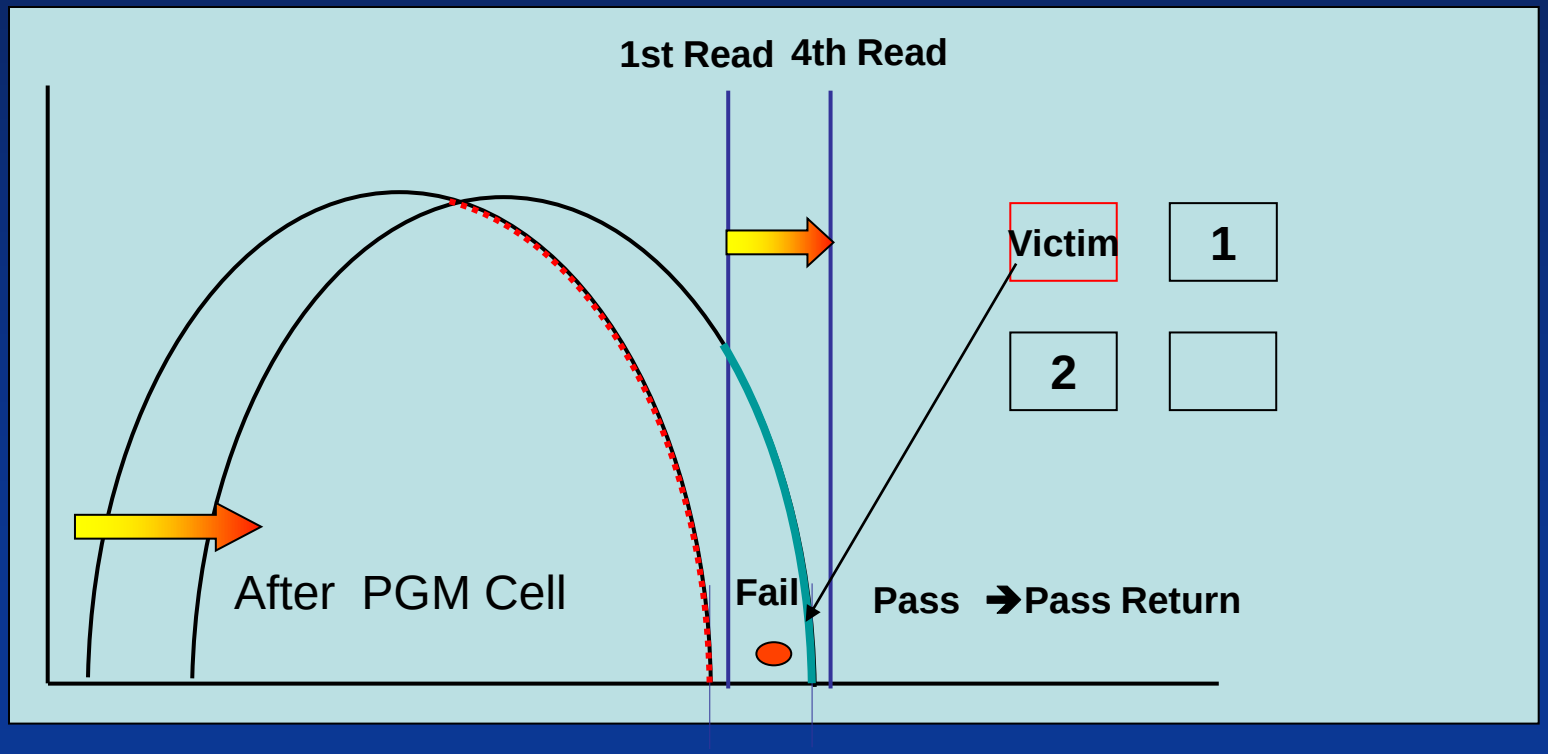
After Changing Read Level



Changed read level can compensate the V_{th} shift

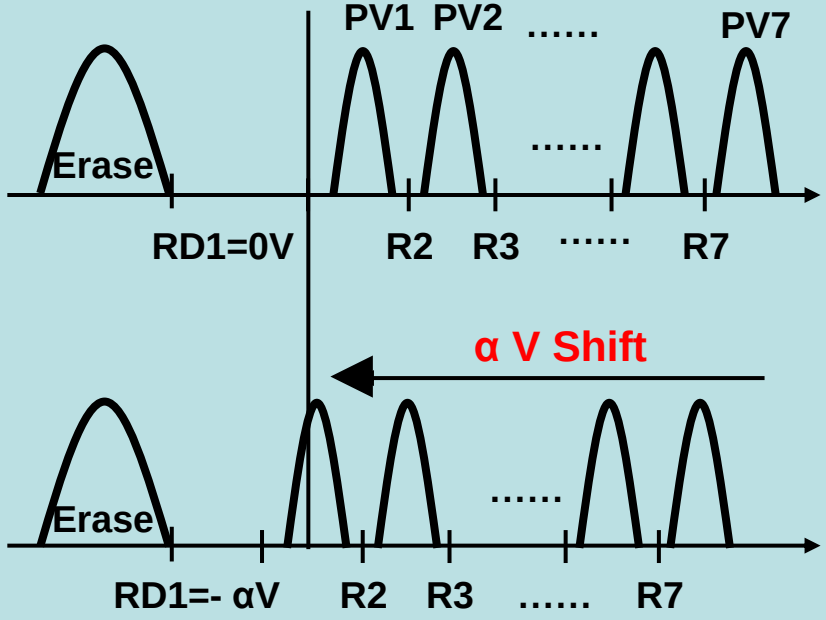
Interference Cancellation

- 1st Read : Fail
- 2nd Read : Checking the status of adjacency Cell (1)
- 3rd Read : Checking the status of adjacency Cell (2)
- 4th Read : Change read level : 1st Read Level + Interference Value



Negative WL Scheme

- The V_{th} distribution shifts to left side virtually with - α V
- The burden of high PV level can be relieved
- The PV margin can be enlarged



Conventional

PV1=0.5V, PV7 =4.5V

RD1=0V

Negative αV

PV1=0.5- α V, PV7=4.5- α V

RD1=- α V

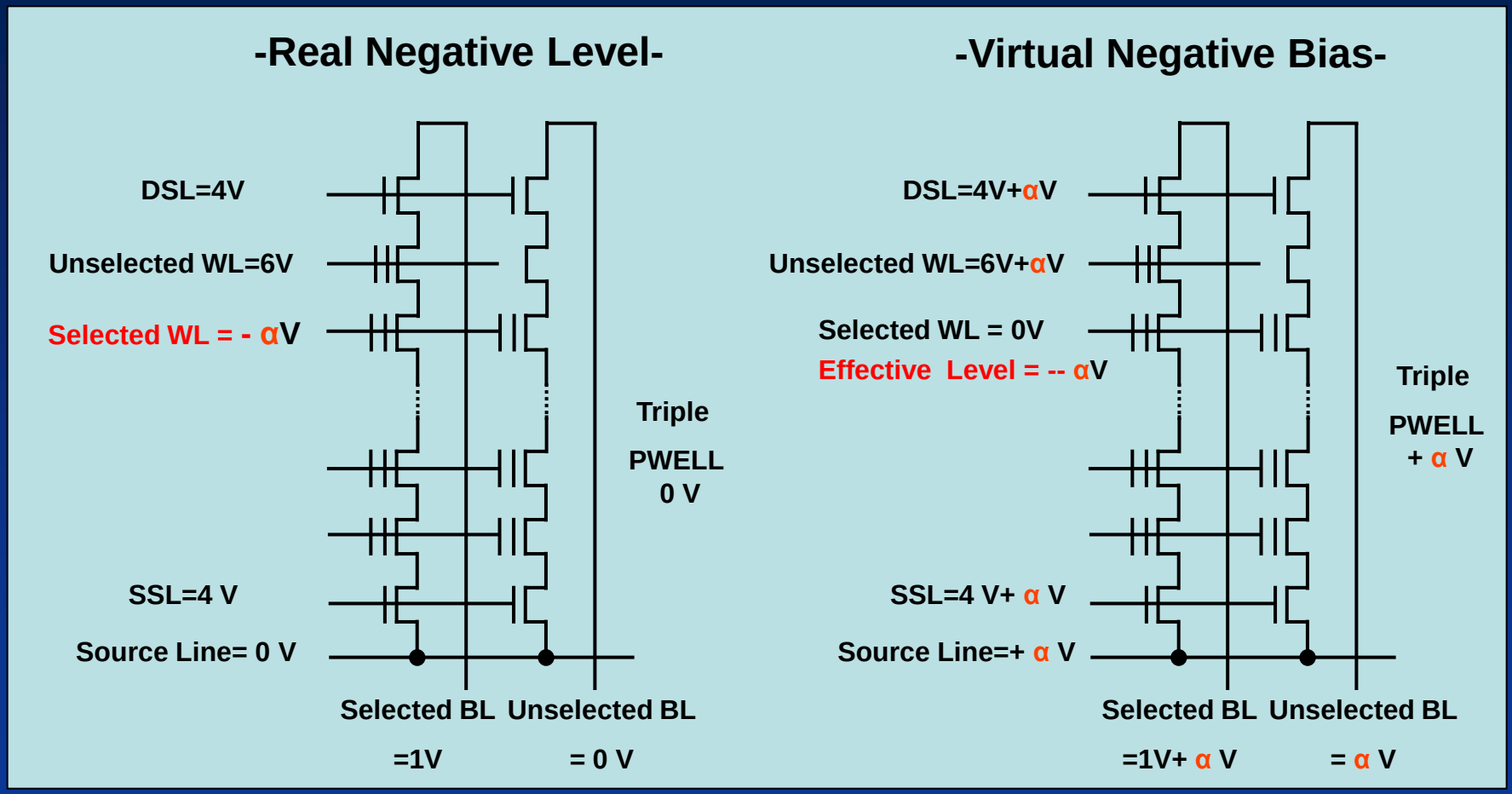
Negative WL Scheme

- **Lowering PV1 Level → Maximizing Delta of PV7 between PV1**
- **Shifting PV1, PV7 → Lowering PGM Bias → Improving Disturbance**

	Real Negative Scheme	Virtual Negative Scheme
Merit	Stabilized bias	No Adding Process / Mask
	Simple Operation	-
Demerit	-	Complicated X-DEC Operation
	Transferring Negative Bias in Peri Circuit → Complicated Well Structure	Needing Time of Pre – Discharging TPWell → Performance Degrade

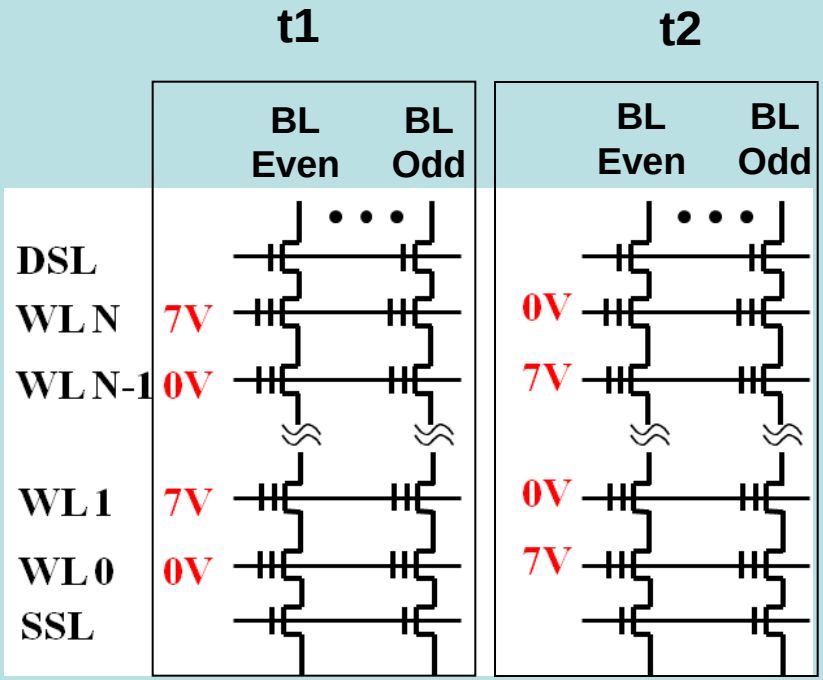
Negative WL Scheme

- If you need to get minus α V in verify operation



Alternative Erase and Verify (AEV)

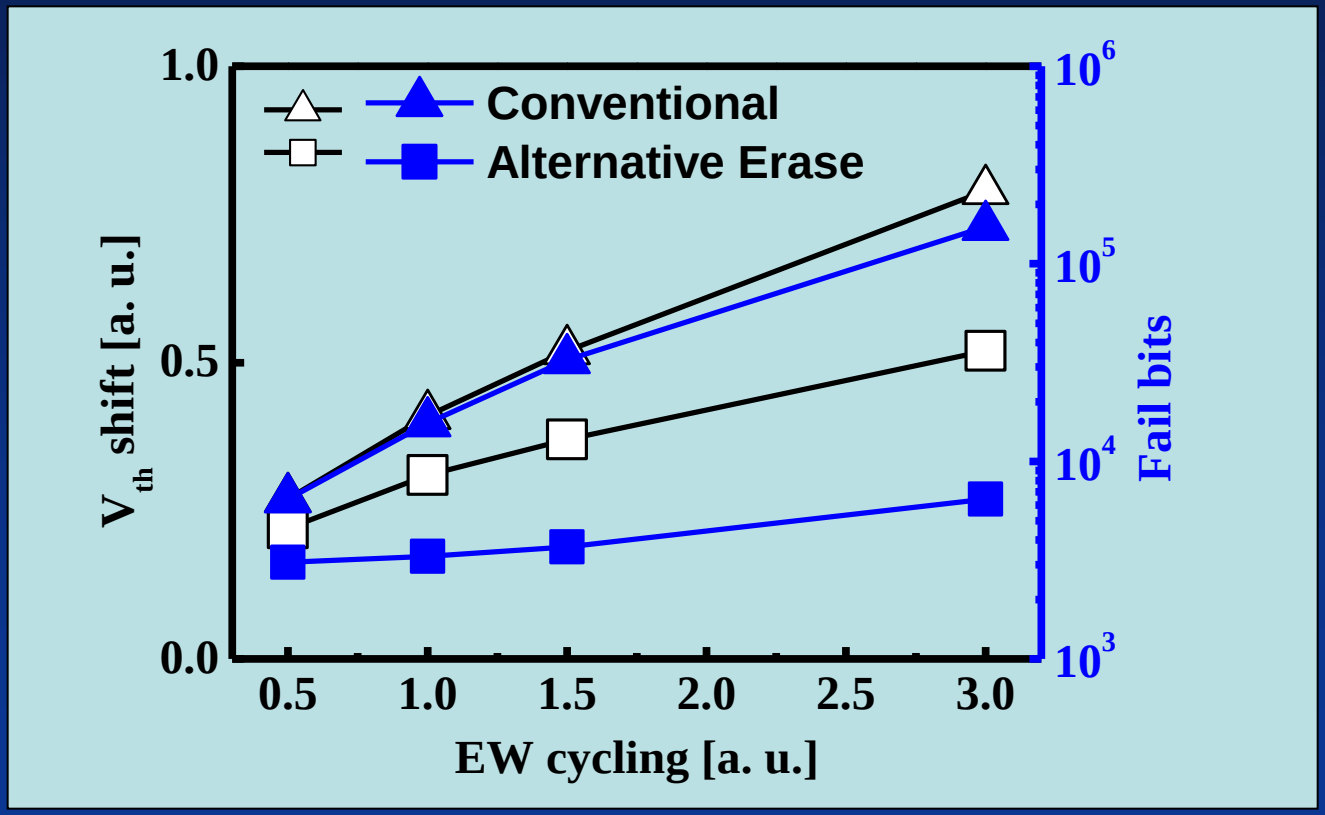
- Even/Odd W/Ls are separately verified with different bias level to avoid additional erase pulse caused by erase slow bits
- Only erase failed W/Ls (even/odd) are erased with ISPE bias



	t0	t1	t2
	Erase	Even WL Verify	Odd WL Verify
Even W/L	0 V	0 V	7 V
Odd W/L	0 V	7 V	0 V
TPWell	Erase Bias	-	-

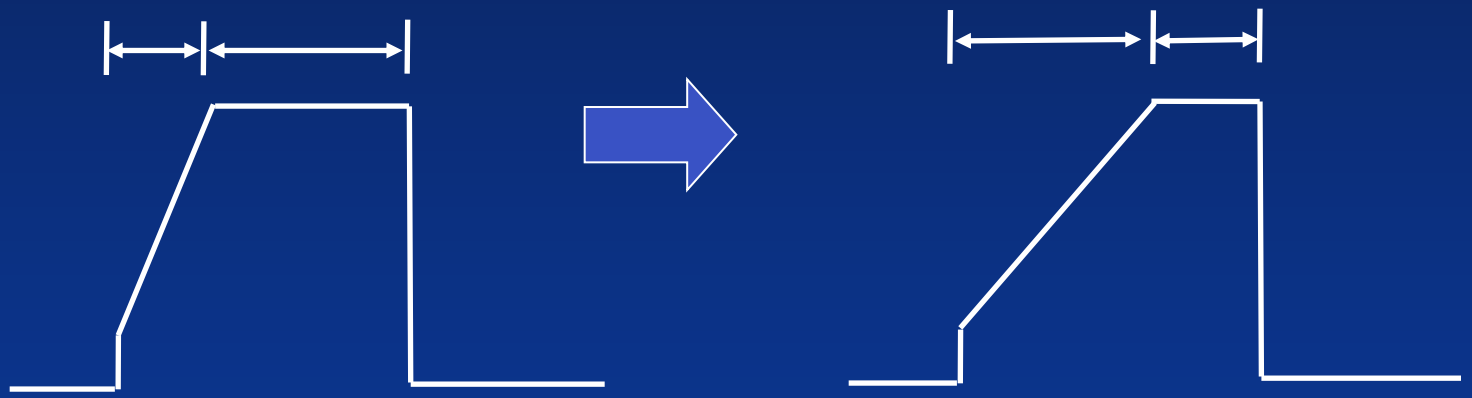
Alternative Erase and Verify (AEV)

- The AEV method reduce the EW degradation than conventional ISPE method, because of delaying starting next erase pulse



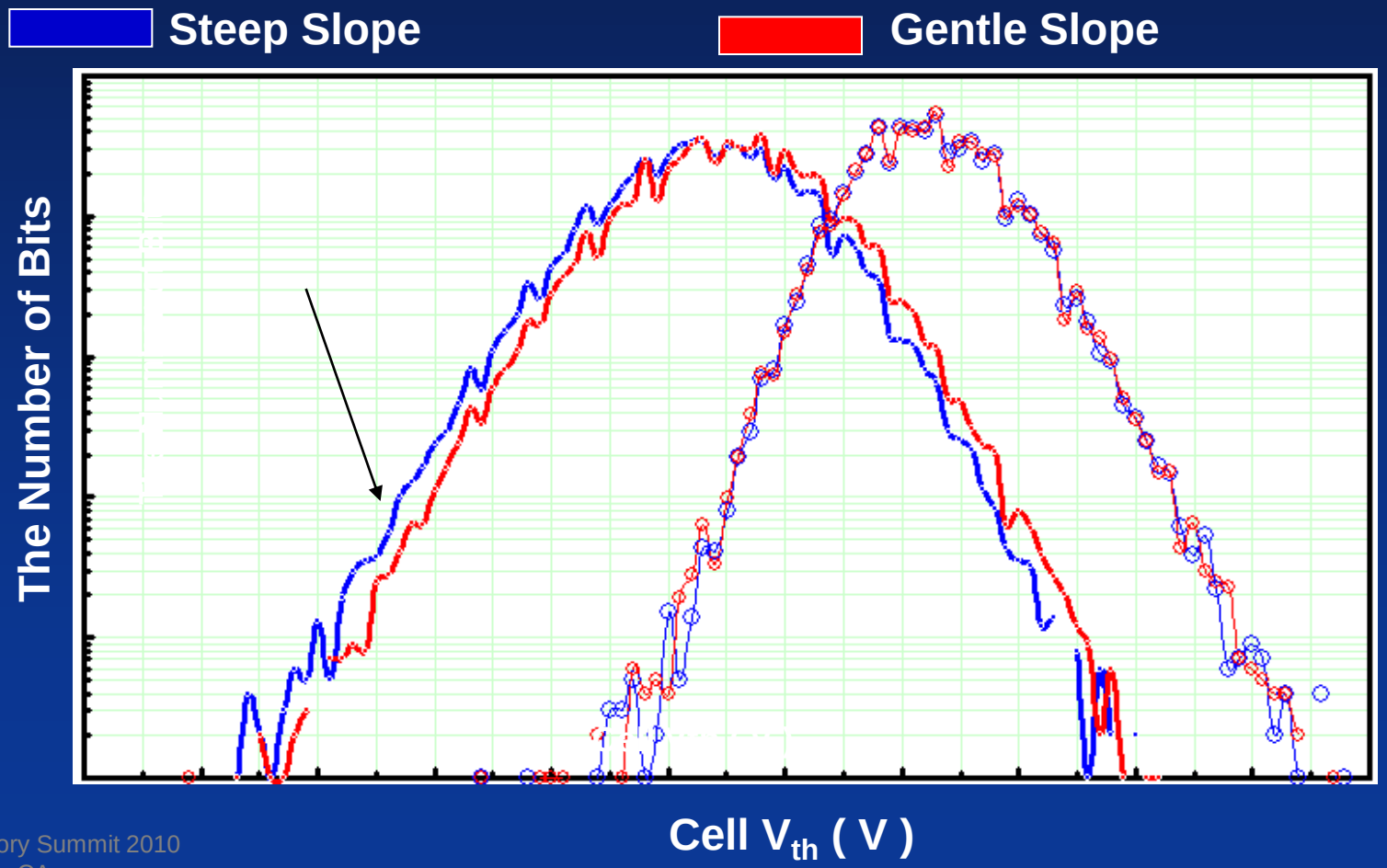
Optimizing Erase Pulse Shape

- TLC needs to reduce erase stress because PV7 is higher than PV3 of MLC
- Increasing the rising Slope
  - Reducing FN stress in Si / SiO_2 interface



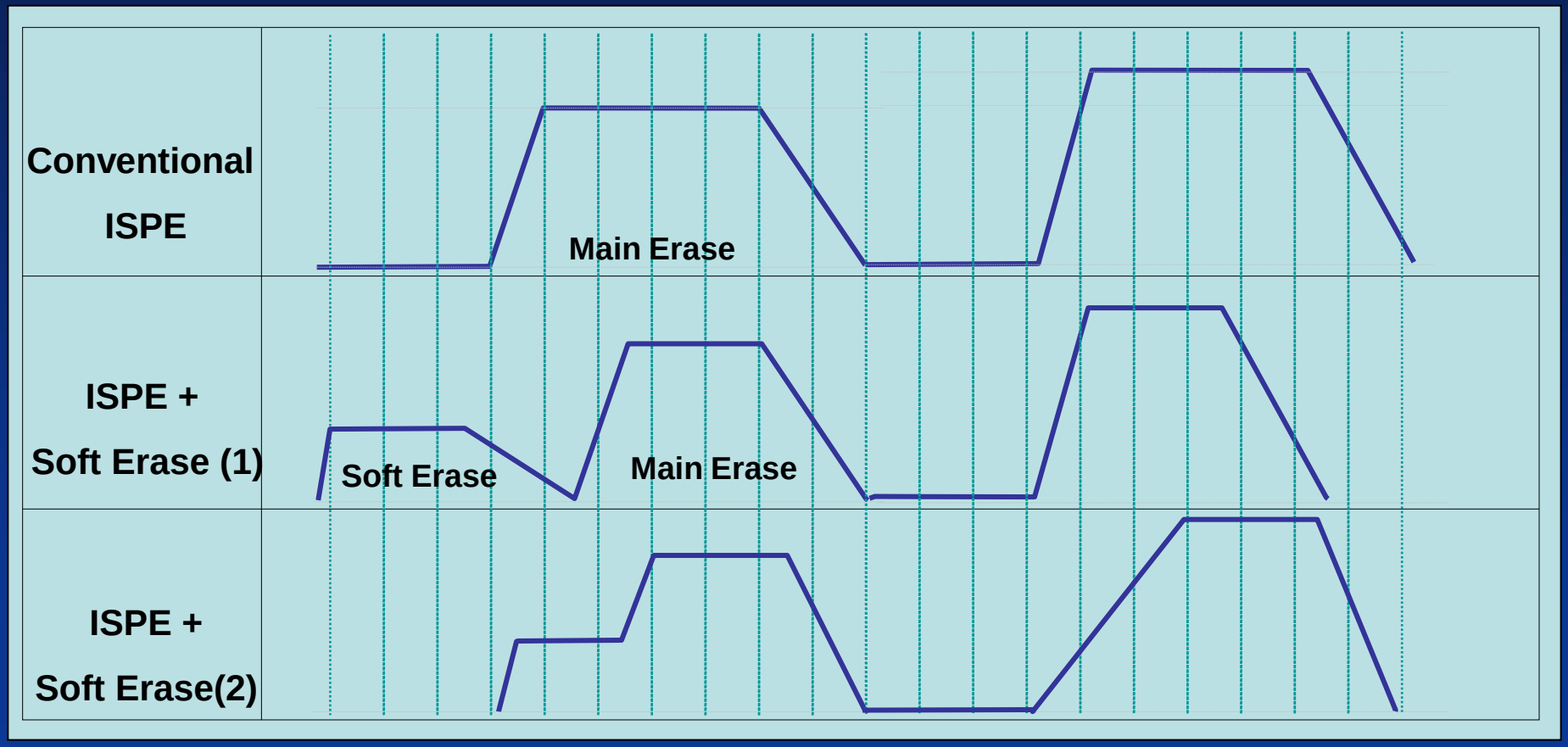
Optimizing Erase Pulse Shape

- Slow rising time relieve the reliability characteristics
  (EW Cycle 1K + Retention 0.5Y)



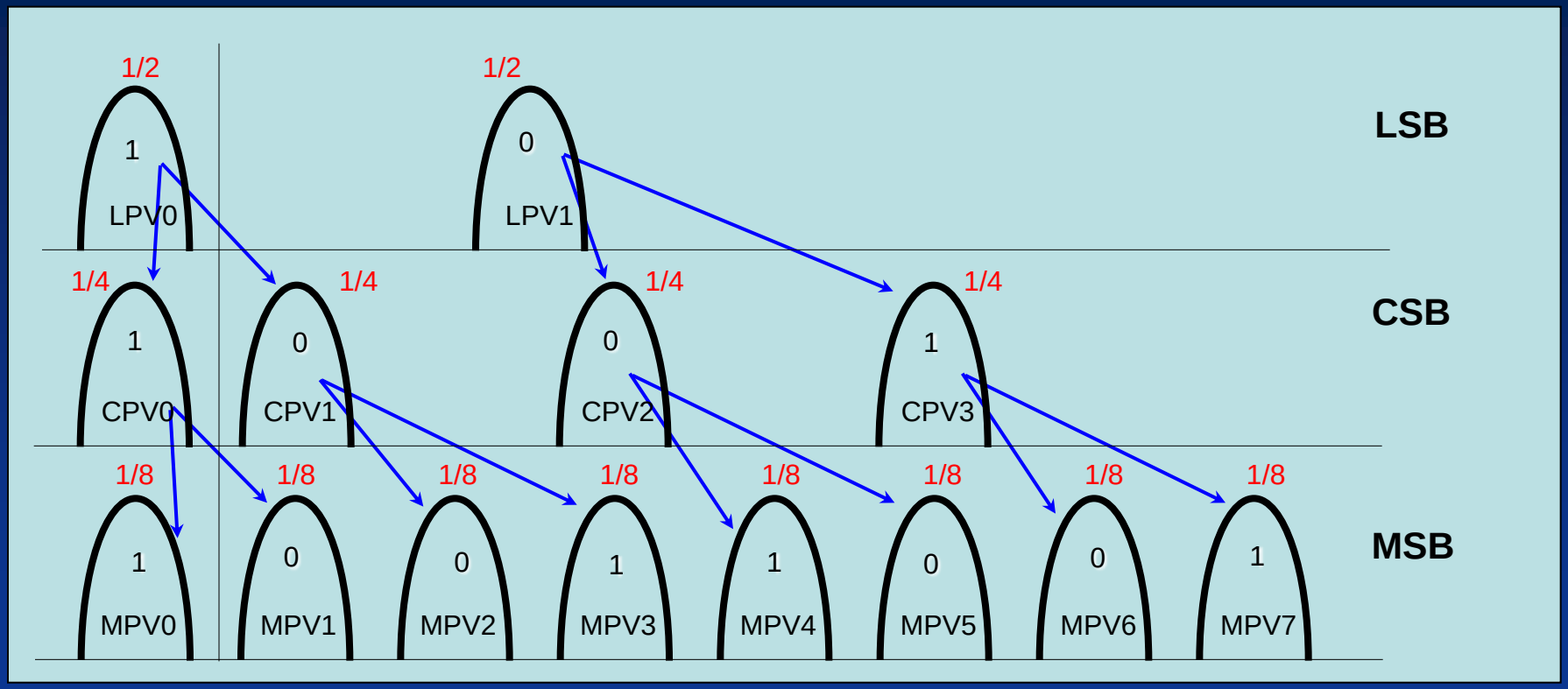
Soft Erase Scheme

- Soft erase can reduce erase stress, especially in PV 7, and also erase time can be reduced through optimization



Data Randomization

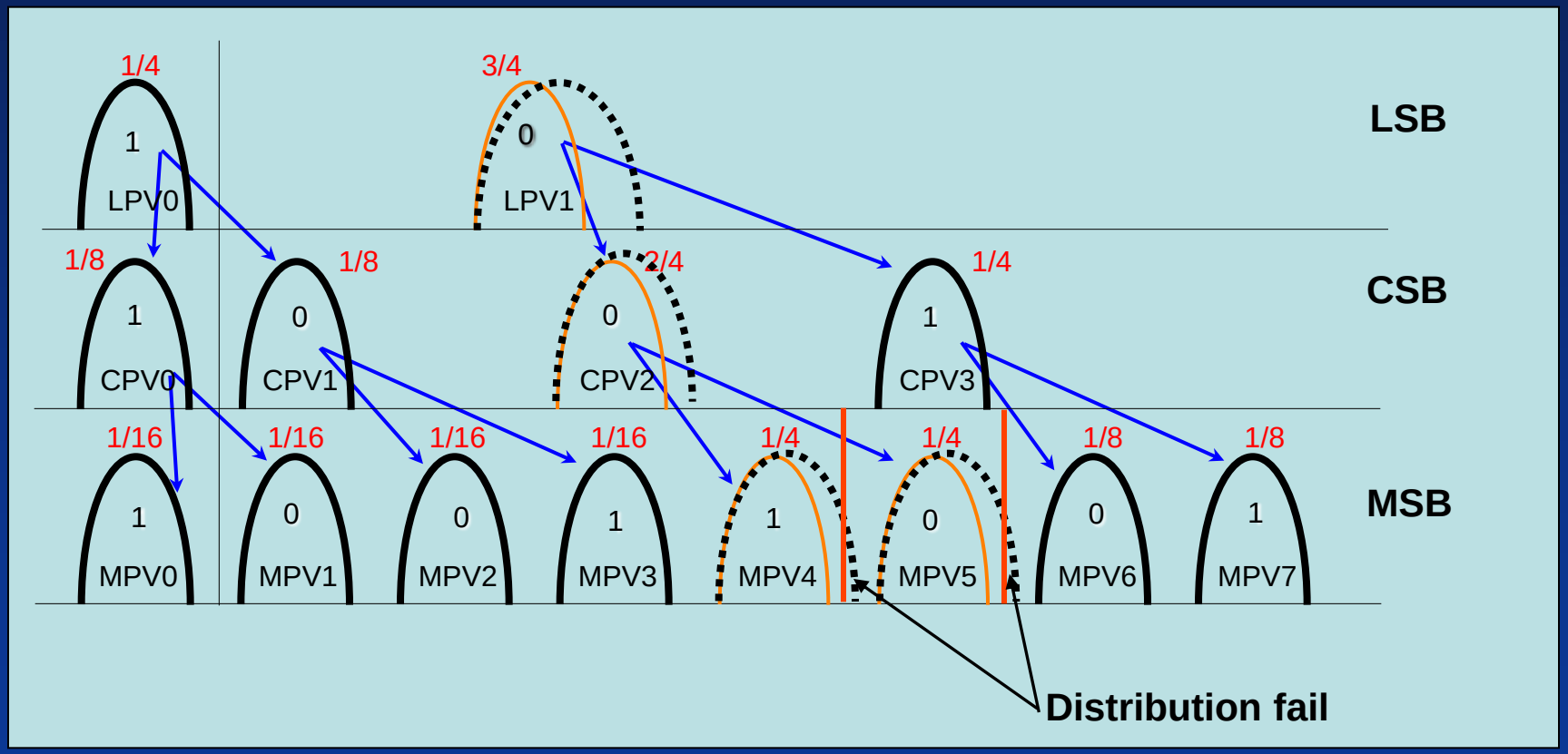
- All the cell are evenly distributed to each programmed levels



Schematic diagram of randomization process

Data Randomization

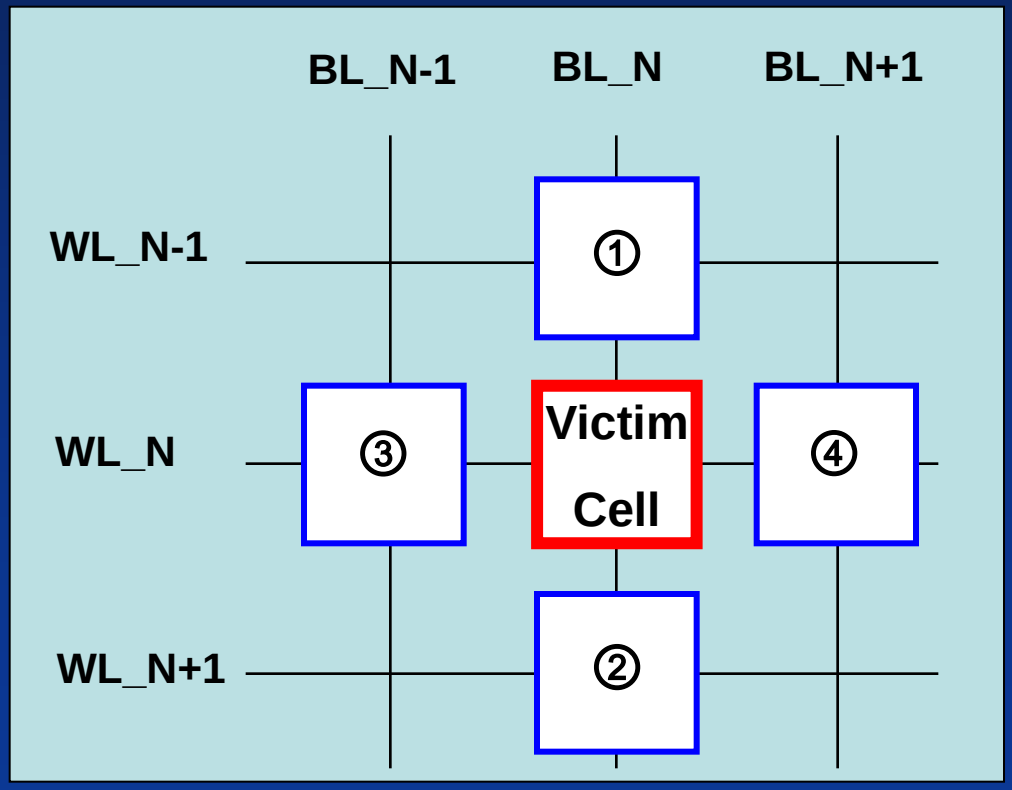
- Without Randomization
- Some levels are wider distribution than others
- Instabilities after retention or EW cycles



Data Randomization

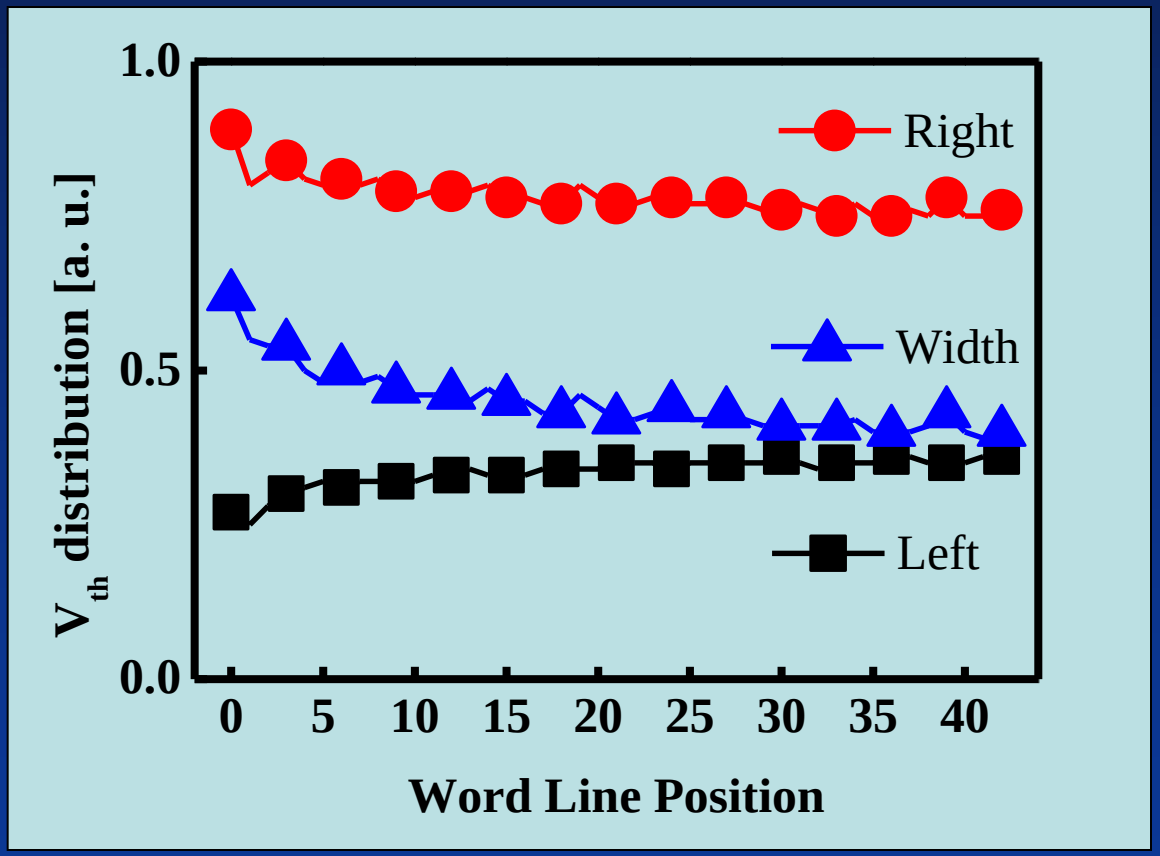
- The large PV level gap between victim and neighboring cells should be avoided in order to minimize the interference

  - Suggestion : 12 ≤ PV of ① + PV of ② + PV of ③ + PV of ④ ≤ 14



Independently Controlled Bias for Each W/Ls

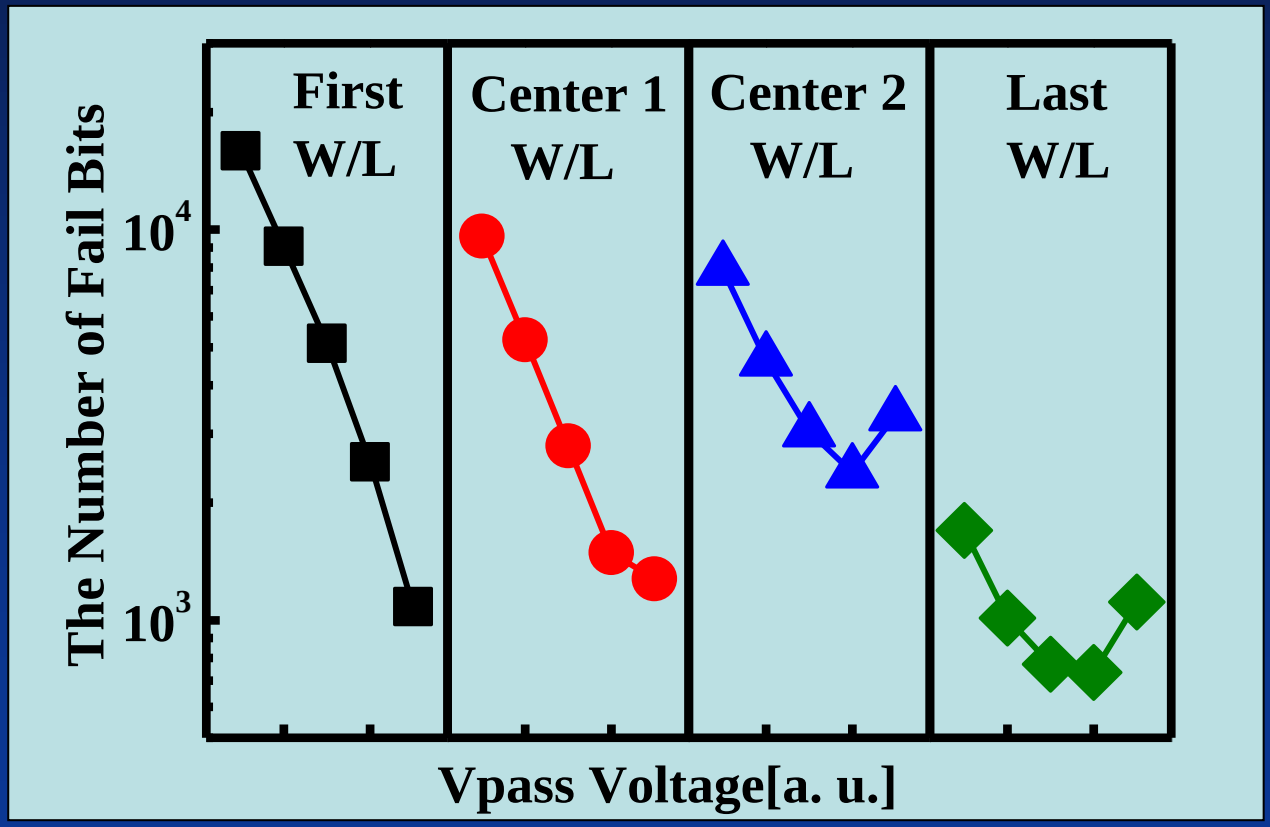
- Large numbers of W/Ls in a string
- The cell characteristics are widely varied with W/L position
- PV level and ISPP step should be controlled independently



The difference of PV1 distribution along the W/Ls

Independently Controlled Bias for Each W/Ls

- The number of fail bits are different as the cell position
  - Different V_{pass} in program bias should be used



The number of fail bits under program stress

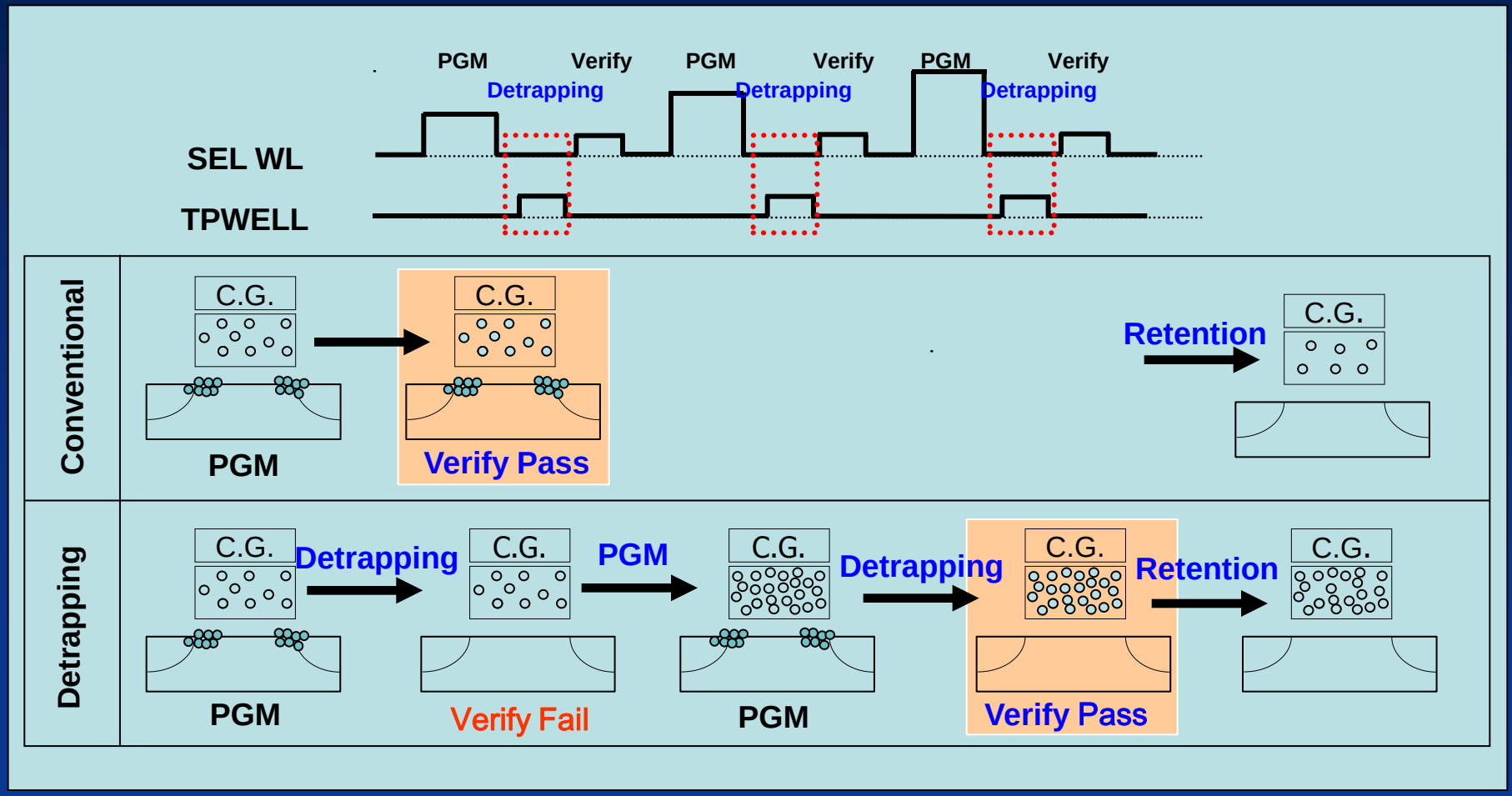
Independently Controlled Bias for Each W/Ls

- **Adjusting level of PGM/Read bias to maximizing reliability and performance**

	1st WL	Centered WL	Near by Last WL
ISPP Step	↓	↑	↑↑
V_{pass} in program	↑	-	↓
PV1 level	↑	↓	↑

Detrapping the Trapped Charges

- Remove the trapped charge before program verification by low erase pulse



Detrapping in E/W cycles

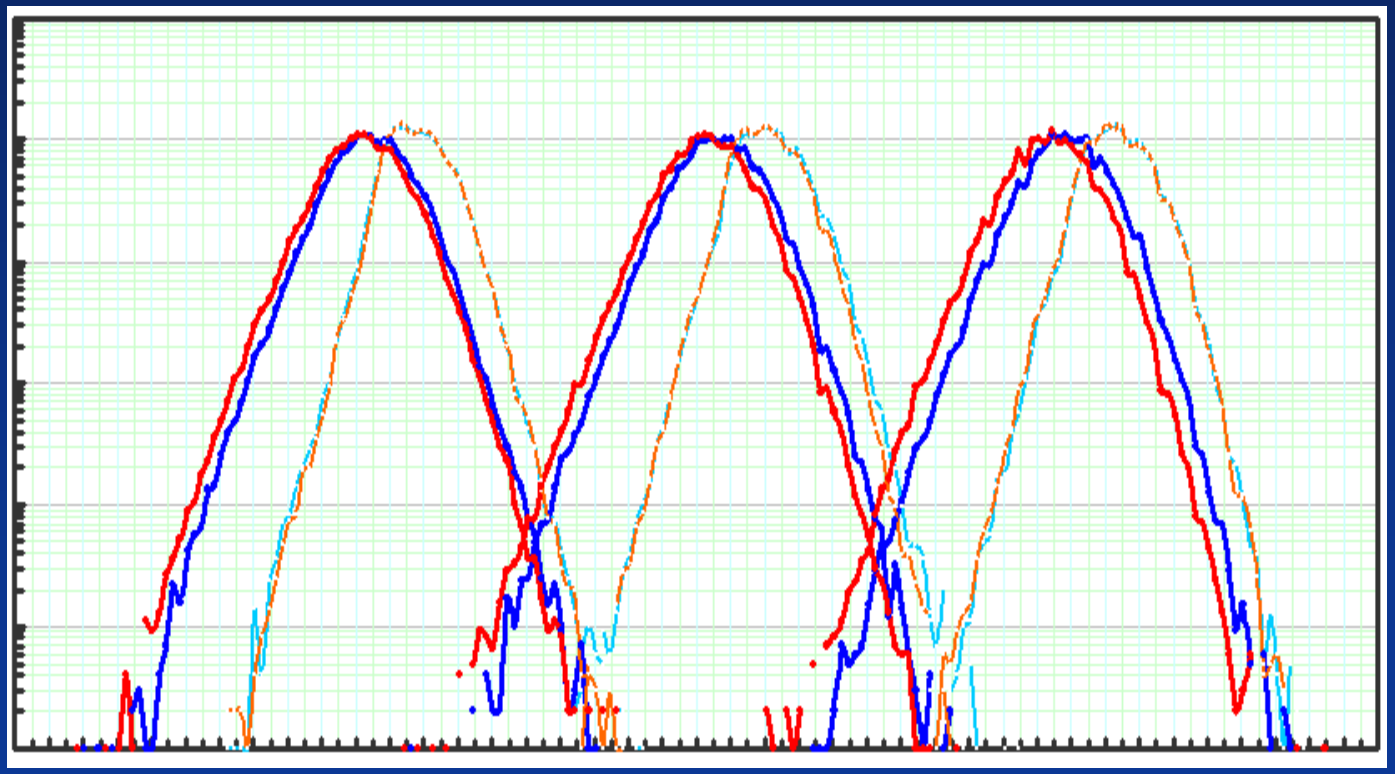
- The stress condition : E/W cycling 500cyc + Retention bake 0.5 yr

Cycling without detrapping

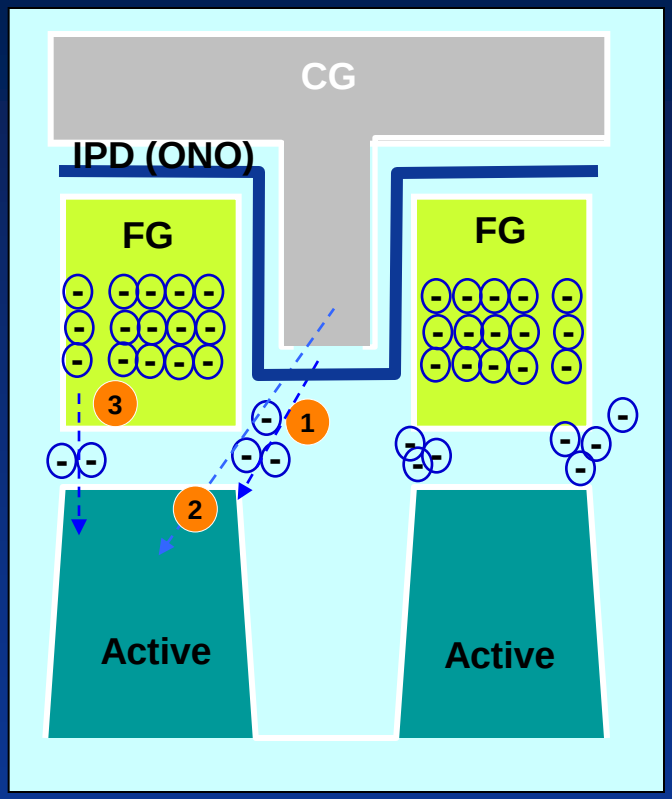
Cycling with detrapping ON

Retention after cycling without detrapping

Retention after cycling with detrapping



Detrapping Mechanism



- Applying the low level bias in Well

Removing shallow trapped charges in

- IPD trap Sites (1)
- Gap fill material (interface) (2)
- Interface between T_{ox} and Si (3)

Conclusions

- TLC (3 bits per cell) needs to be more optimized condition than MLC in PGM /Read/ Erase for improving the reliability
- In read operation, dynamic read, interface cancellation and negative W/L schemes are proposed to overcome the V_{th} distribution overlap
- In erase operation, Alternative Erase & Verify and erase pulse optimization are proposed to reduce the erase stress
- In program operation, data randomization, Independently controlled W/L bias and de-trapping schemes are proposed to improve the interference, different W/L characteristics and retention characteristics