

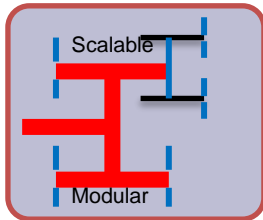


Engineering Challenges in Developing Large Flash Memory System

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Presented by
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Introduction



Case Study of System Design

- Scalable and Modular Design
- Image Storage and Processing System
- Flash Memory Based



Challenges

- 1X -> 1000X Data Handling Capability
- 1X-> 20X Runtime Data Write Capability



Solutions

- 2 Tier Master Slave Architecture
- System Cost to match System Throughput

System Specifications

Scalable Storage

- *Current Requirement 46 GB image to 460GB based on resolution*
- *Future requirement of 4 TB*

Search and Retrieve window 4 MB

- *Needle in a haystack !*

Scalable Flexible External Memory

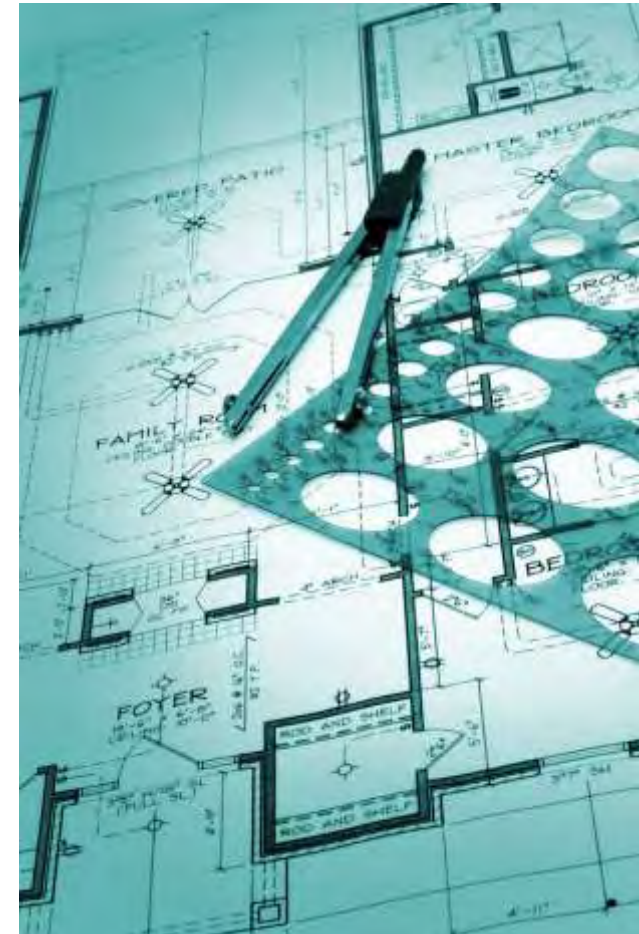
- *SD Card, Flash, ...*

Data Origination

- *Vanilla Off-the-shelf Desktop*

Base NRE Cost < \$25K

- *Cost can scale with throughput*



Design Challenges

Selection of Communication Protocols

- Based on throughput requirement
- Wide Range of Data
- Small search window

Design Architecture and Trade-offs

- Power Management
- Memory Management
- Cost Management
- Data Integrity wit Low Overhead



Communication Interfaces

Assumption

- Data Rates can be handled by FPGA/SD Cards

Throughput

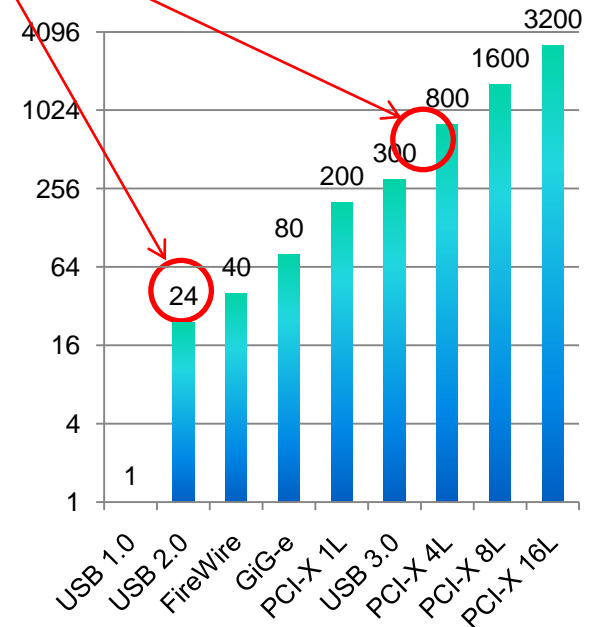
- PCI – X Supports simultaneous Read/Write

Ease of Use

- USB and GIG-E can be directly connected to output port of system
- Trade off Flexibility Vs. Speed

Target

Data Rate in MB/s



Design Trade-offs

Throughput and Cost Considerations

- Determines the number of memory controllers that must run in parallel
- Determines the tradeoff between Speed vs. Ease of Use
 - 25 MB/s for SD Card Vs. 100 MB/s for Nand Flash
 - GPIO – 100 Mb/s Vs. LVDS – 400 ~ 700 Mb/s Vs. SERDES – 2.5Gb/s

FPGA and Cost Considerations

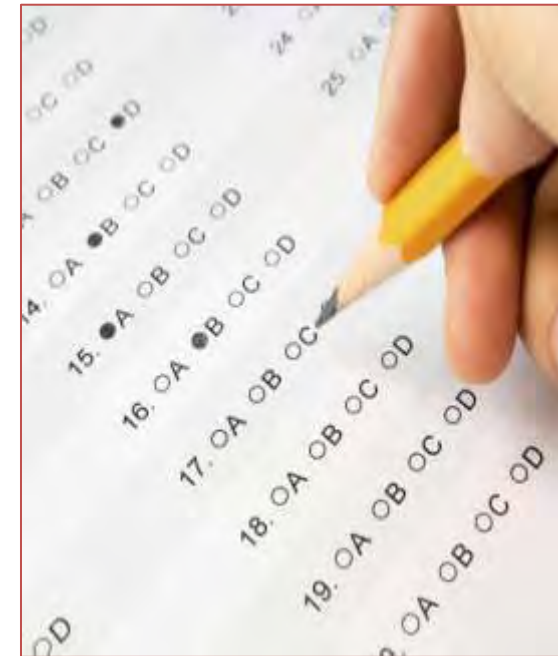
- How many such controllers can be packed into one FPGA
 - Capacity of FPGA
 - I/O Count of FPGA

Power Considerations

- Number of simultaneously operating controllers determines power budget

Tiered Architectures

- Flat Vs. 2 Tier Vs. N Tier determines FPGA selection, cost, scalability



Operational System

Overall Architecture

- 2 Tier Architecture
- 1 Base Memory Board + 4 Daughter Memory Cards
- Supports throughput scaling by parallel Memory Reads

Base Memory Board

- Designed with both USB and PCI-X on host-end
- 4 Matched Pair LVDS at Other End
- FPGA dedicated to Transfer Data from Host to Daughter Cards

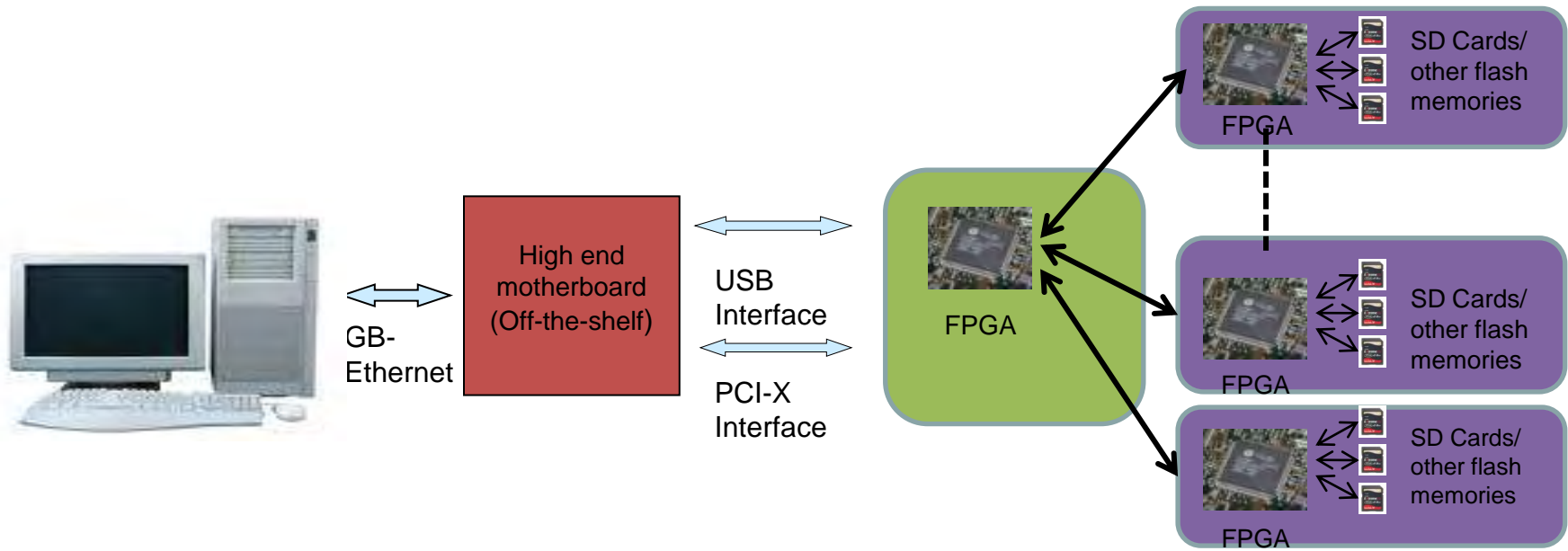
Memory Daughter Card

- Supports from 4 GB (96 x 4 MB) -> 4 TB (96 x 4 GB) Storage



Picture shows one Image Processing and storage modules consisting of one memory base board and one memory board (having multiple SD Cards)

System Architecture



Mother Board

- Gigabit Ethernet
- 12 GB RAM
- 5 USB ports
- USB and PCI -X

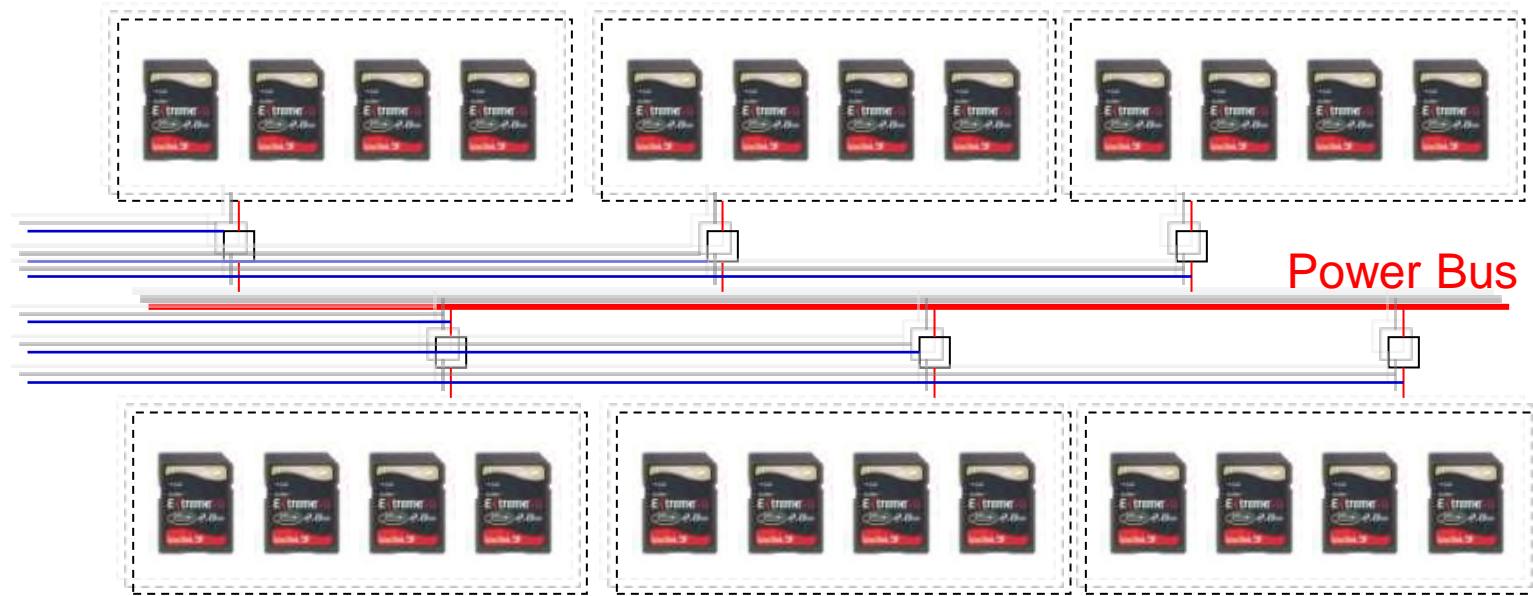
Base Memory Board

- FPGA
 - Spartan 3
 - 4 Memory Controllers
 - 40 LVDS Matched Pairs (100 MHz each)
 - 20 Tx / 20 Rx
 - Distributed Memory

Daughter Memory Cards

- 4 Cards
- Each Card
 - 24 slots
 - Arranged as 6 x 4
- SD Card or Flash
- 80% I/O Utilization

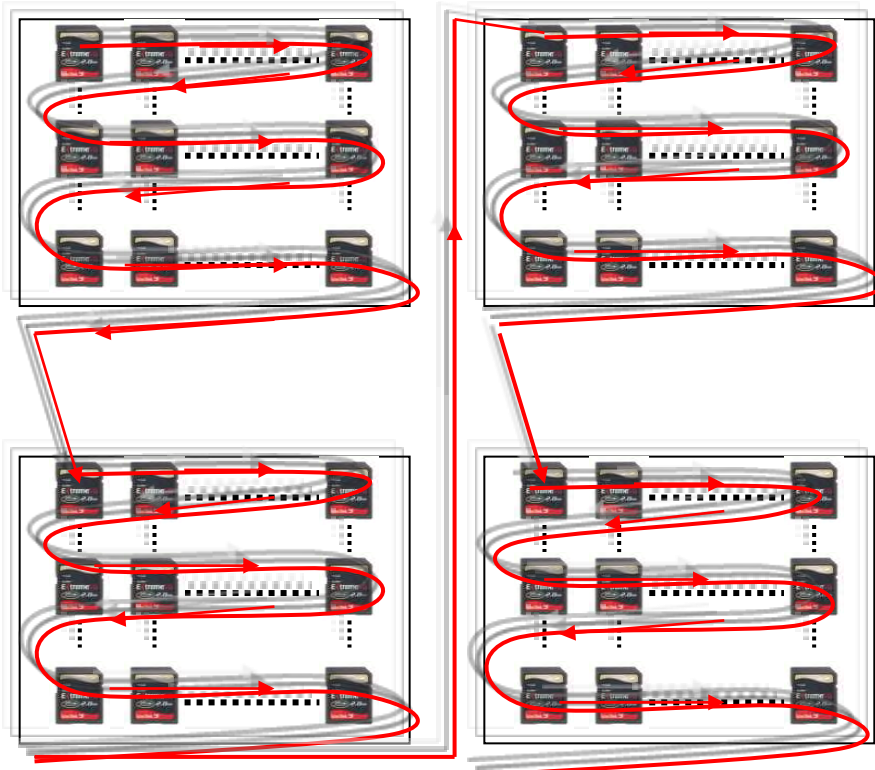
Power Management



SD Cards Arranged in banks of 4

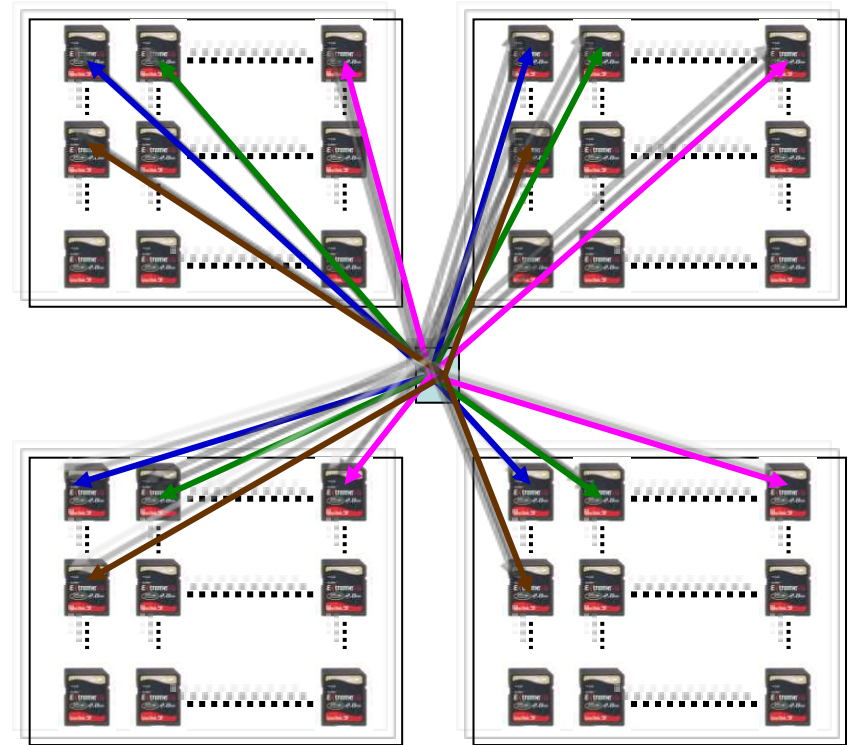
- Non operational banks turned off
- FPGA Controls the switch and turns on/off before read/write operations
- 5/6th (~80%) power savings

Memory Management



Sequential Storage and Access

- Retrieval is fast
- Throughput is slow



Distributed Storage and Access

- Throughput is fast
- Scales well

End-To-End Design

System Design

- Architecture
- Component Selection
- Manufacturing
- Communication Design
 - *USB, PCI-X, LVDS*
- O-T-S Board
- System Integration
 - *with host PC*

Hardware Design

- RTL Design
 - *FPGA Based*
- Multi-Board Partitions
- Verification
- Board Design
 - *Schematic*
 - *Layout*
 - *Signal Integrity*
 - *Test*

Software Design

- Firmware
 - *Inc. Driver development*
- Application Software
 - *Operator Control*
 - *Monitoring GUI*
- Porting
 - *Onto prototyped system*
- System testing

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*In collaboration with partners

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