

A close-up, angled view of a microchip die, showing its intricate circuitry and a central square area.

Between Fuses and Flash

An Overview of CMOS NVM in Consumer Applications

THE SEMICONDUCTOR INDUSTRY'S TRUSTED IP PARTNER



Virage Logic Blue
Pantone: 534
RGB: 40/70/115
CMYK: 100/80/30/5



Red
Pantone: 484
RGB: 180/35/25
CMYK: 0/95/100/29



Purple
Pantone: 2415
RGB: 165/25/130
CMYK: 35/100/0/10



Green
Pantone: 368
RGB: 123/190/67
CMYK: 7/5/5/5



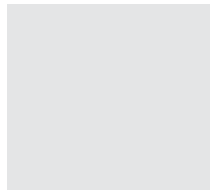
Orange
Pantone: 158
RGB: 245/128/37
CMYK: 0/61/97/0



Yellow
Pantone: 123
RGB: 255/196/37
CMYK: 0/25/95/0



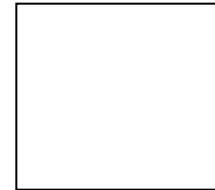
Teal
Pantone: 327
RGB: 0/145/145
CMYK: 100/0/45/15



Light Grey
Pantone: 427
RGB: 228/229/230
CMYK: 7/5/5/5



Medium Blue
Pantone: 286
RGB: 0/95/170
CMYK: 100/65/0/5



White
RGB: 255/255/255
CMYK: 0/0/0/0

Agenda

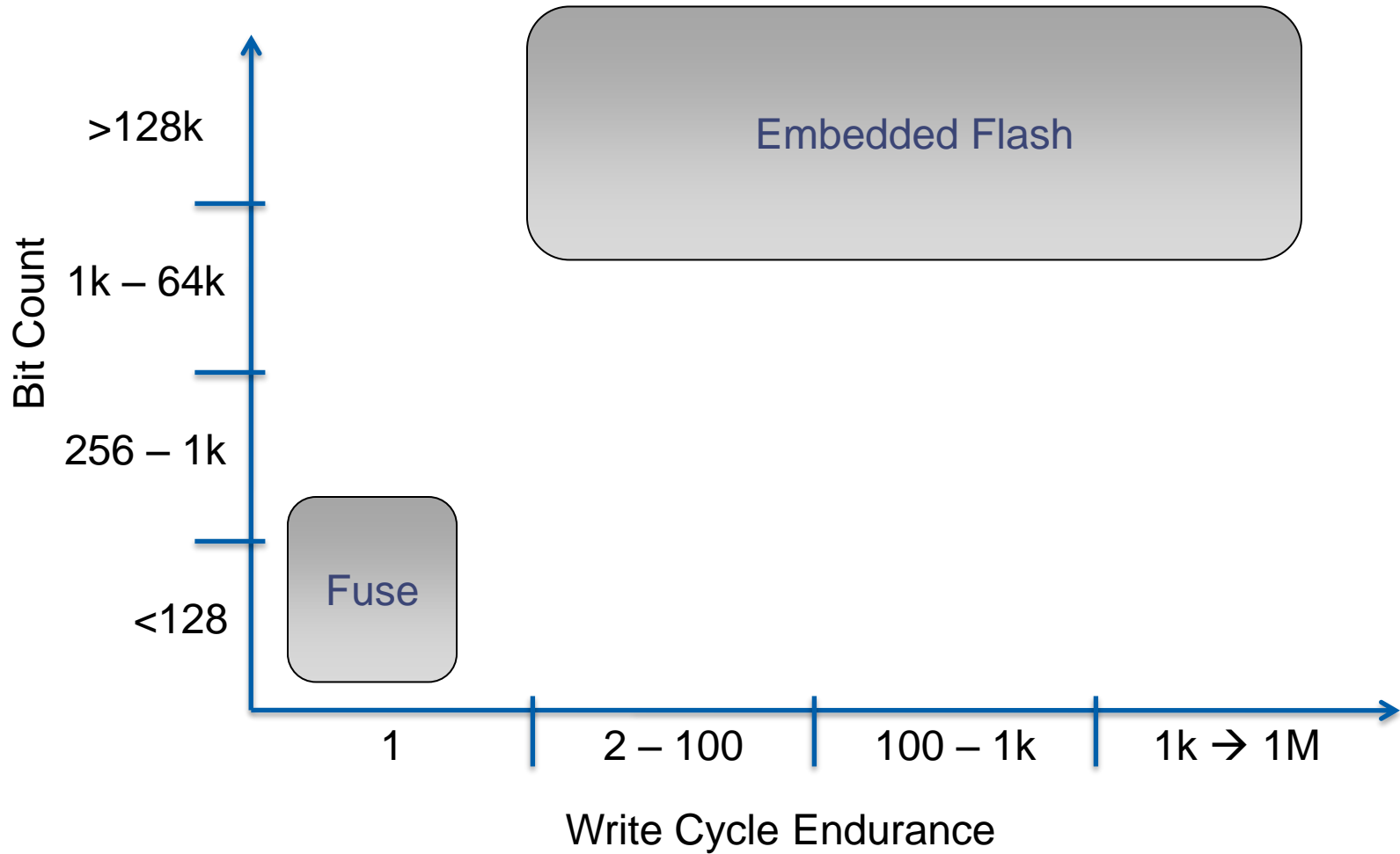
- Definition of CMOS NVM
- Market Landscape
- Technologies
- Applications
- Summary / Conclusions

What Is CMOS NVM?

- **CMOS NVM** = nonvolatile memory manufactured in a standard CMOS process
 - No additional masks or processing steps
- Includes several different technologies
 - **MTP** = **M**ultiple **T**ime **P**rogrammable
 - Up to 1M cycle endurance
 - **FTP** = **F**ew **T**ime **P**rogrammable
 - ~100 cycle endurance
 - **OTP** = **O**ne **T**ime **P**rogrammable
 - Either floating gate or antifuse based technologies

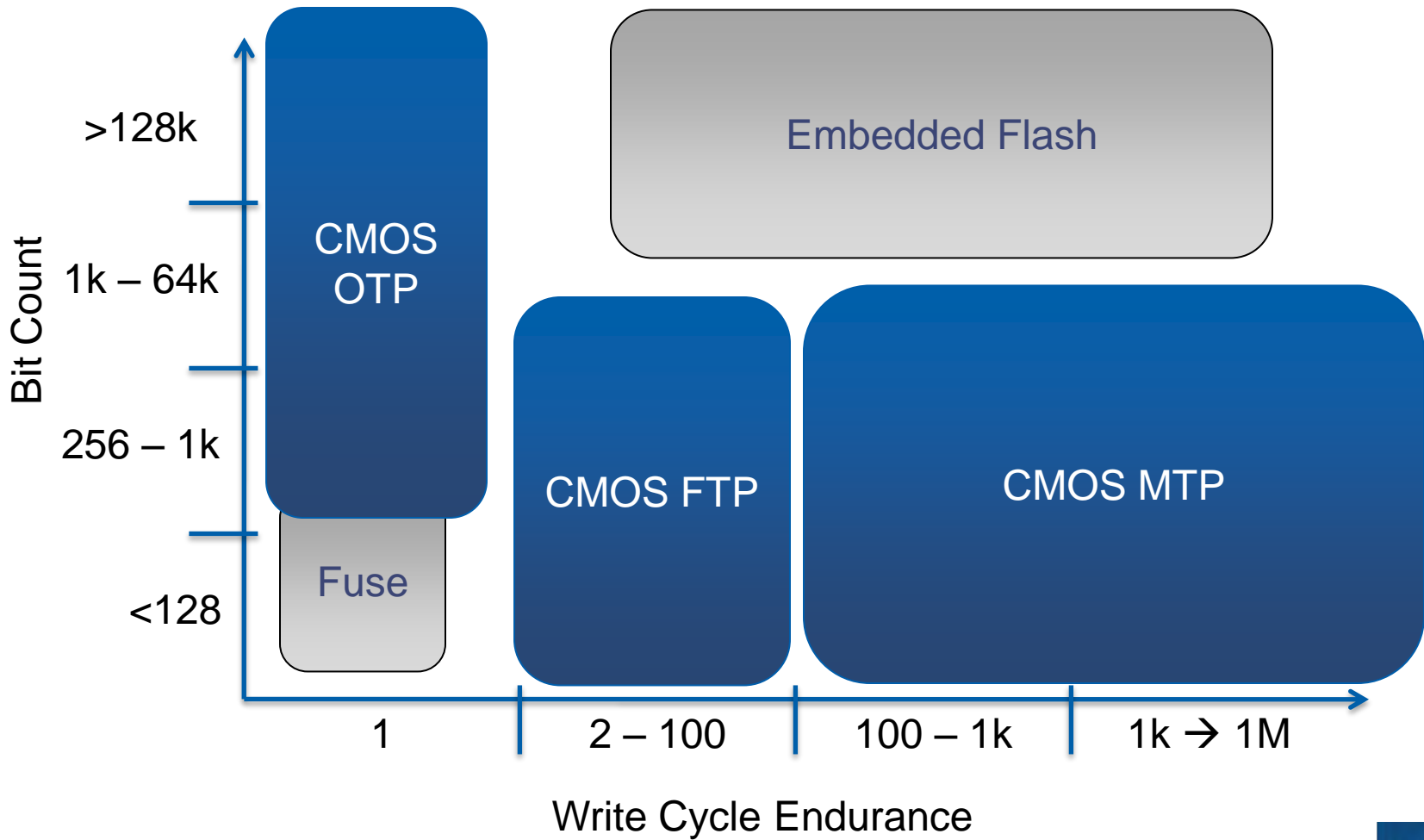
Embedded NVM Landscape

Traditional Fuses and Flash Leave Significant Applications Unserviced



Embedded NVM Landscape

CMOS NVM Fills the Gap



Embedded Flash Overview

Includes Other Mask Adder Solutions (SONOS, FRAM, MRAM, etc.)

Basic Technology

- Floating gate / charge storage
- Process / mask adders to standard CMOS process
- Available from foundries – technology from 3rd parties
- Available down to 90nm?

Advantages

- High endurance (20k → 100k write-erase cycles)
- High density (>1Mb)
- Production proven for high reliability applications (i.e. automotive)

Target Applications

- Microcontrollers
- Embedded code storage

Limitations

- Process cost / complexity
- 25% → 100% wafer adder
- Advanced process node support
- Long test times for large arrays (several seconds)

Fuse Overview

Includes Other Mask Adder Solutions (SONOS, FRAM, MRAM, etc.)

Basic Technology

- Overstress of poly, metal, oxide to create an open/short
- Developed and available from foundries
- Available down to 40nm

Advantages

- ~Free from the foundry
- Available early in process life – foundries develop fuse technology along with advanced nodes

Target Applications

- Trim
- Device ID

Limitations

- One time programmable only
- Limited bit count
- Long-term reliability concerns

OTP Overview

CMOS Based OTP Technology

Basic Technology

- Floating Gate – typically hot carrier injection
- Antifuse – overstress of gate oxide causing a short
- Available down to 55nm

Advantages

- High density (1Mb or more)
- Low cost CMOS process

Target Applications

- Code storage
- Encryption keys
- Trim / configuration data

Limitations

- One time programmable only
- Long test time for large arrays
- No electrical testing capability

MTP / FTP Overview

Reprogrammable NVM in Standard CMOS

Basic Technology

- Floating Gate – combination of FN-FN and hot carrier-FN
- Single poly standard CMOS process
- Supports up to ~16k bits
- Available down to 65nm

Advantages

- High endurance (MTP) up to 1M cycles
- Minimal area (FTP)
- High temperature (150C operation)
- Qualified to meet automotive standards

Target Applications

- Encryption keys
- Datalogging
- Trim / configuration settings
- Wireless / RFID

Limitations

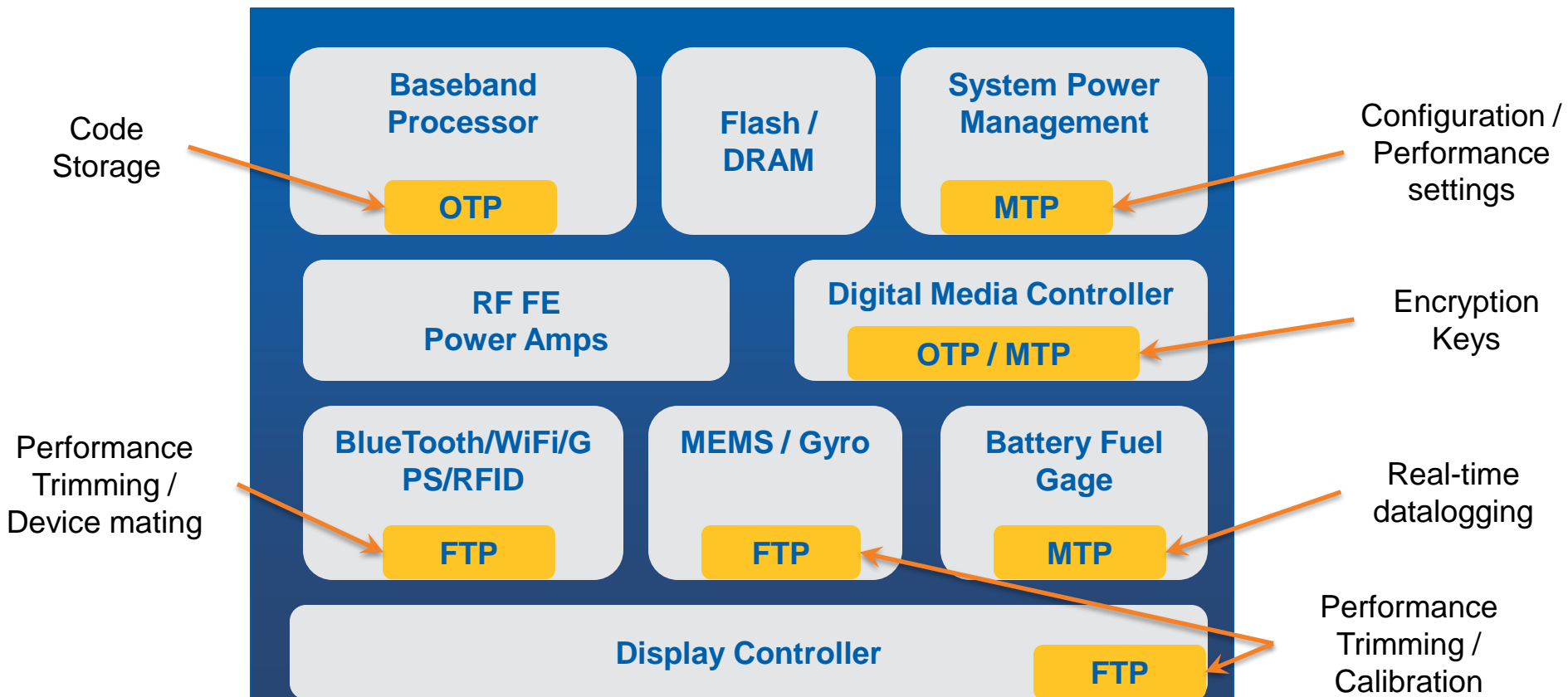
- Currently limited to ~16kbit
- Currently requires 50A gate oxide (solutions already in development)

A close-up photograph of a microchip die, showing its intricate circuitry and gold-colored surface, set against a blue background.

Key Applications

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CMOS NVM in Smartphones



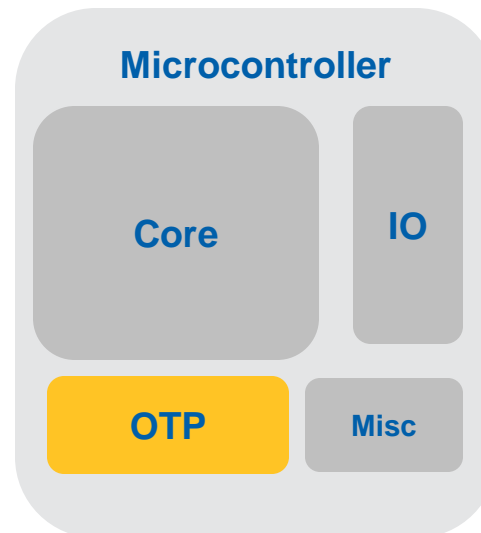
Code Storage Applications

Using OTP to Store Boot / Firmware Code

Attribute	Importance
Density	★★★★
Area	★★★
Flexibility (i.e. reprogrammability)	★★
Power	★

■ Competing Solutions

- Mask ROM
- Embedded Flash
- External NVM



■ CMOS NVM Advantages

- Post-fab programming (ROM)
- Advanced process node support (eFlash)
- Available at power-up (external)

■ End Products

- Consumer electronics
- Automotive
- Energy monitoring
- Medical

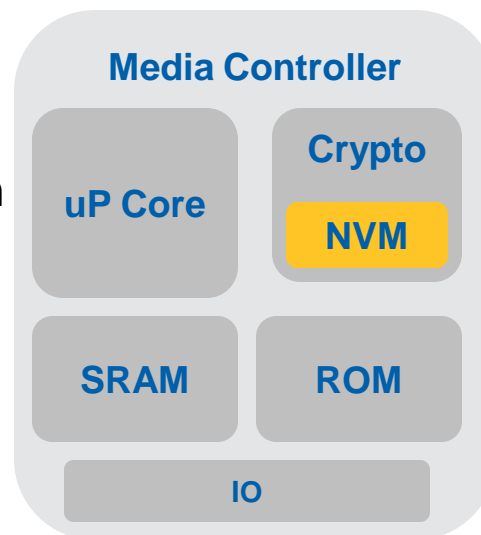
Storing Encryption Keys

OTP or MTP to Store AES, HDMI, etc. Keys

Attribute	Importance
Density	★
Area	★ ★ ★
Flexibility (i.e. reprogrammability)	★ ★ ★
Power	★ ★

■ Competing Solutions

- Software implementation (no NVM needed)
- External Storage



■ CMOS NVM Advantages

- Secure – both floating gate and antifuse
- Advanced process support
- Ability to tightly integrate with crypto engine
- MTP allows proactive / reactive key updates

■ End Products

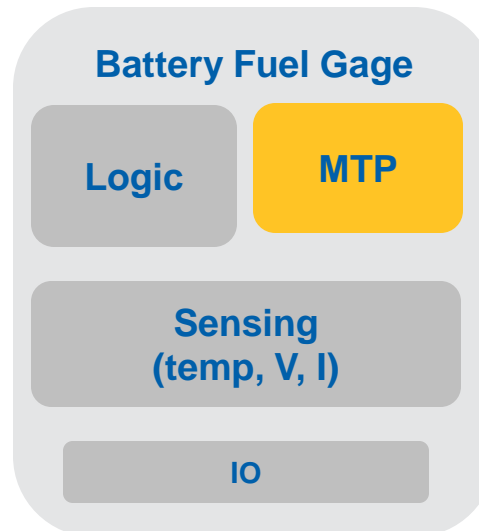
- HDMI Tx/Rx
- Digital media controllers
- Secure Flash Drives
- Encrypted HDD

Real-time Datalogging

OTP or MTP to Store AES, HDMI, etc. Keys

Attribute	Importance
Density	★ ★
Area	★ ★
Flexibility (i.e. reprogrammability)	★ ★ ★ ★
Power	★ ★ ★

- Competing Solutions
 - Embedded Flash



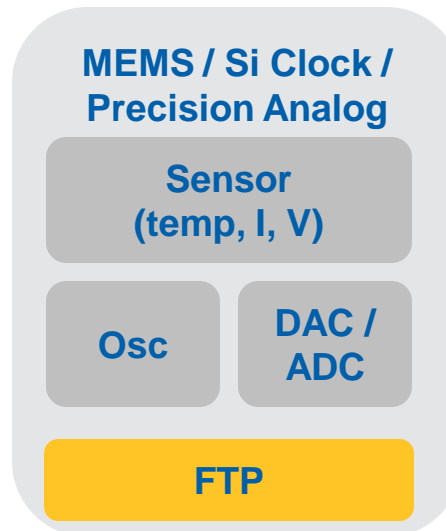
- CMOS NVM Advantages
 - Up to 1M cycle endurance
 - Support for BCD processes
 - High temperature operation (150C)
- End Products
 - Portable Devices
 - Notebook
 - Server / Telecom Power Management

Performance Trim

Overcoming the Limitations of Fuses

Attribute	Importance
Density	★
Area	★ ★ ★ ★
Flexibility (i.e. reprogrammability)	★ ★ ★
Power	★ ★ ★

- Competing Solutions
 - Fuses



- CMOS NVM Advantages
 - Reprogrammable up to 100 times
 - Allows post-package / in-field calibration
 - Fully integrated high voltage circuitry
- End Products
 - MEMS devices
 - Silicon clocks
 - Precision analog

Example FTP Specification

Targeted at MEMS, Si Clocks, Precision Analog

Parameter	Min	Typ	Max	Units
General				
Retention	10			Years
Endurance	100			Cycles
Temperature Range	-40	+25	+85	°C
Bit Counts	64		1k	bits
Program				
Input		16		Bits
Power Supply	1.55	1.8	2.0	V
Current		200	400	µA
Time		4	8	ms
Erase				
Input		16		Bits
Power Supply	1.55	1.8	2.0	V
Current		200	400	µA
Time		4	8	ms
Read				
Output		16		Bits
Power Supply	1.55	1.8	2.0	V
Current		100	200	µA/MHz
Time		50	120	ns

- Targets bit counts from 64 bits → 1k bits
- 100 write-erase cycle endurance
- Ideal for trim / OTP replacement applications

Embedded NVM Performance Summary

Technology	Process Node	Process Adders	Bit Counts	Endurance	Key Usage
Embedded Flash	180nm 90nm?	Yes	>1Mb	20k → 100k	Code storage
Fuses	→ 40nm	No	<1kb	1	Factory Trim
FG OTP	→ 110nm	No	<256kb	1	Trim / config Code storage
Antifuse OTP	→ 55nm	No	>1Mb	1	Code storage Keys
MTP	→ 65nm	No	<16kb	1M	Datalogging Keys
FTP	→ 65nm	No	<16kb	100	Precision trim Config

Conclusions

- Traditional embedded NVM technologies are not sufficient to cover the breadth of new applications and technologies today
- Emerging applications are driving high volumes and new requirements for embedded NVM
 - Firmware / Boot code for SoC
 - Encryption keys for securing data / media
 - Real-time datalogging
 - Precision trim for MEMS, analog
 - Wireless / RFID
- CMOS based NVM fills the gaps with a variety of enabling technologies
 - OTP → code storage
 - MTP → encryption keys, datalogging, RFID
 - FTP → precision trim, wireless
- Visit us at www.viragelogic.com for additional information on CMOS based NVM