Beyond ECC - Memory Signal Processing (MSP™)

Flash Memory Summit
August 19th, 2010

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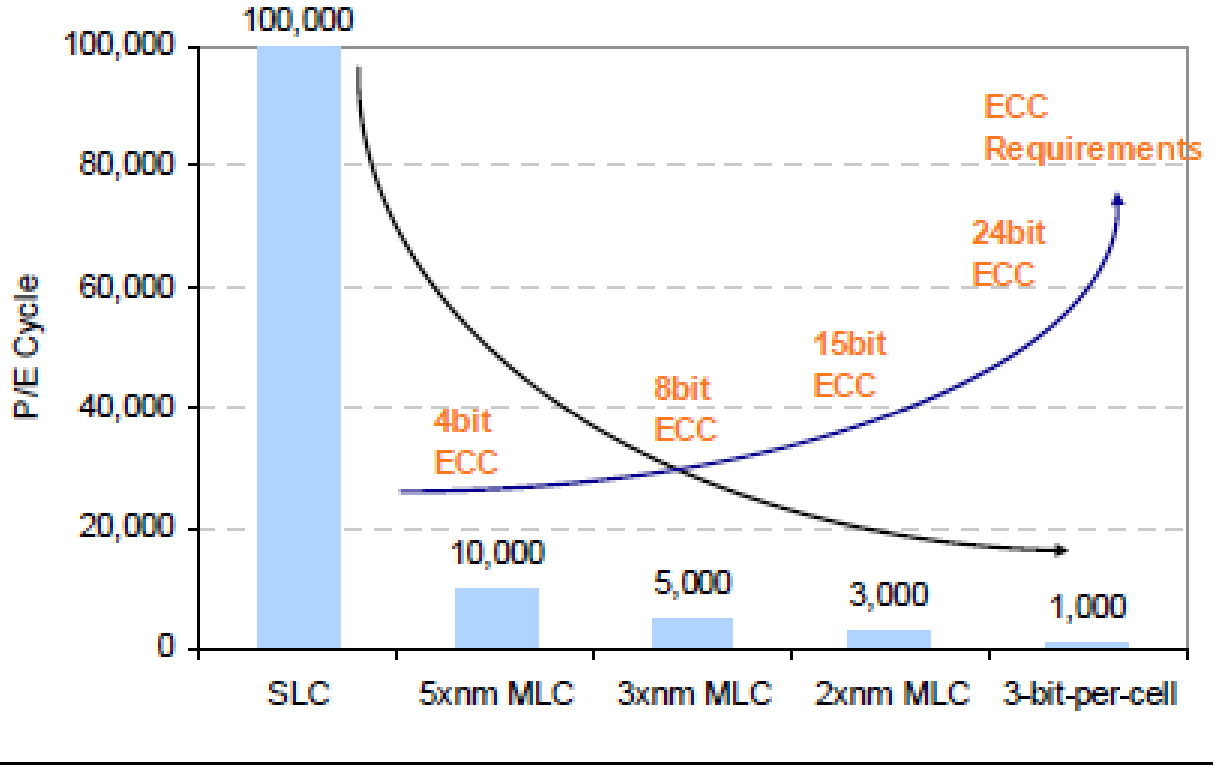
About Anobit

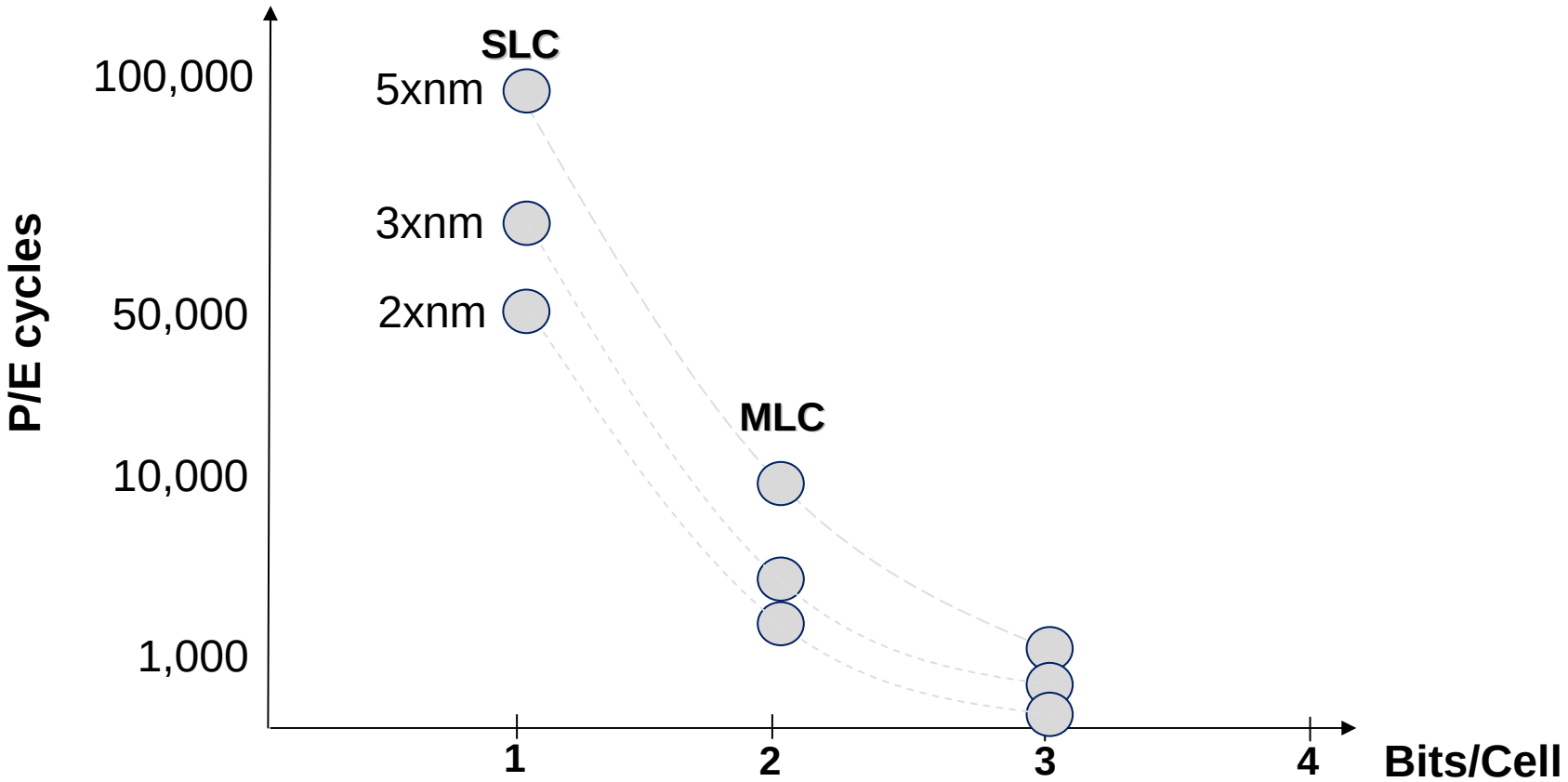
- Founded in 2006
- Based in Israel
- Subsidiaries in the US and Korea
- 130 Employees

NAND Flash Evolution



Source: Morgan Stanley Research

NAND Flash Evolution



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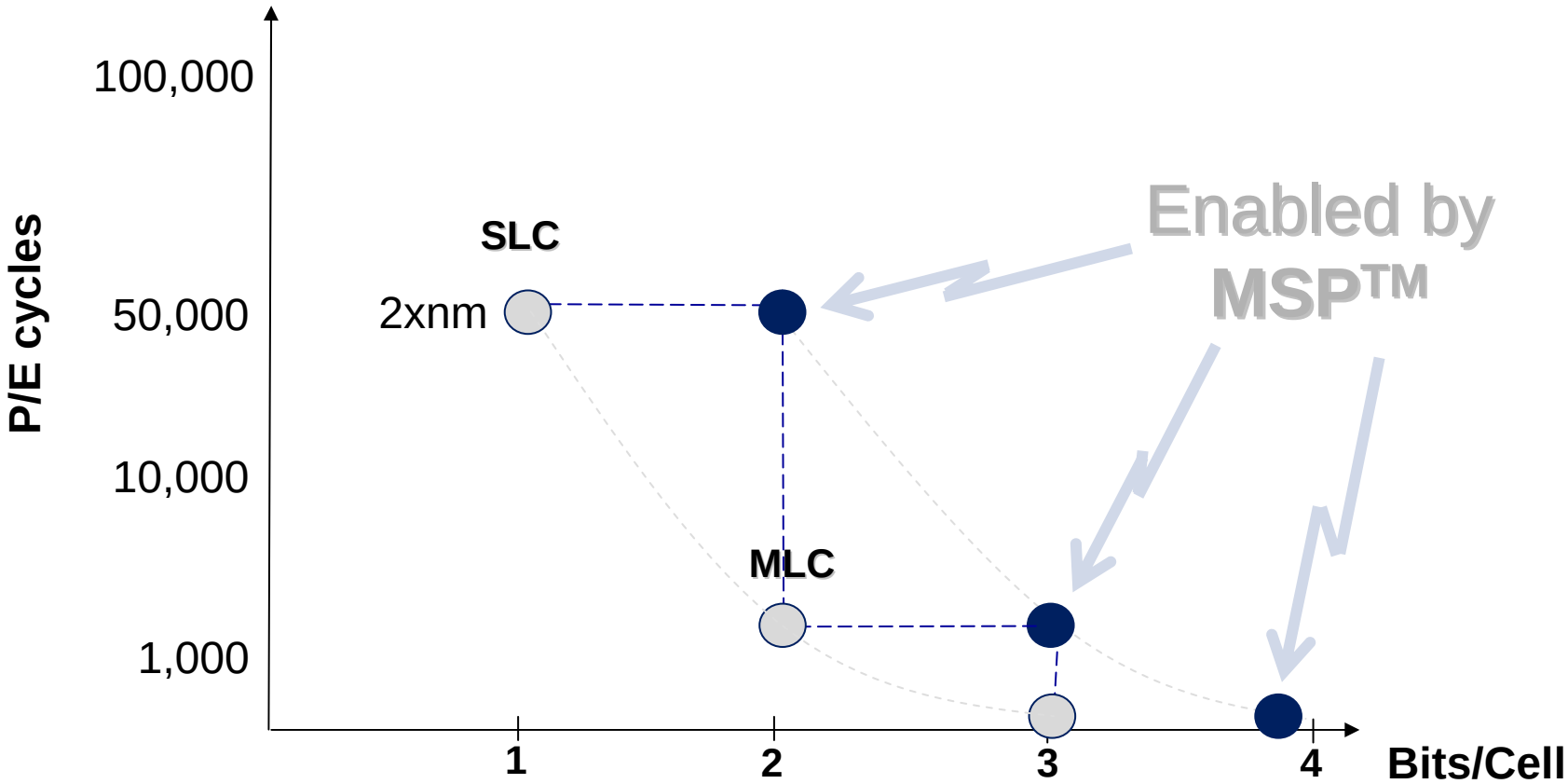
NAND Flash Evolution



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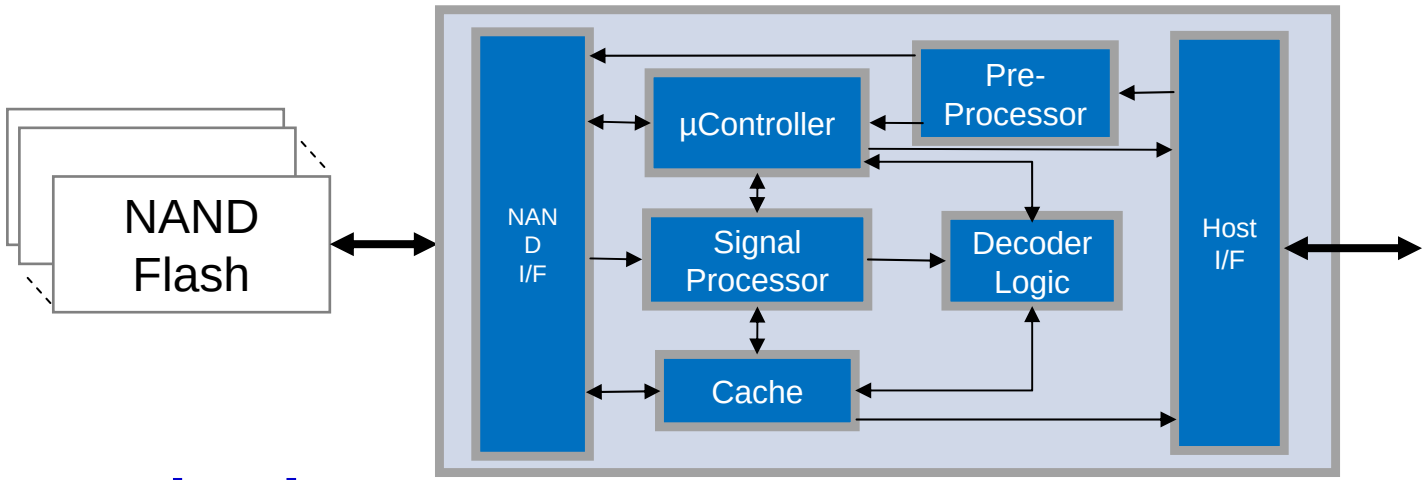
MSP™ – Memory Signal Processing

Over 60 patent applications



Error Reduction

- Compensates for process and array impairments
  Cross coupling, Read disturbs, Program disturbs, Data retention impairments, Endurance impairments

Error Correction

- Advanced ECC with improved error correction capabilities

Benchmarking:

MSP vs. 48b/1KB ECC

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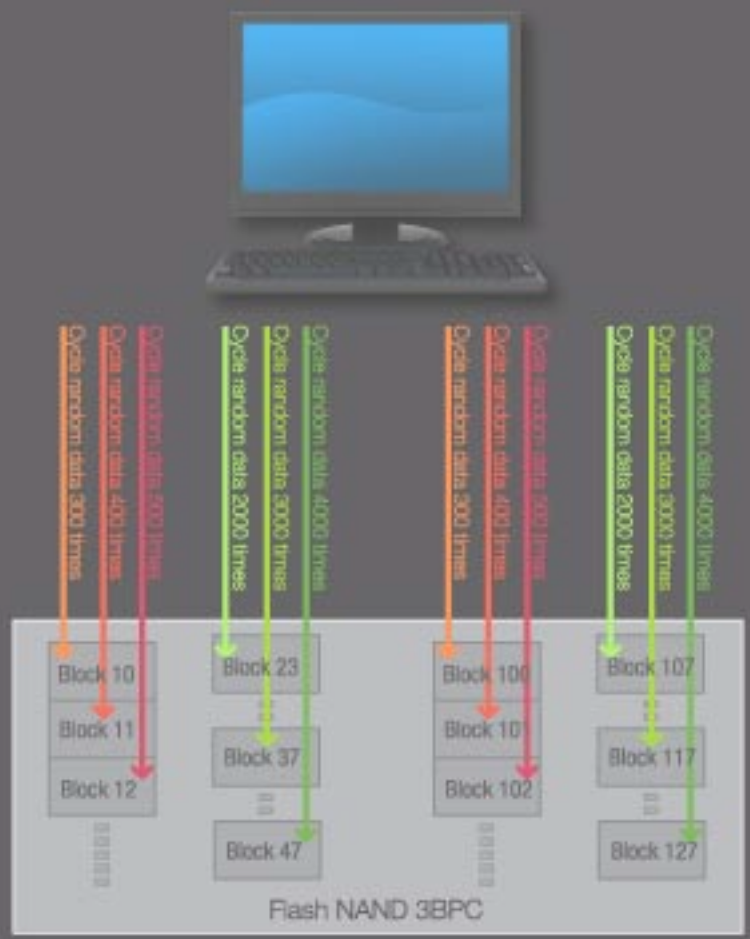
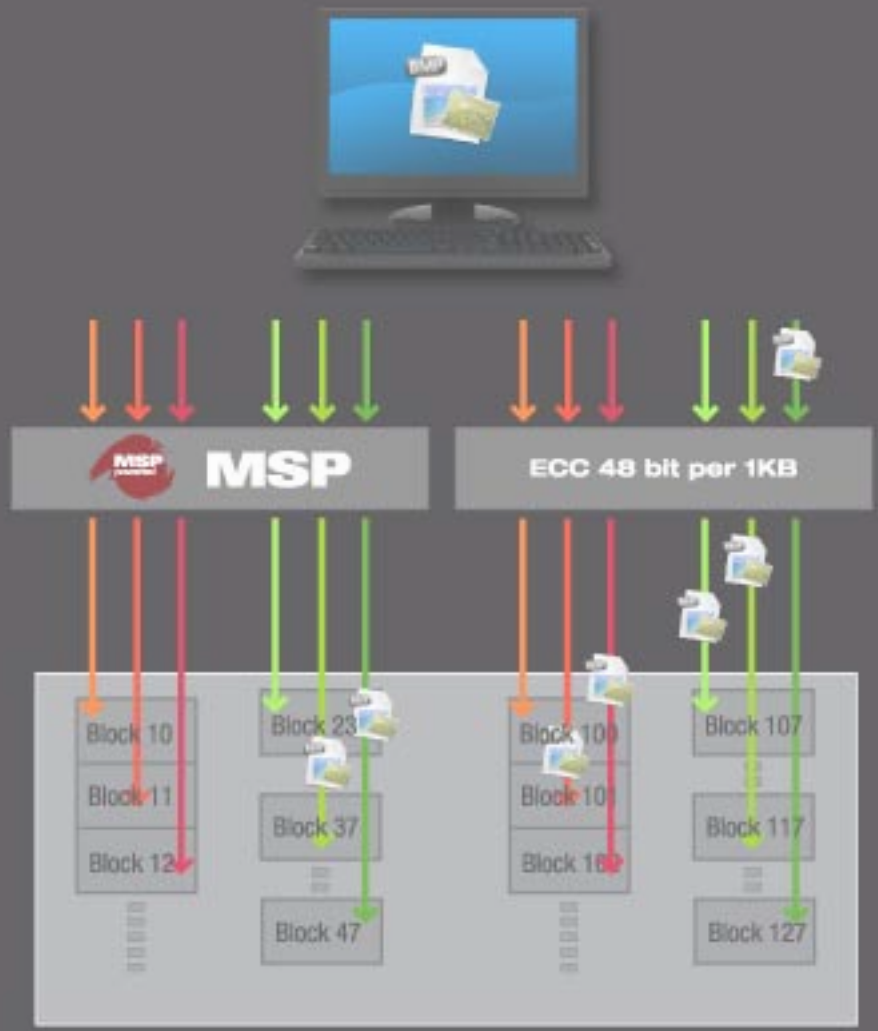
Cycling each block to unique P/E cycles

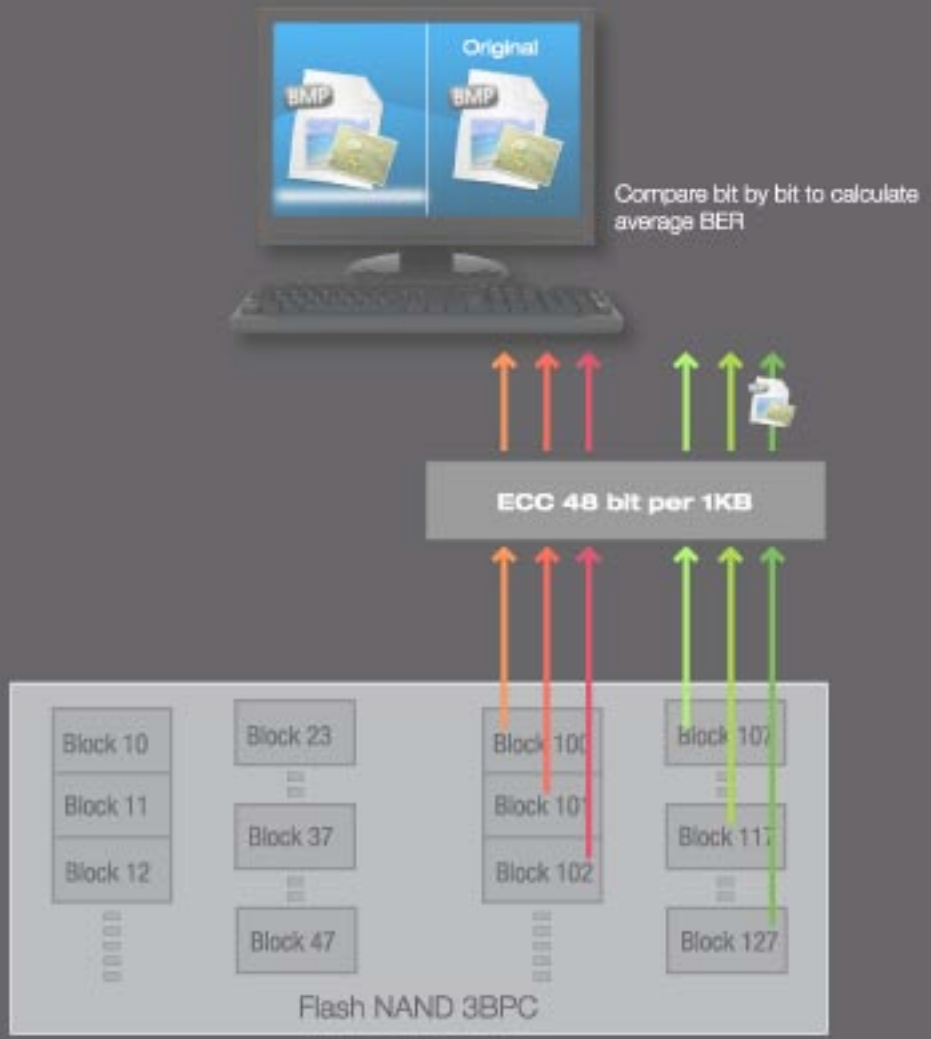


Program image to each block

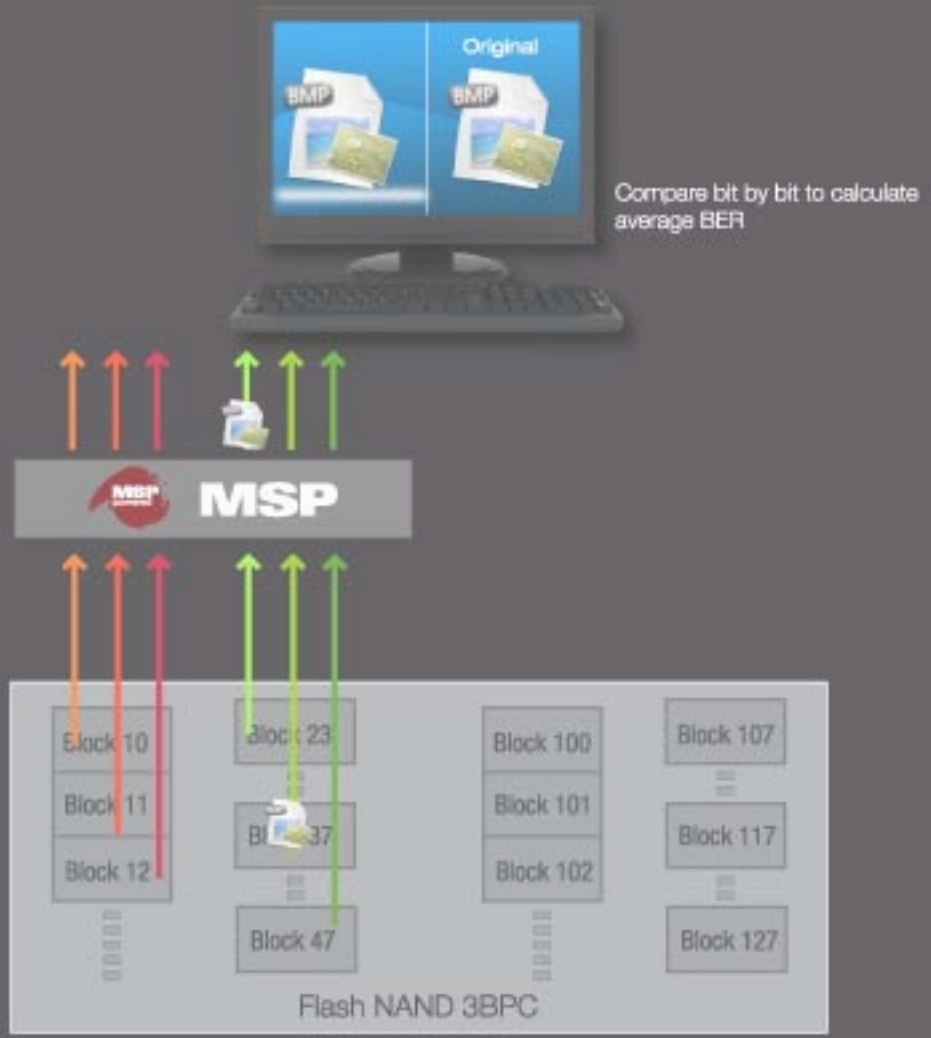


Baking to 1yr JEDEC procedure

Read with ECC

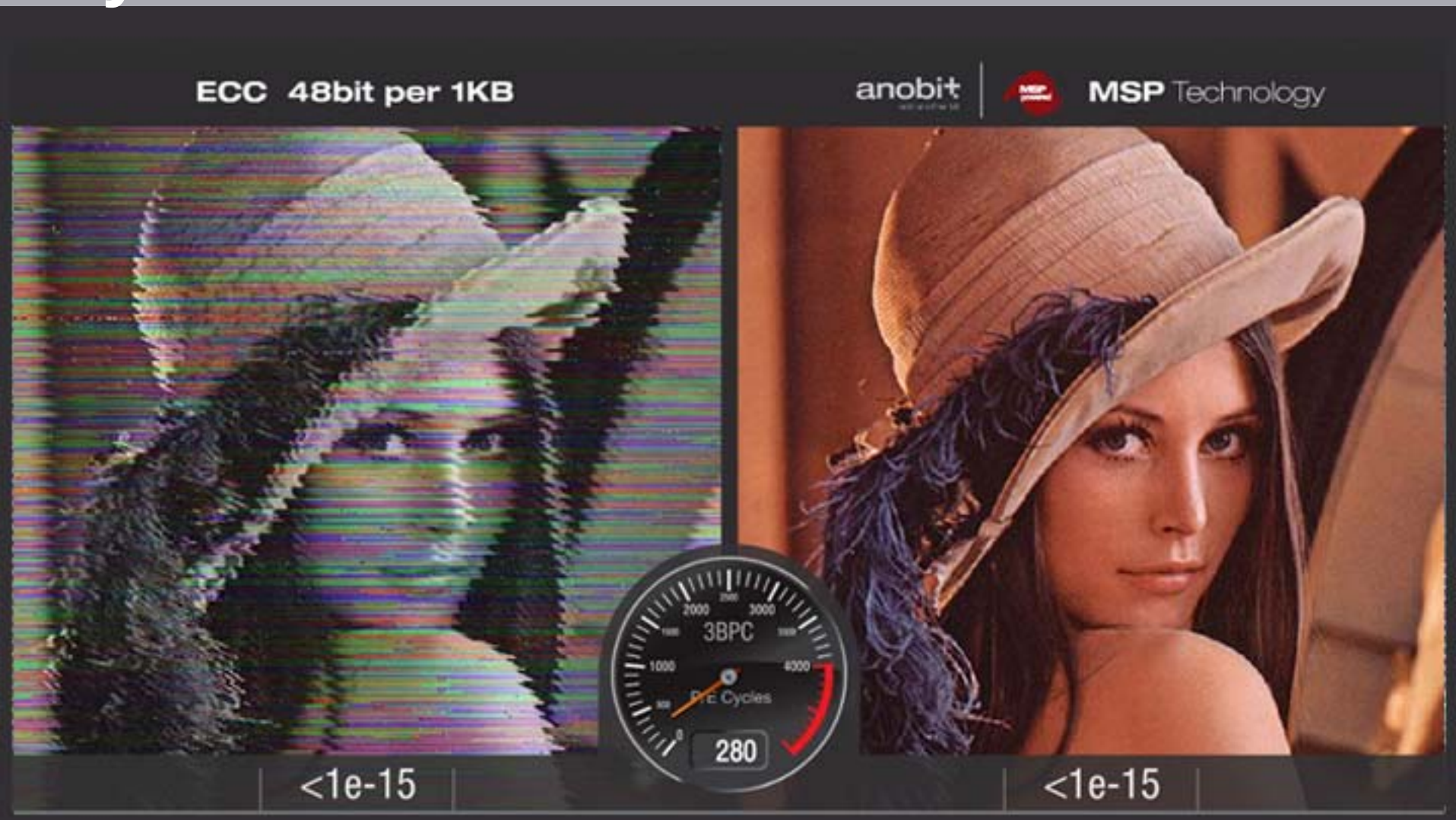


Read with MSP



Cycle 0

Cycle 280



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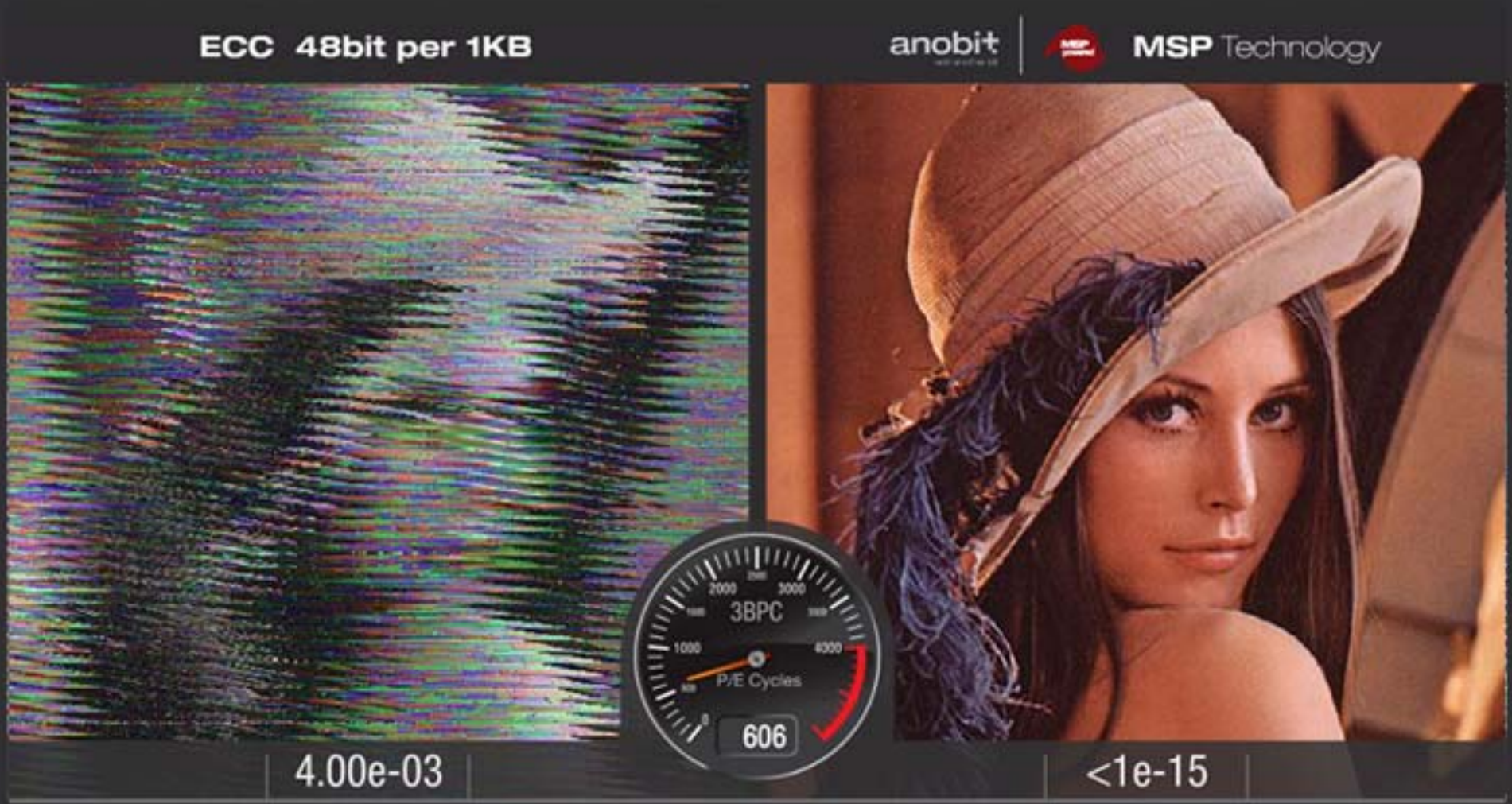
Cycle 660



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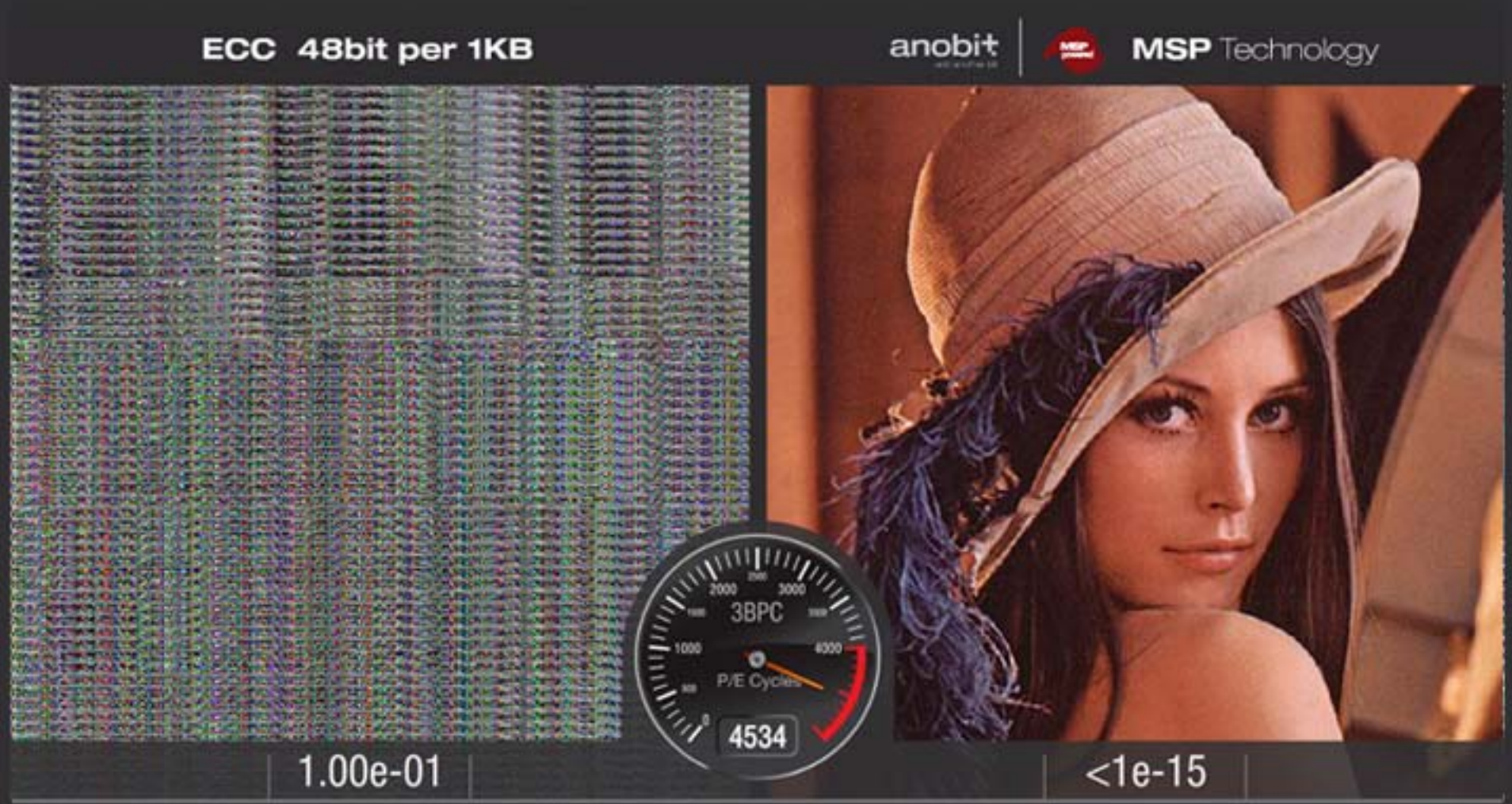
Cycle 4534



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Cycle 4544

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Genesis I enterprise SSD

- Drive Endurance:
  - 10X Drive Cycles / day; 356 days/year; 5 years
  - Fully random, non-compressible data
- Equivalent to 50K P/E NAND cycles

Thank you

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