Enabling New-Generation Flash Memories in SSD

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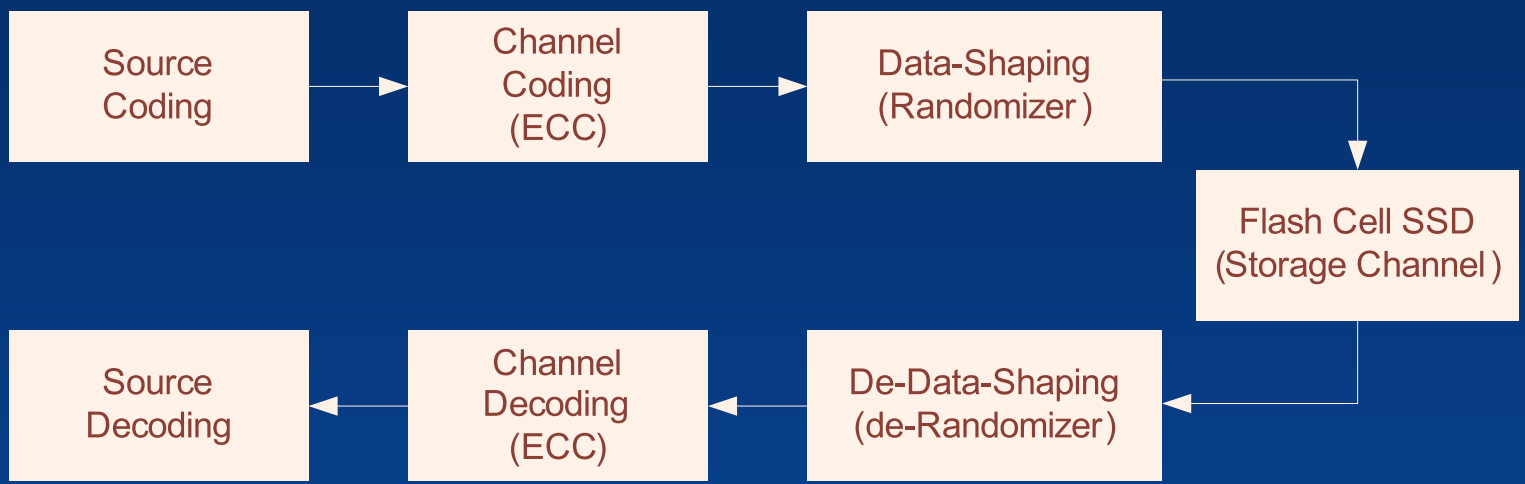
SSD Storage System



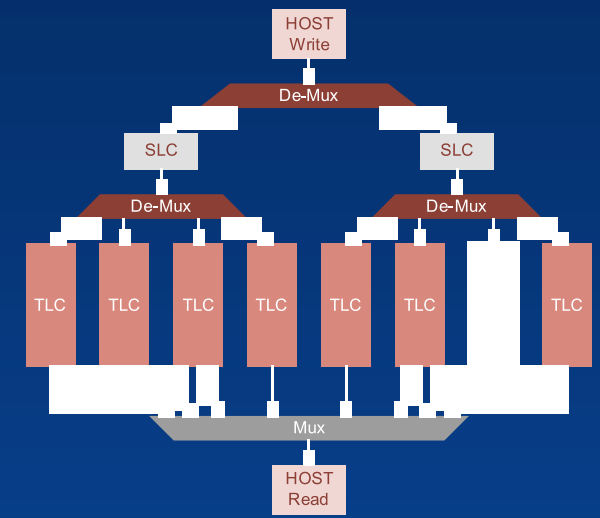
- While the channel becomes more noisy, the storage systems are still required to provide high data endurance.
- There is no retransmission scheme in storage system.
- As the flash process develops rapidly, the error rate goes higher than ever.
- The benefit from process shrinking will be mitigated by the increase of error rate

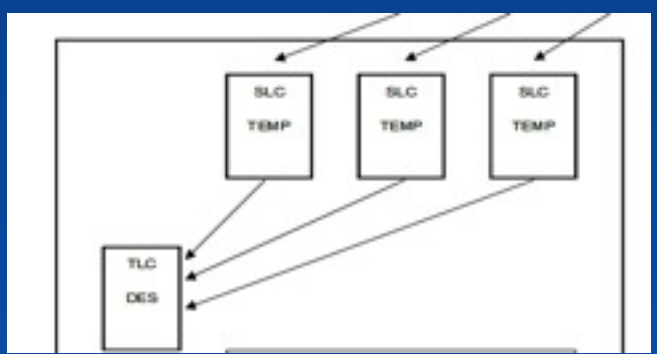
The Challenges of Flash Applications on SSD

- In TLC flash, the tProg (T-program) and tR (T-read) parameters need to set greater in order to reduce bit errors.
- Read/write disturbance and adjacent cell interference.
- The PV state drifts down and hence causes data retention issue.
- Vth distribution is broadening as P/E cycles increases.

Taking Advantage of LSB Natures First - Cache NAND

- The hybrid LSB (SLC) blocks and TLC blocks within one flash can solve the tProg issue.
- Data are written into LSB blocks and background moved to TLC blocks without error correction.
- Data are read out from TLC blocks.

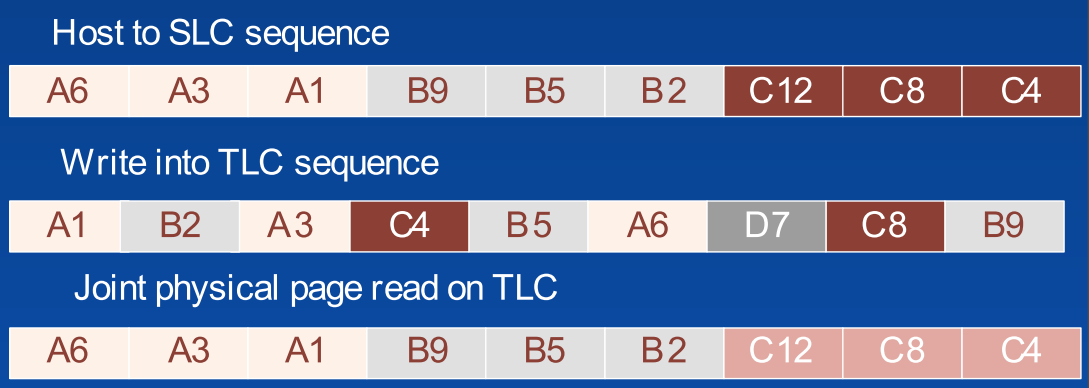




Cache NAND

- The Cache-NAND may be regarded as a buffer.
- Joint Page Read can reduce the tR value.
- However, Joint Page Write is not available to be used for TLC.
- When the data is background moved from SLC to TLC, Joint Page Read will be achieved.

Page -type	LSB	CSB	MSB
page 0	1	3	6
page 1	2	5	9
page 2	4	8	12
page 3	7	11	15



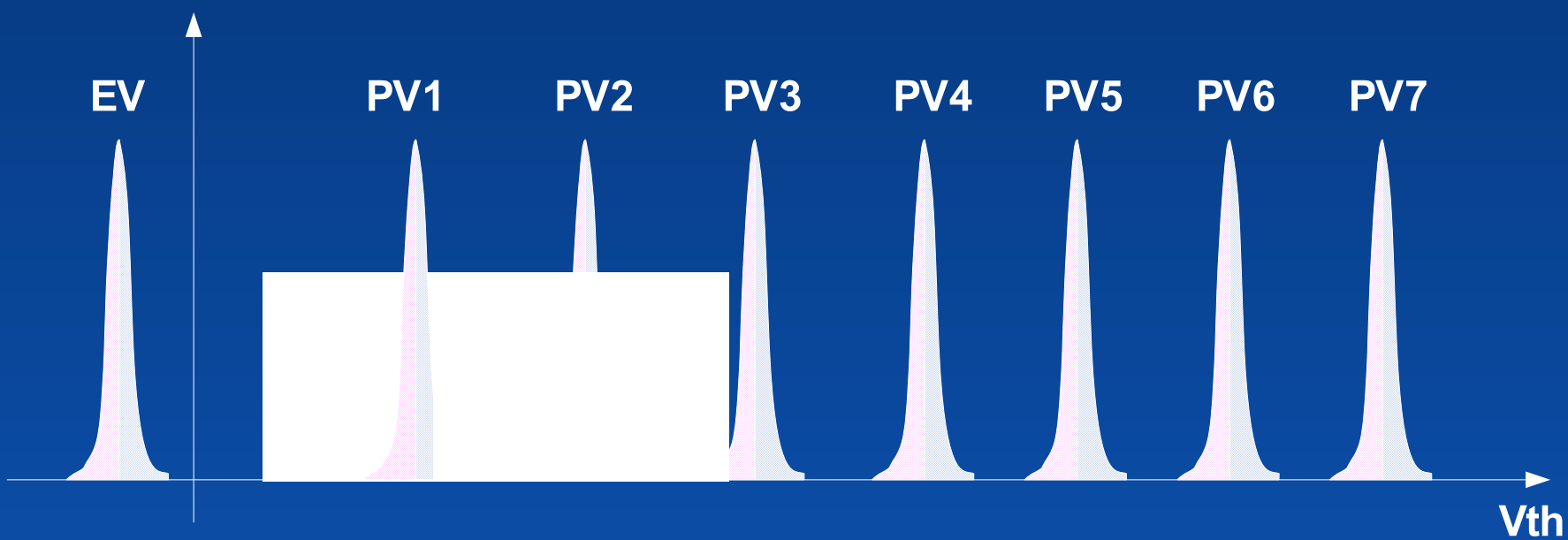
What Cache NAND Brings

- Reliability
  - Take advantage of natures of LSB (SLC)
  - Re-program becomes feasible if program (to TLC) failed
- Performance
  - Good random performance
  - Internal copy operation becomes feasible
  - Multiple page operation makes difference

But, we need more techniques to overcome TLC weaknesses!

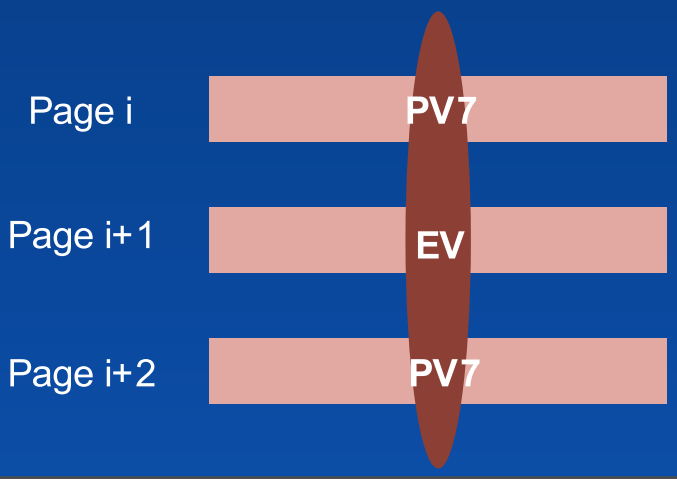
More Precisely Program (Write)

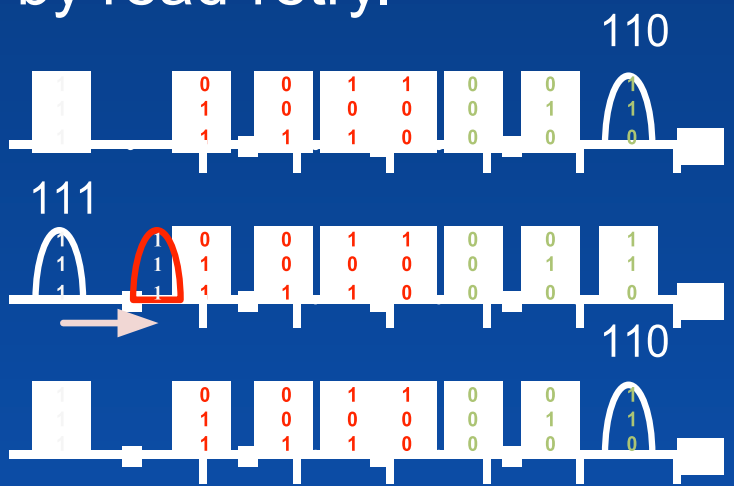
- A very centralized distribution is necessary for each PV state.
- The tProg and tR values will be large in order to reduce the error probability.



Noise Cancellation in Sequential Read (Adjacent Cell Interference)

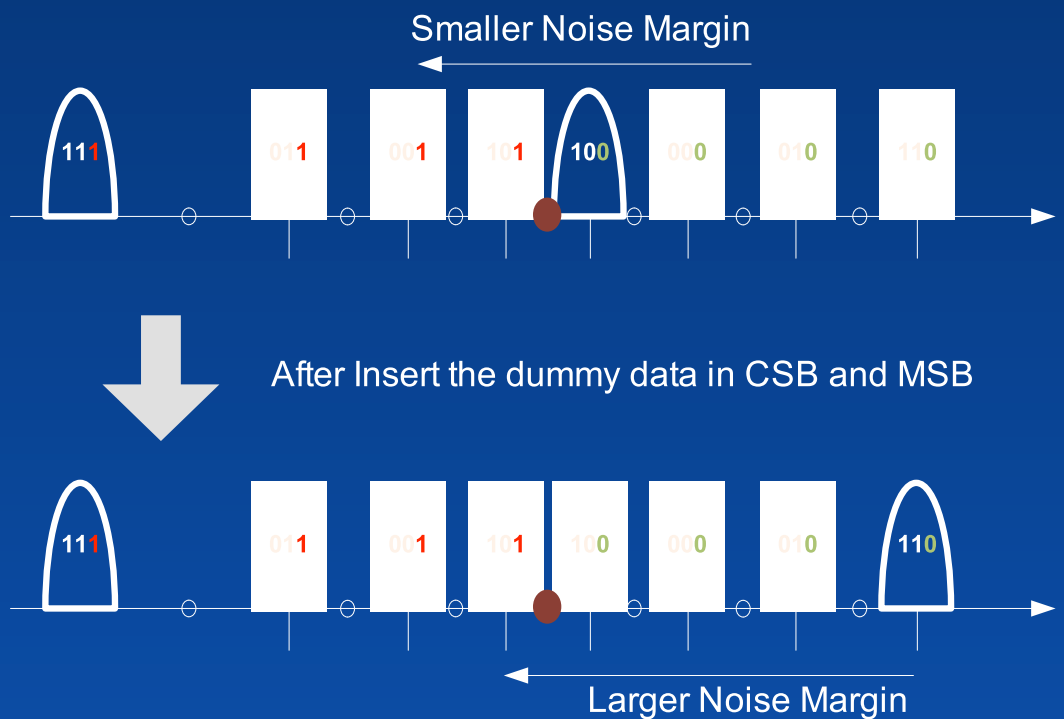
- After the data-CW write order is changed, the adjacent physical page will be read out in sequence.
- If an EV state appears between two PV7 states, the EV state may turn into to PV1.
- Weak PV1 can be forced to change to EV state, and then the ECC needs to be checked.
- Weak PV1 can be identified by read-retry.





Increasing Noise Margin

- Some important data (such as link-list table) will be written in LSB only, and dummy CSB and MSB will be written to enhance the data reliability.

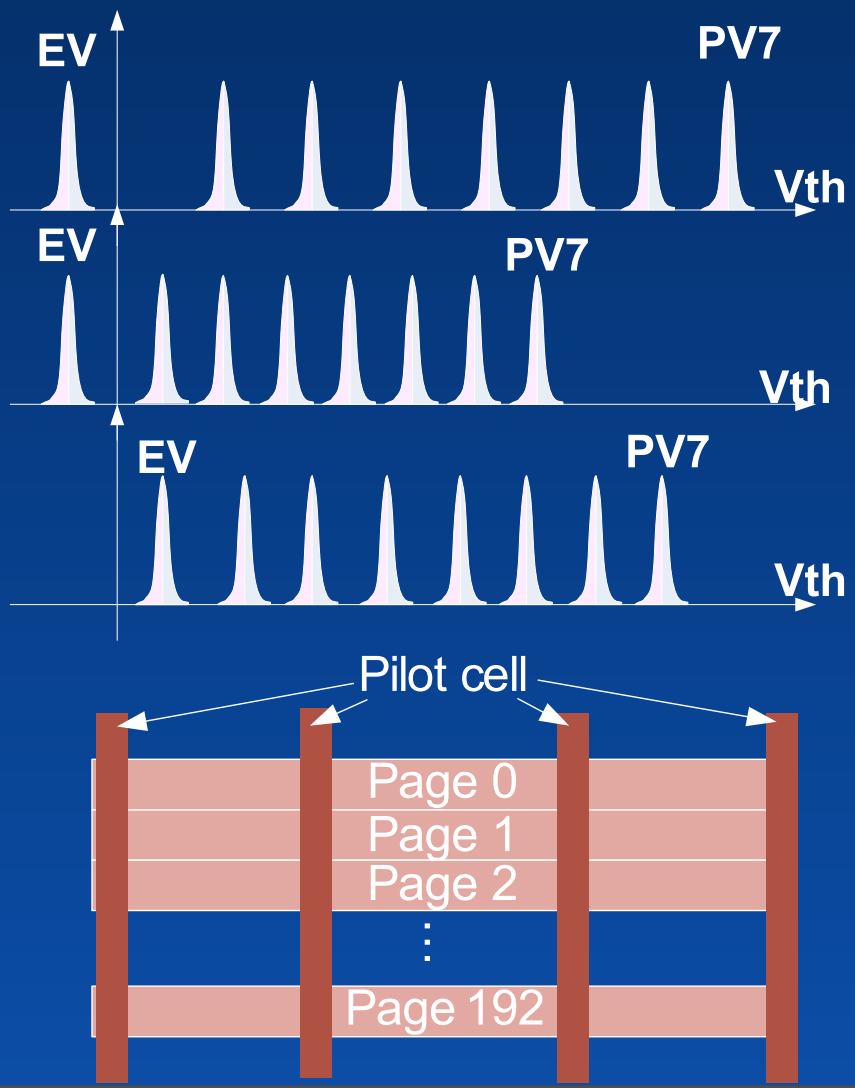


Static Refresh and Early Retirement

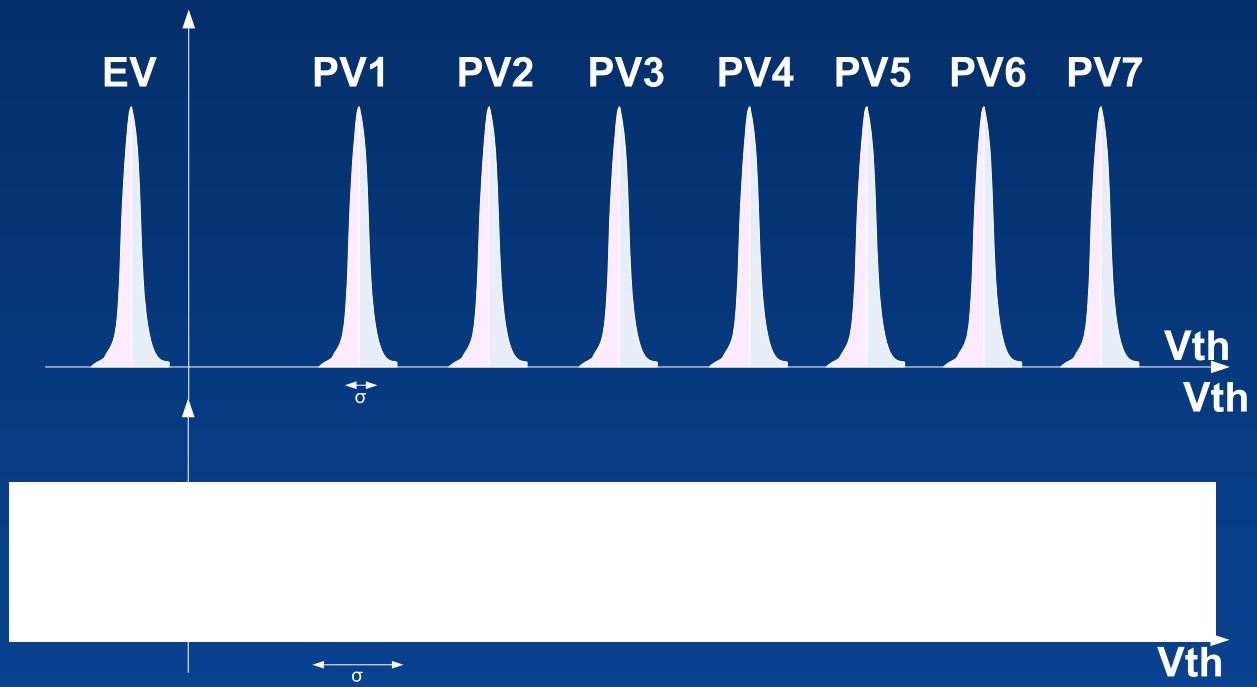
- In everyday use, more than 60% are repeated read operations, and the accumulated charge loss would eventually result in data loss.
- The refresh of the reference cells, ‘StaticDataRefresh’, is achieved by erasing and re-programming the data into the same cell or into another cell when the correctable error number is lager than a predefined level.
- This implementation practically restores the data to its original, error-free state, and hence, lengthening the life of the data .
- As a block ages over time, it cannot reliably store charge anymore, EarlyRetirement enters the scene.

Vth Tracking

- Under different ambient conditions (temperature, humidity, access count, … etc), the Vth may drift in different levels or directions.
- Insert some PV7 in each page at pre-determined locations to track the Vth drift.



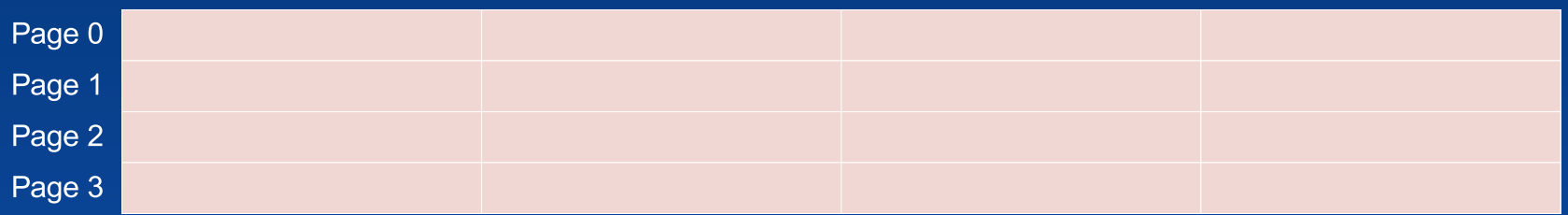
Voltage Distribution Broadening



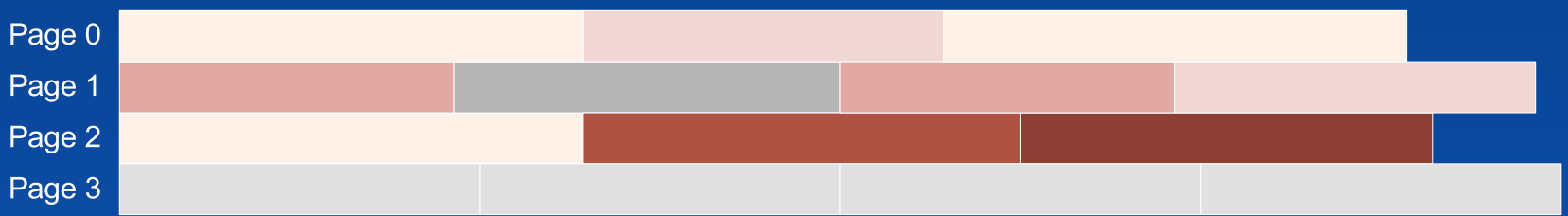
- The noise variance becomes larger, the original ECC with hard decoding method may not work, or needs larger parity to provide stronger protection.
- Several soft-decoding methods should be considered.

Rate Compatible Scheme in Storage System

- If the operation system is able to generate an indicator for the storage device, different protection strengths can be used to enhance system reliability depending on the data importance.
- Drawback 1: More system overhead.
- Drawback 2: Alignment issue.



The same protection strength for the same sector length.



The different protection strengths for the different sector lengths.

Data-Sector Accesses in SSD

- Without considering the disk-compression function on the OS system, the accesses of data-sectors can be classified into two types:
  - Without source coding (uncompressed):
    - OS minimum resident working set, web-browser, TextEdit, CAD tool access data-sector.
  - With source coding (compressed):
    - JPEG, MPEG, H2.64, MP3, … etc.
- Important data related to the system reliability will not be compressed.
- If uncorrectable errors occur in the compressed data, some noise suppression methods can be employed for data reconstruction.

Data-Shaping

- The uncompressed data blocks have very unbalanced distributions of 0 and 1.
- In new generation MLC and TLC flash, the unbalanced distribution damages the data stored in flash cells.
- Data-shaping is necessary to be used to scramble the original data.
- After applying data-shaping to a sector, this sector cannot be compressed any more.

Example: Operation System DLL File

```
00 0C 12 0E B8 00 12 59 B3 00 0C 12 34 19 0C B6
00 30 4E B2 00 0C C6 00 09 B2 00 0C A7 00 0C 12
0E B8 00 12 59 B3 00 0C 12 34 19 0D B6 00 30 3A
04 B2 00 0C C6 00 09 B2 00 0C A7 00 0C 12 0E B8
```

Original data: **0**➔49, **1**➔9, **2**➔11, ……, **E**➔4, **F**➔0

Very unbalanced distribution

```
46 E1 D5 3E 08 19 97 A7 C4 B8 30 4E 00 3F 96 9E
65 F6 9E C0 FB 6E 6D 66 C3 50 74 8D B3 5C BC B6
37 EB 23 FD 0F E0 37 78 A4 F1 DC 1E 5E 8F 88 26
F8 C1 3F 2B 23 B8 B1 3E A5 A3 5C B2 E7 40 32 C3
```

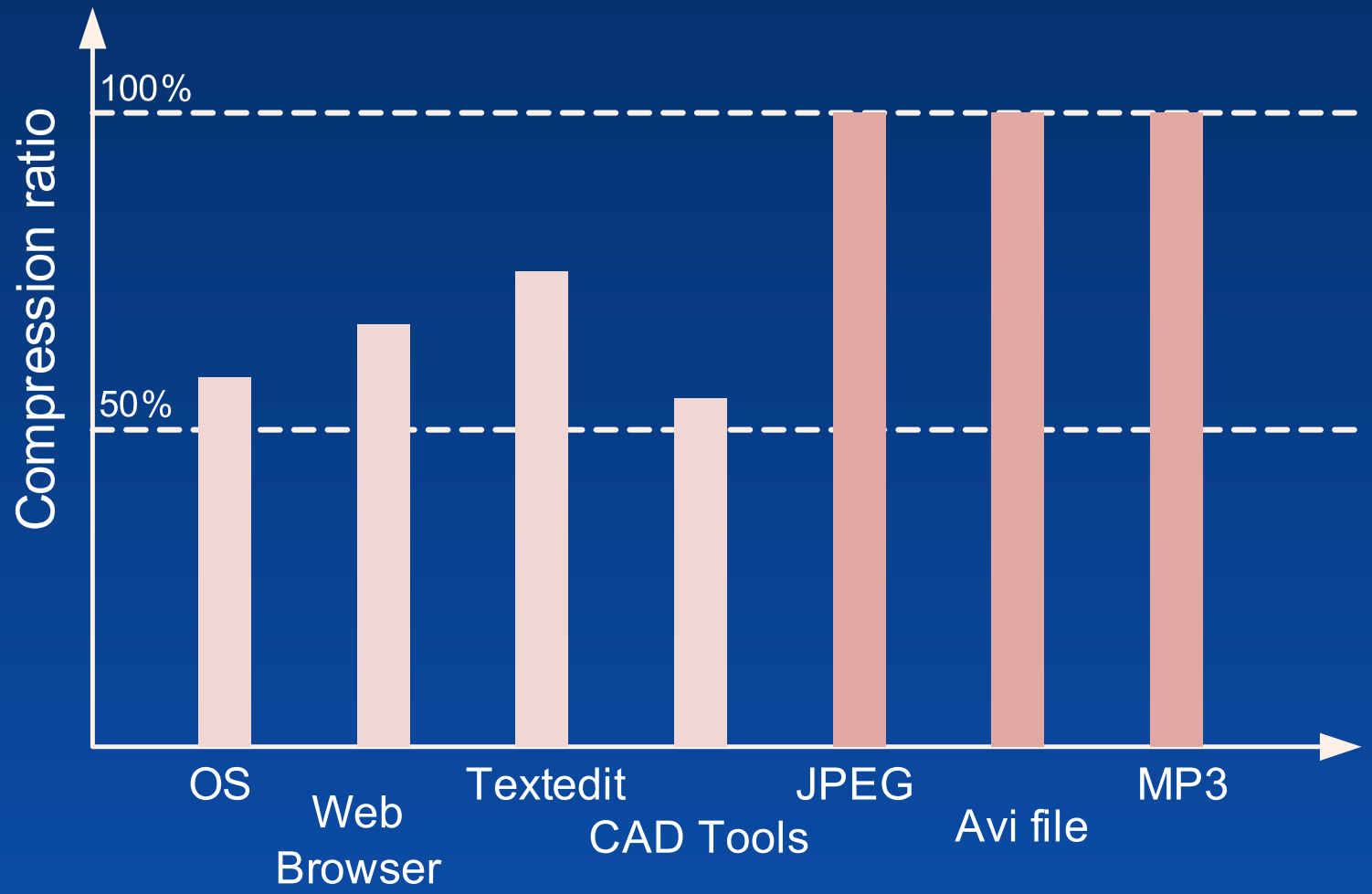
After data-shaping: **0**➔9, **1**➔6, **2**➔6, ……, **E**➔11, **F**➔8

```
24 D7 39 67 E9 CC 00 FA 16 42 E8 59 7B 69 45 75
D4 AD C3 36 F2 8C FD 22 82 3E 98 03 2F 16 C4 9C
```

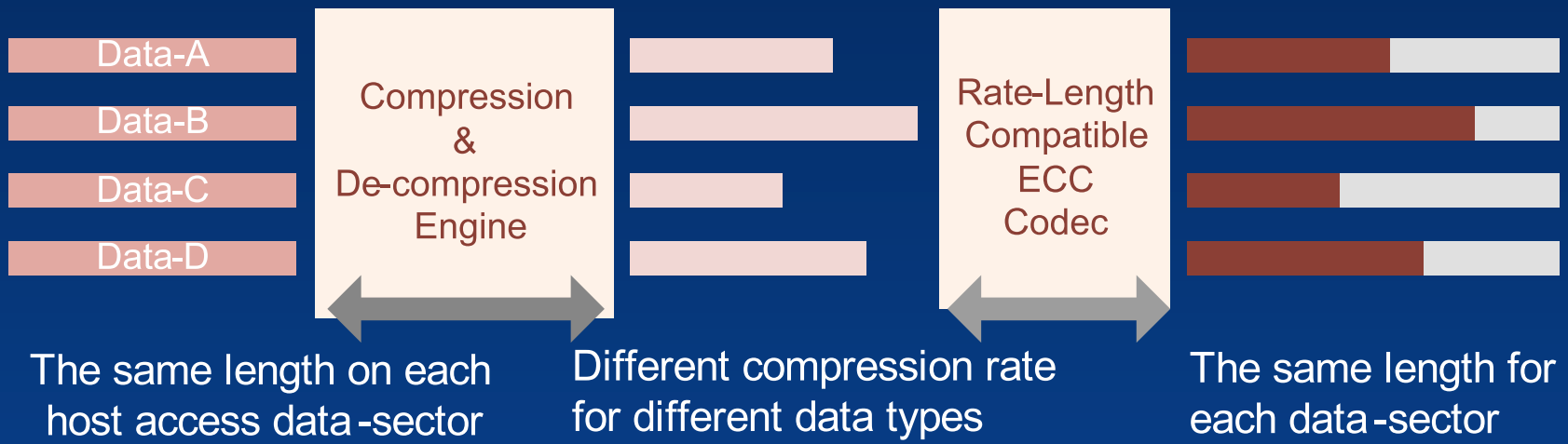
Original after compression:

0➔3, **1**➔2, **2**➔7, ……, **E**➔3, **F**➔4

Compression Ratio



From Source Coding to Channel Coding

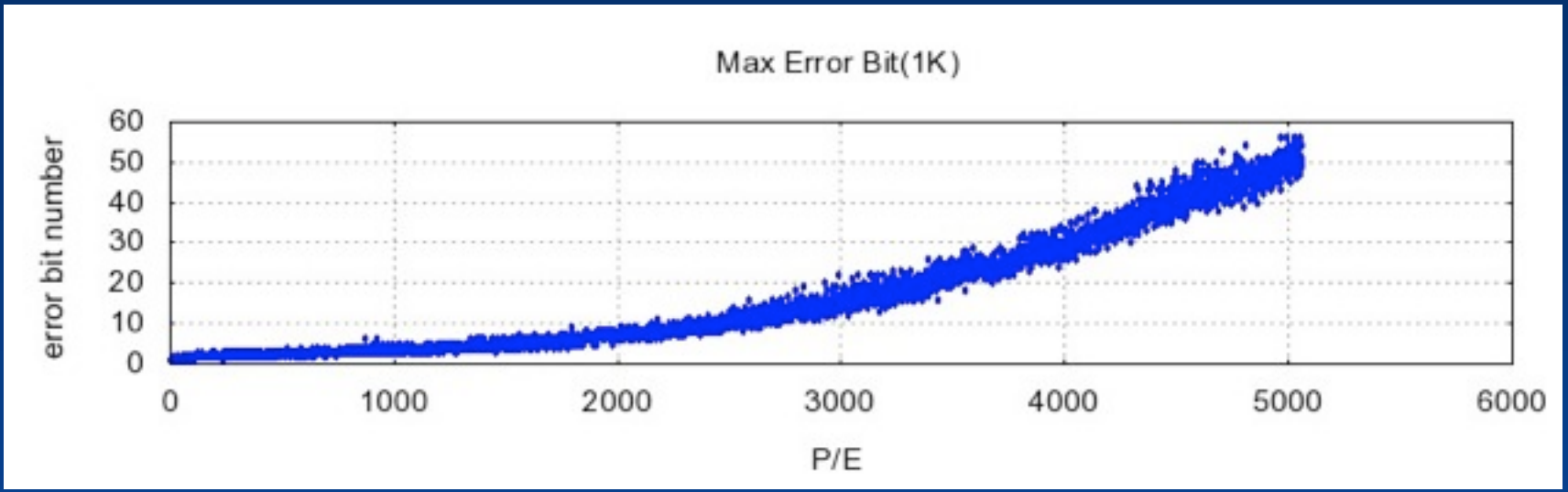


- Different data types have different compression rates and result in different lengths after compression.
- Different parity lengths provide different protection capabilities.
- While combining the two strategies, the data-sector related to OS reliability will be protected in a better manner.
- Each data-sector should be in equal length while being written to flash.

Examples of Different Protection Capabilities

- Original: (1024B + 42B)
  - ➔ 24-bit protection (total length 1066B)
- Compression rate 91% (940B +126B)
  - ➔ 72-bit protection (total length 1066B)
- Compression rate 80% (814 + 252B)
  - ➔144-bit protection (total length 1066B)
- Compression rate 67% (688B+ 378B)
  - ➔216-bit protection (total length 1066B)
- If the original compression rate is 5%, it can provide double correction capability.
  - ➔(982B + 84B = 48-bit protection on the 1066B)

Example of TLC Flash



- If the requirement of error correction is 24-bit/1K, this mechanism can extend the flash life time from P/E cycle = 3000 to P/E cycle = 5000 with 7% compression rate.
- If only focus on the region of P/E cycle < 2000, this mechanism will improve the system reliability.

Conclusion

- The adoptions of the innovative and advanced techniques and their combinations definitely facilitate the applications of new flash memories in SSD.
- Silicon Motion presents a new SSD storage system to improve the overall system reliability from different aspects.
- Advanced error correction codes with soft-decoding can be employed in the mentioned techniques and solve the broadening distribution of Vth.

Thank You!

Q & A

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