Efficient Coding Schemes for Flash Memories

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UCSD

University of California San Diego

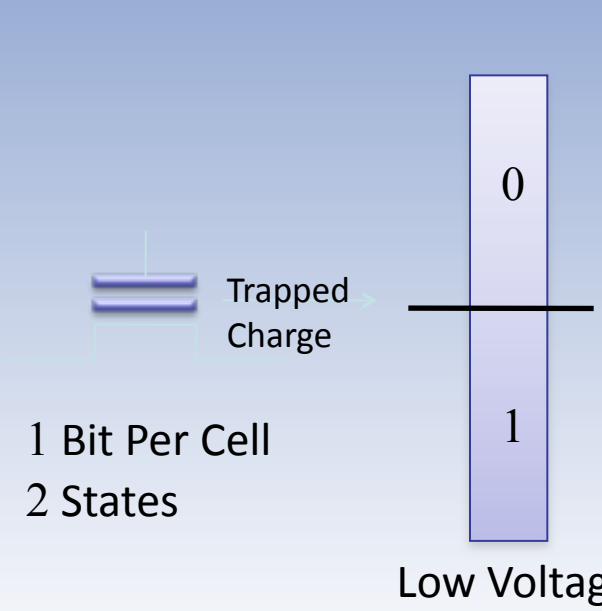
Flash Memory Summit, August 2010

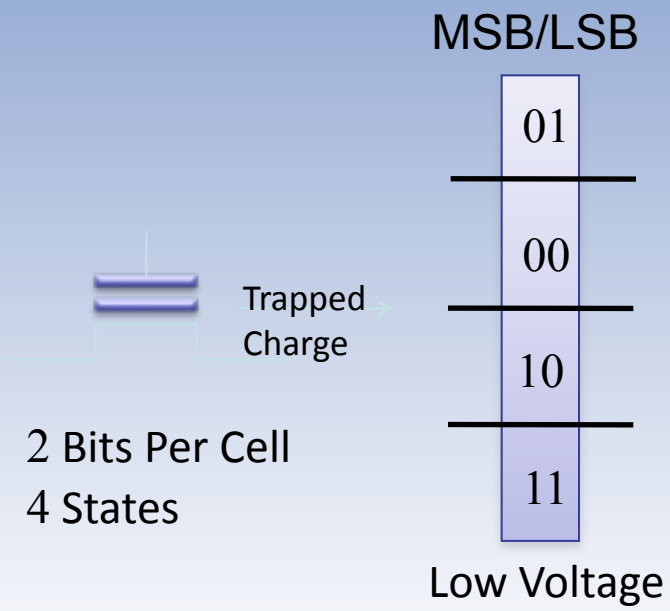
Outline

- Flash Memory Structure
- Single Bit Representation in MLC Flash
- New ECC Scheme for MLC Flash
- WOM-Codes

SLC Vs. MLC Flash

- In SLC flash, each cell stores a single bit
- In MLC, each cell can store multiple bits (typically 2 bits)





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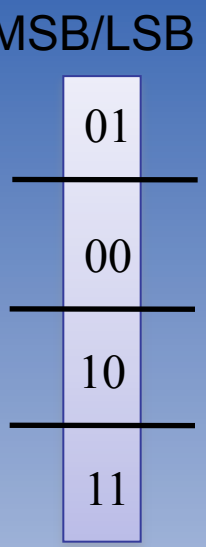

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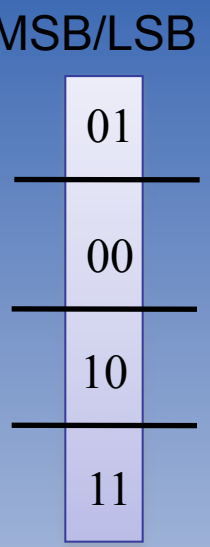

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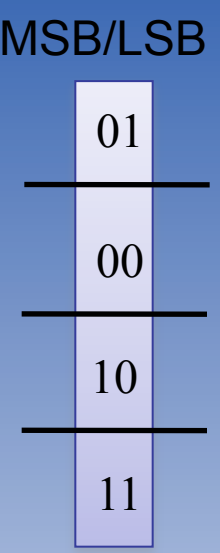

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Row index	**MSB** of **first** 2^{14} cells	**LSB** of **first** 2^{14} cells	**MSB** of **last** 2^{14} cells	**LSB** of **last** 2^{14} cells
1	page 0	page 4	page 1	page 5
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  - The experiment was done in a lab conditions and related factors such as temperature change, intervals between erasures or multiple readings before erasures were not considered

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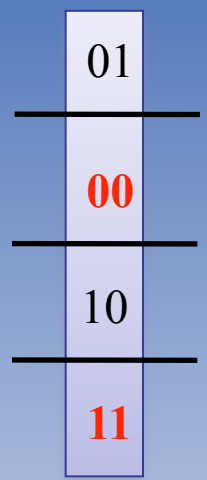

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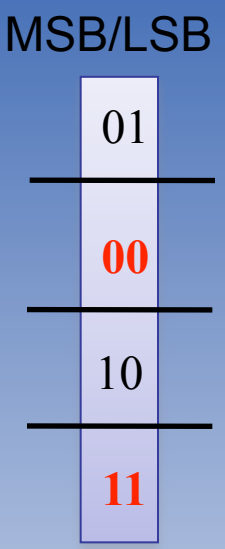

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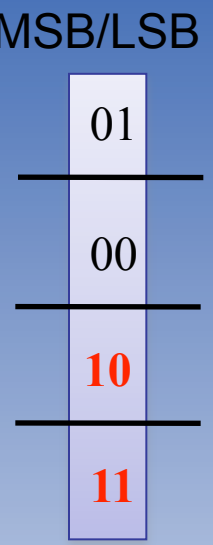

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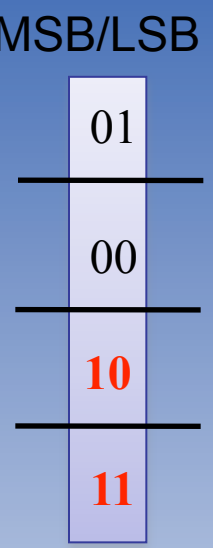

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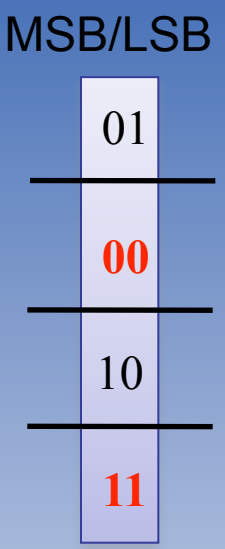

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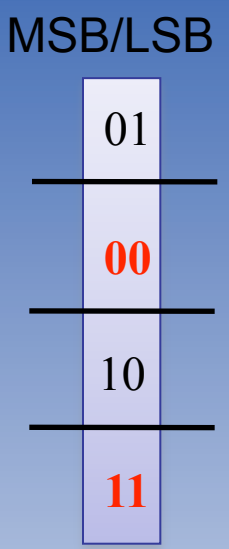

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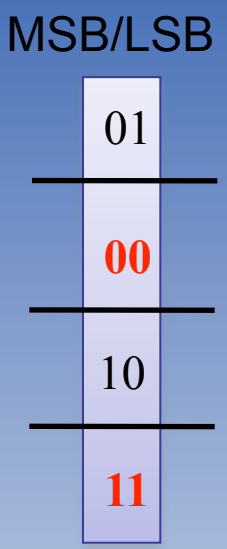

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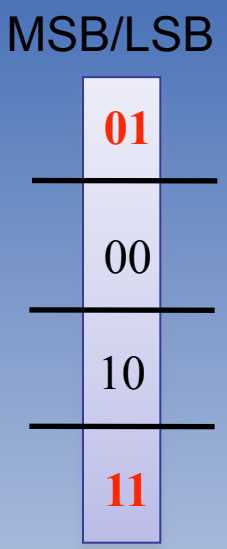

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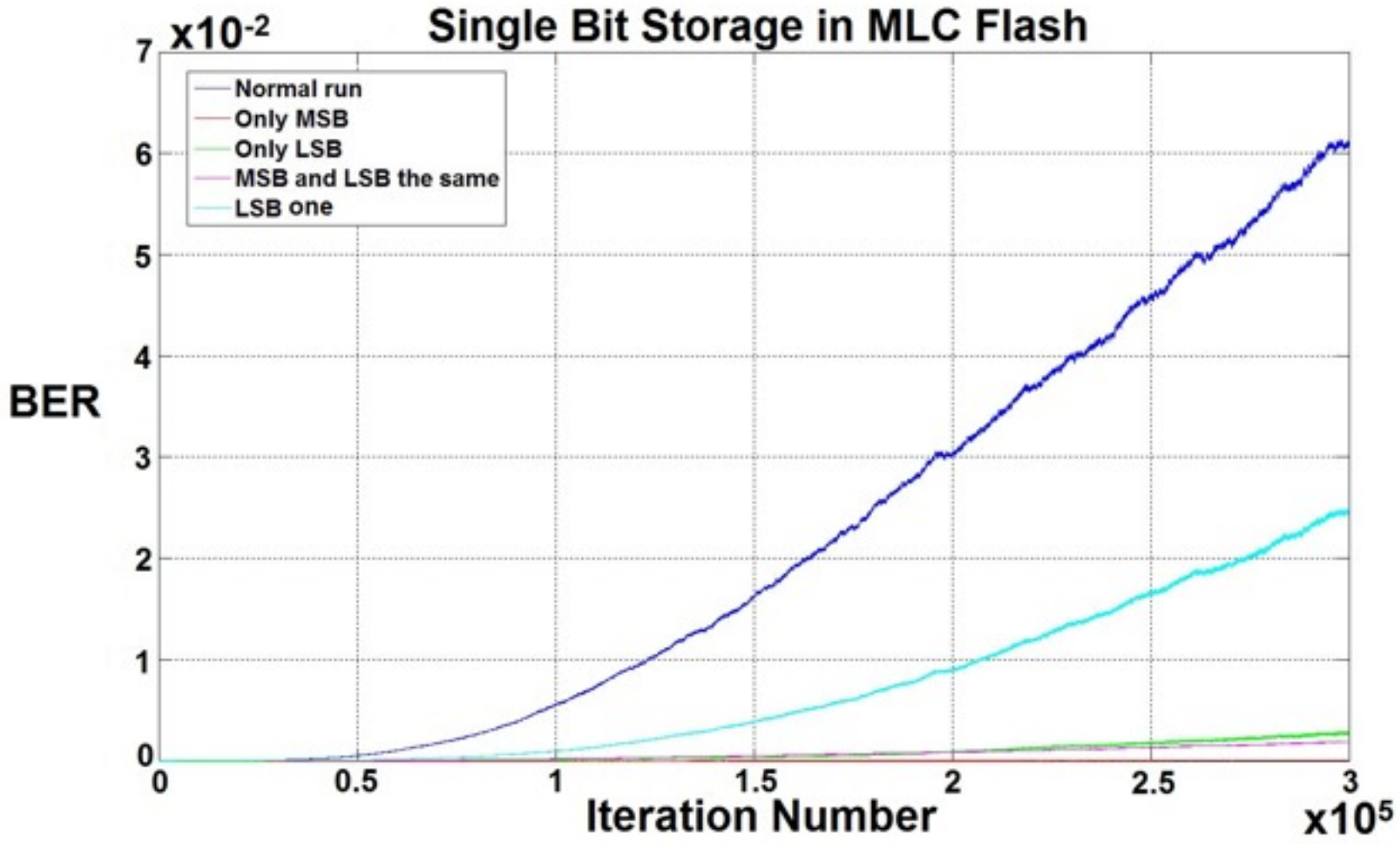

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- What happens when the chip is first used as an **MLC** and then switched to be used as an **SLC**?
- We ran the following experiments:
  - Use the chip for **50,000** iterations as an **MLC** and **150,000** iterations as an **SLC**
  - Use the chip for **100,000** iterations as an **MLC** and **100,000** iterations as an **SLC**
  - Use the chip for **150,000** iterations as an **MLC** and **50,000** iterations as an **SLC**

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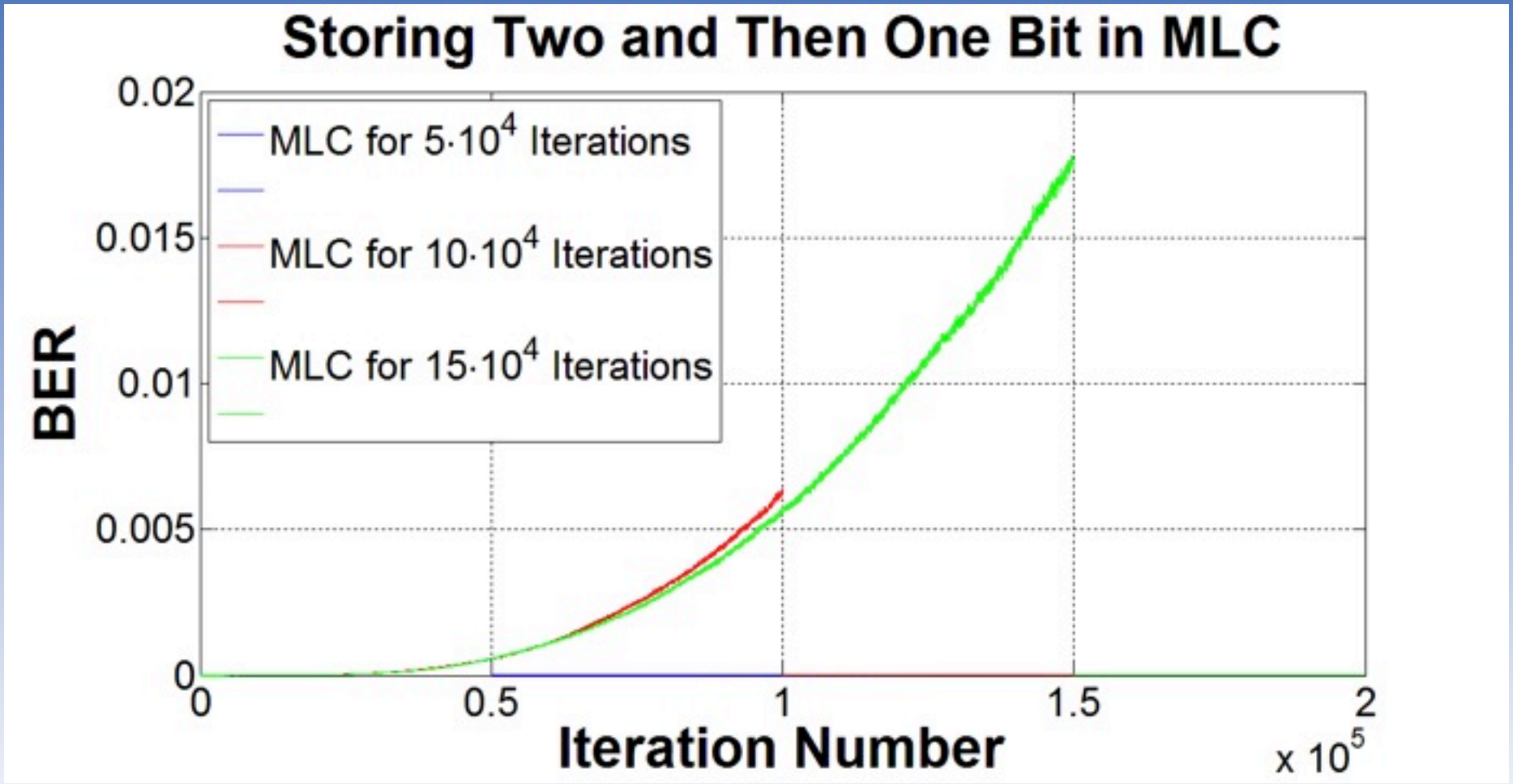

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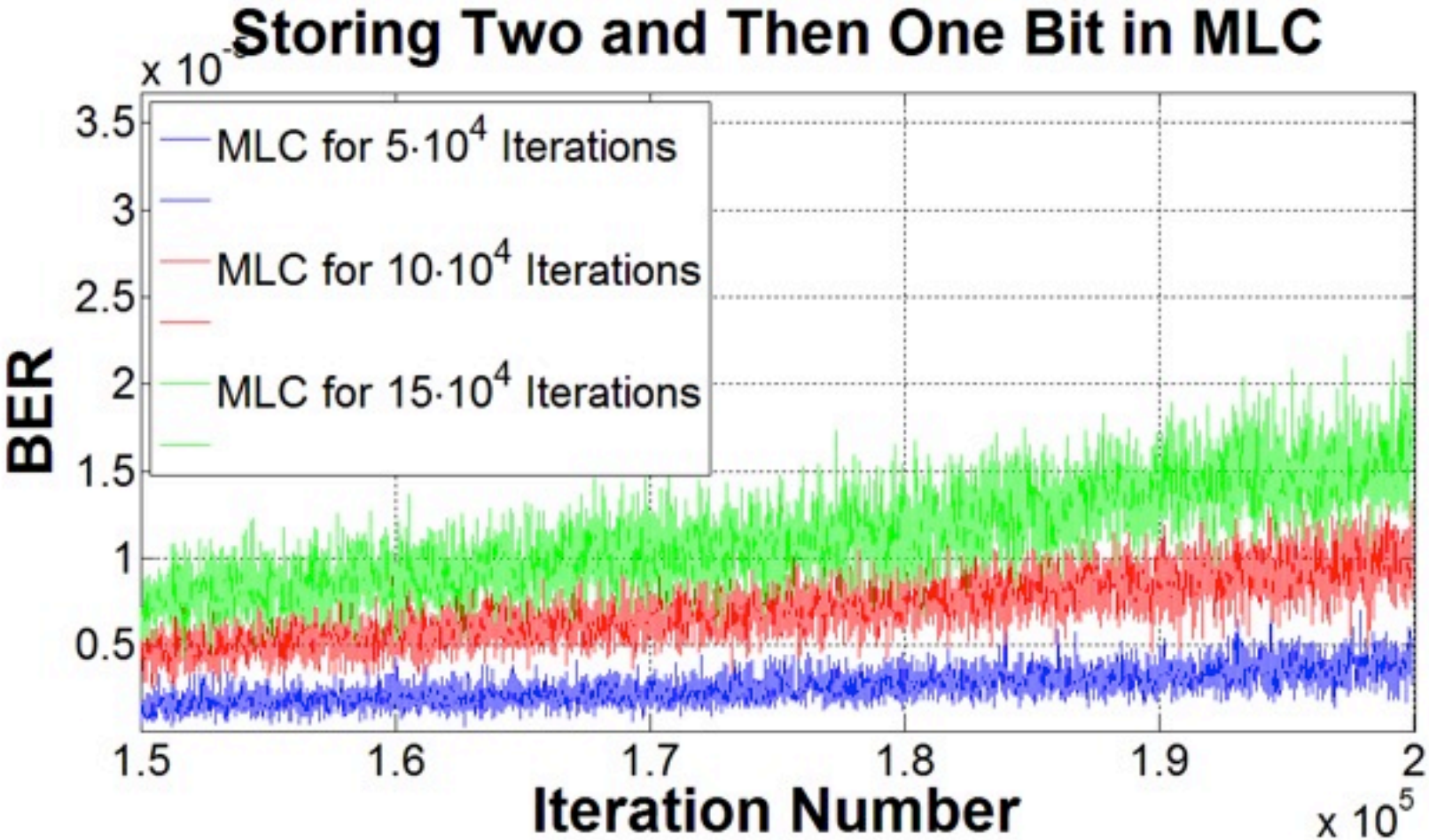

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- If a cell is in error, its level will typically increase by **one level**

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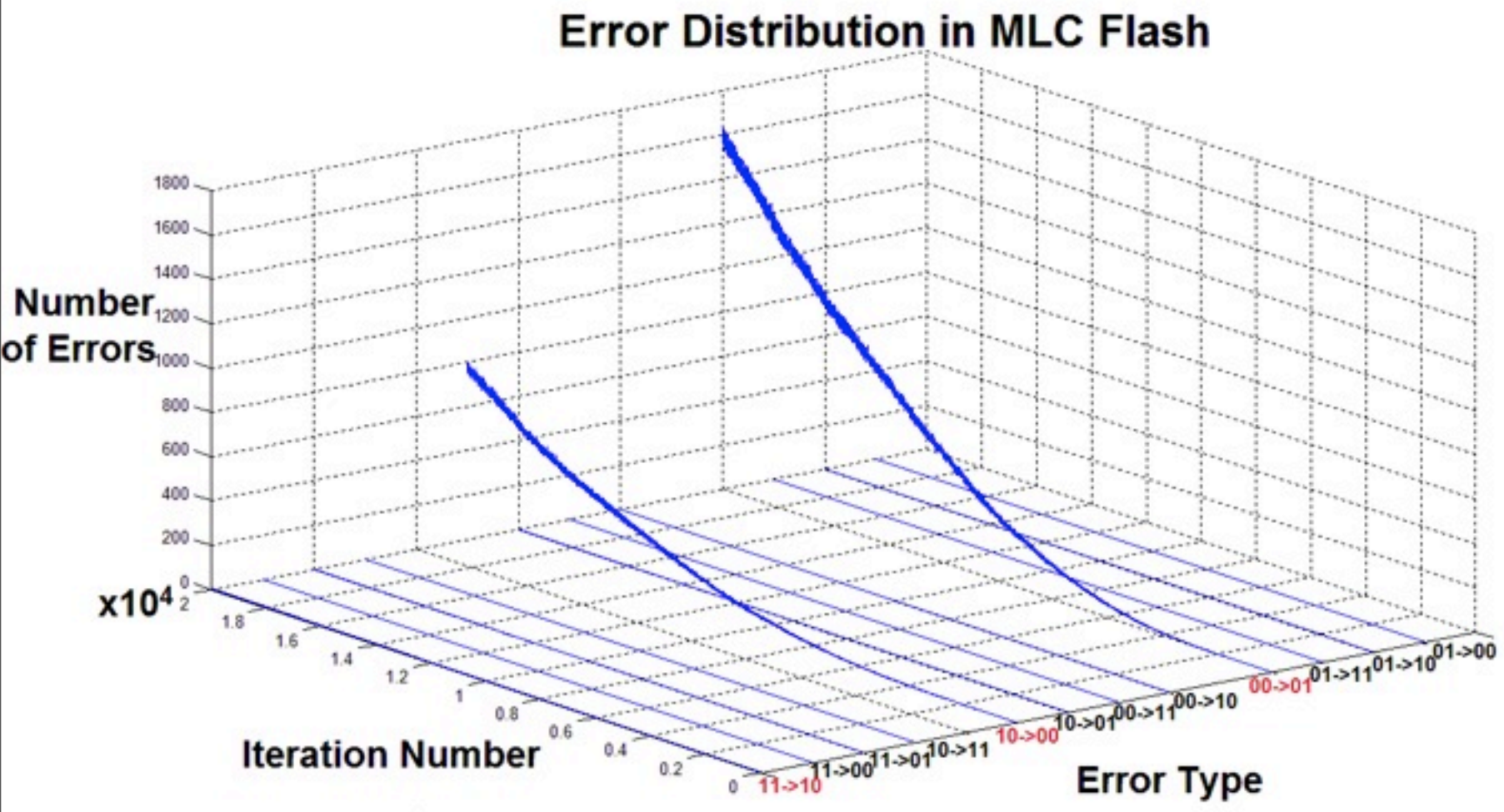

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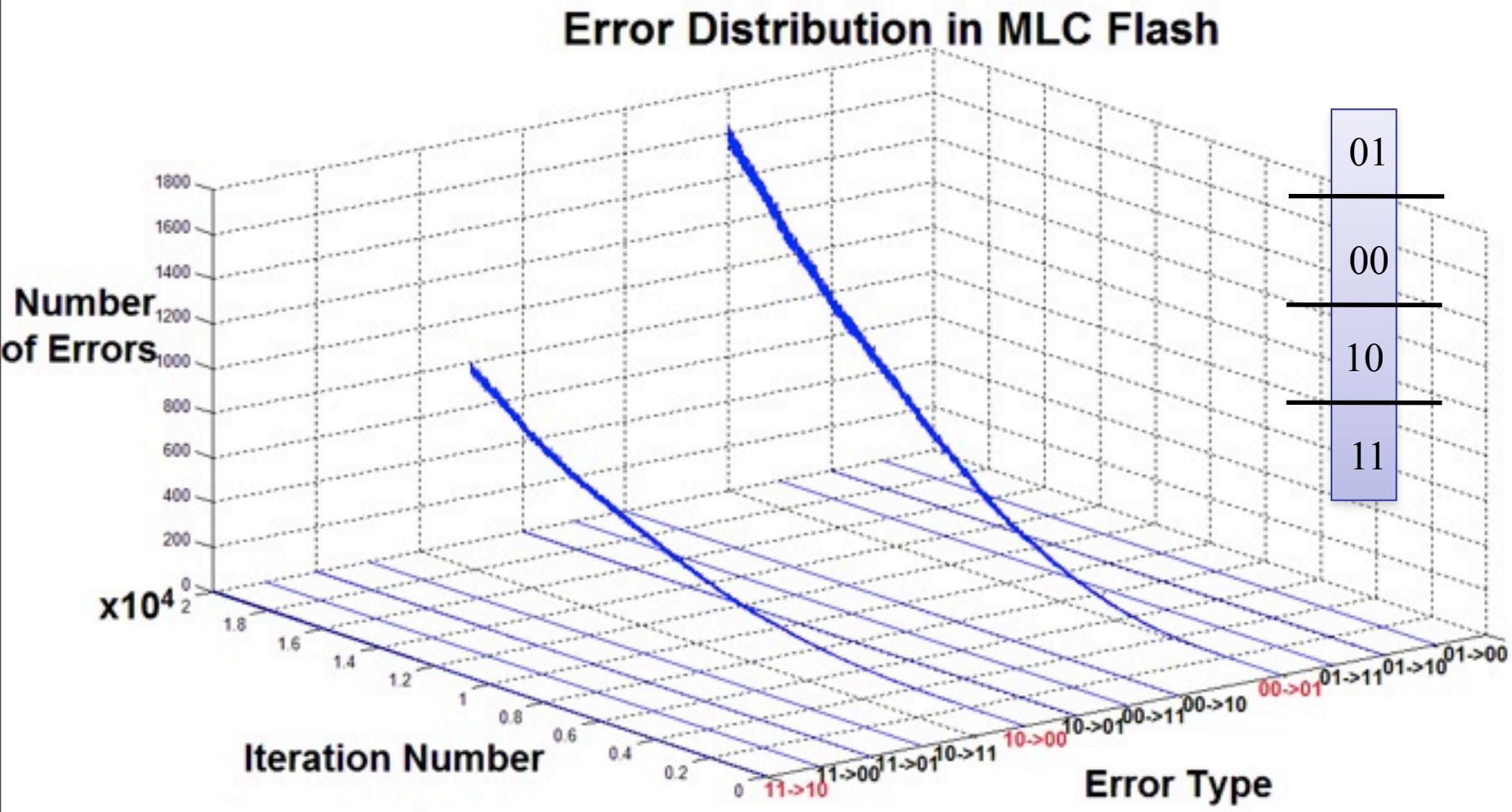

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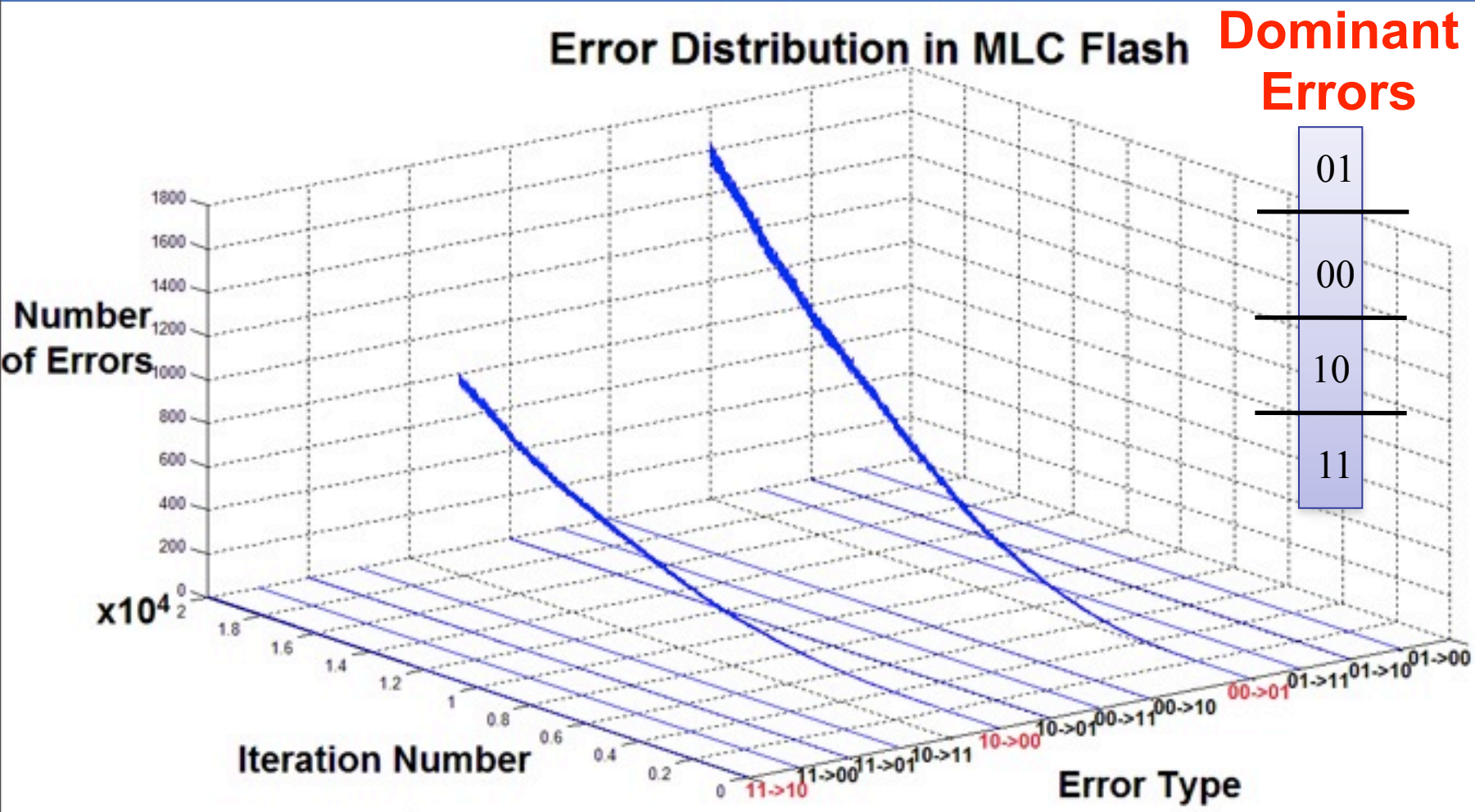

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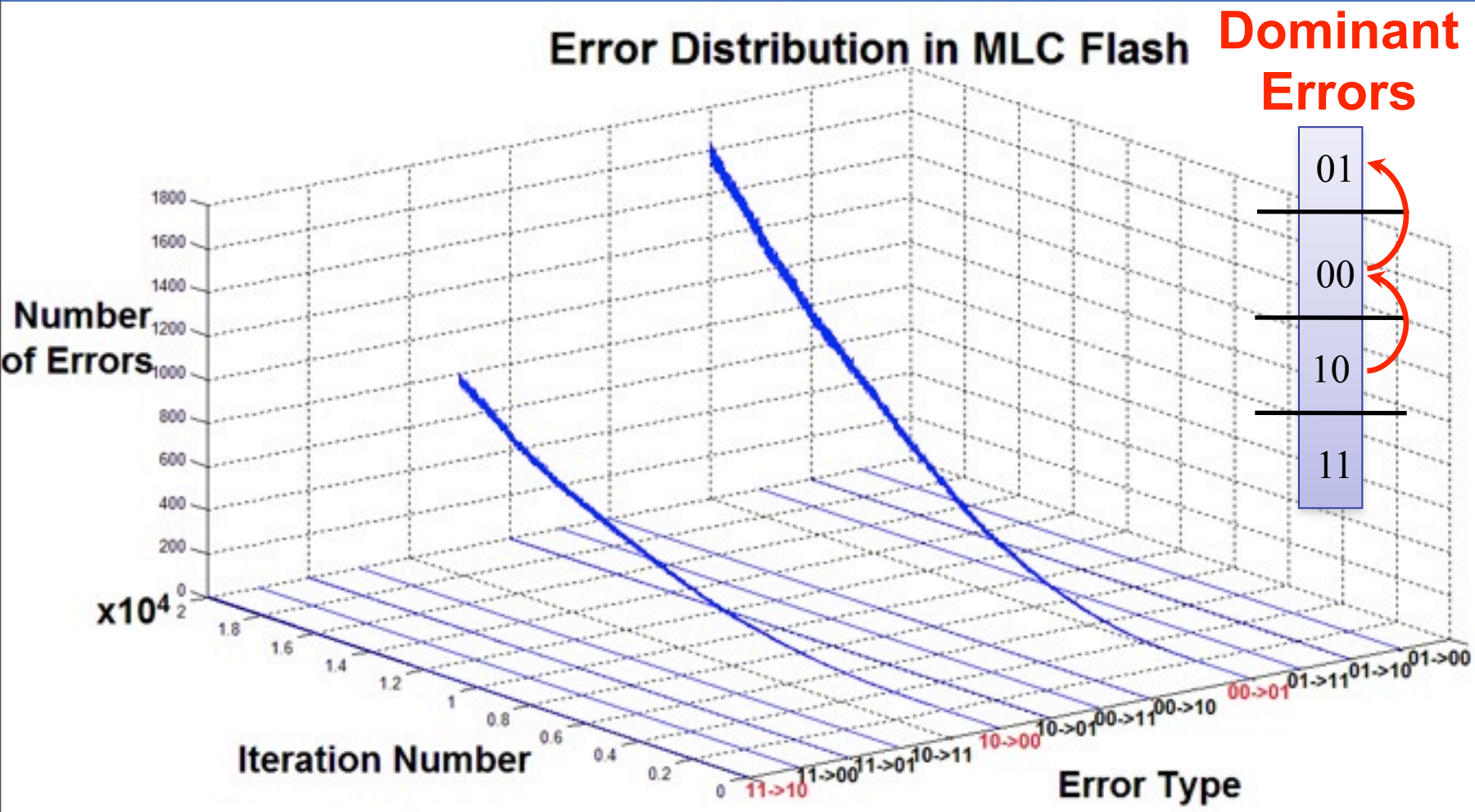

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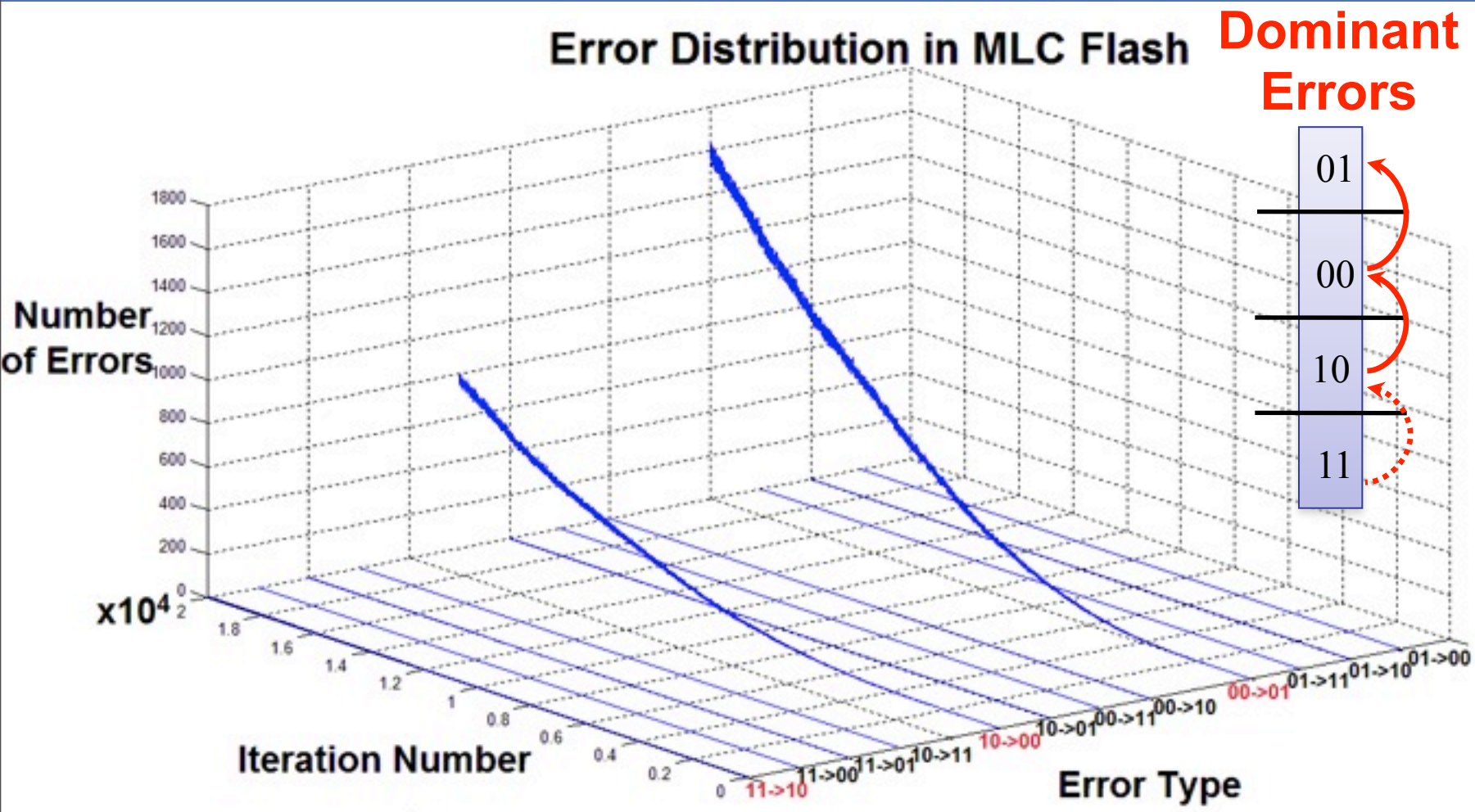

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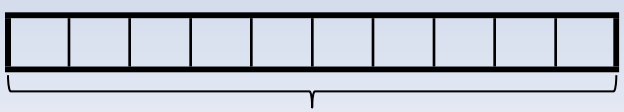

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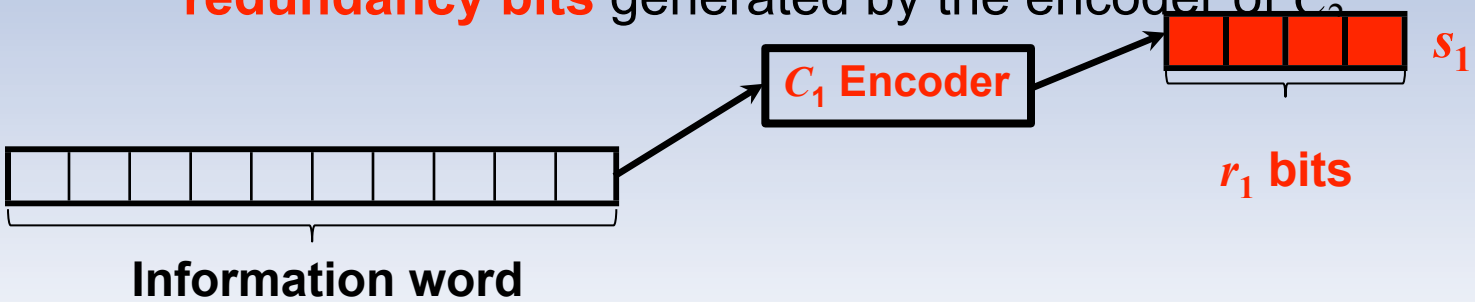

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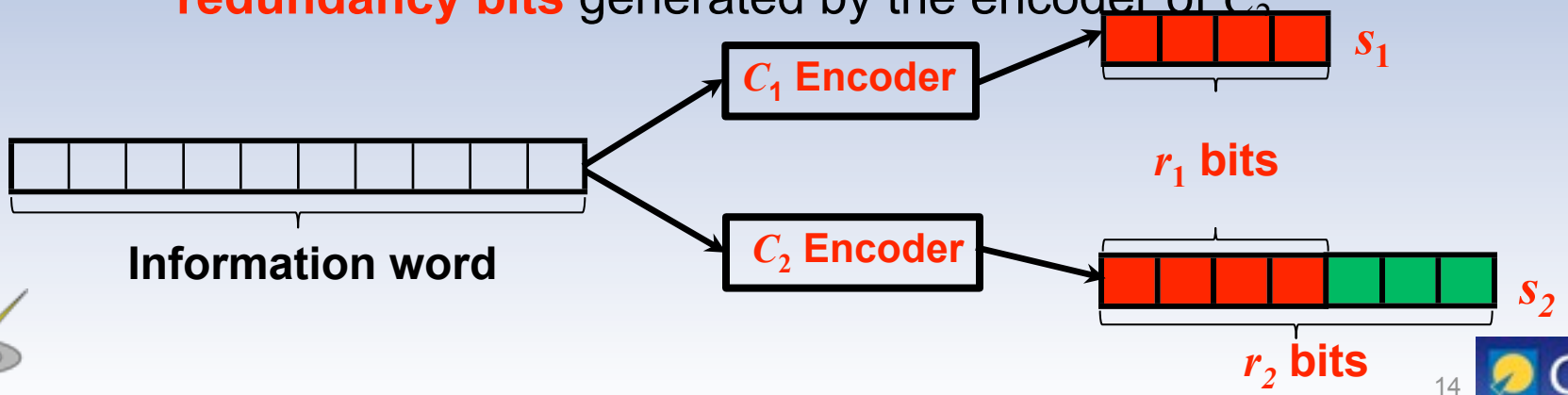

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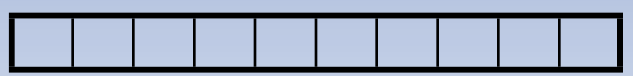

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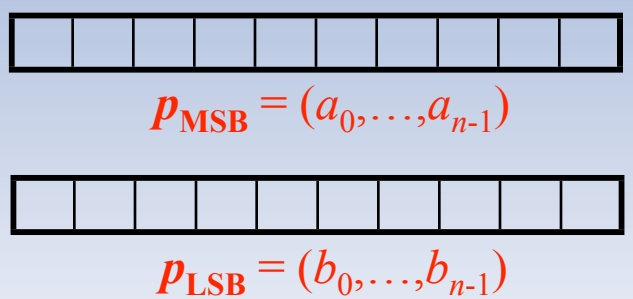

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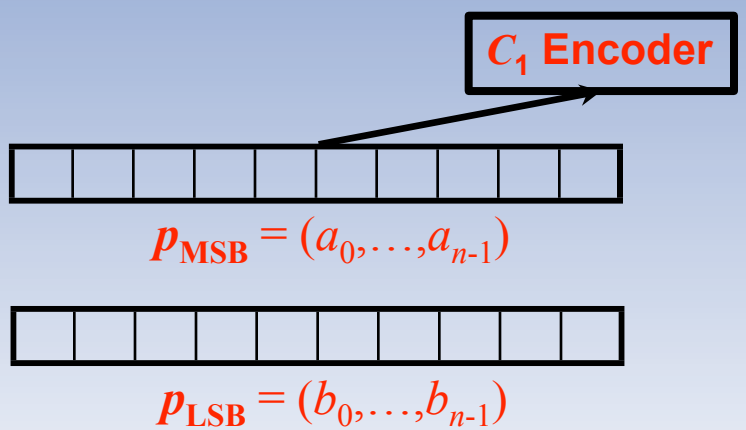

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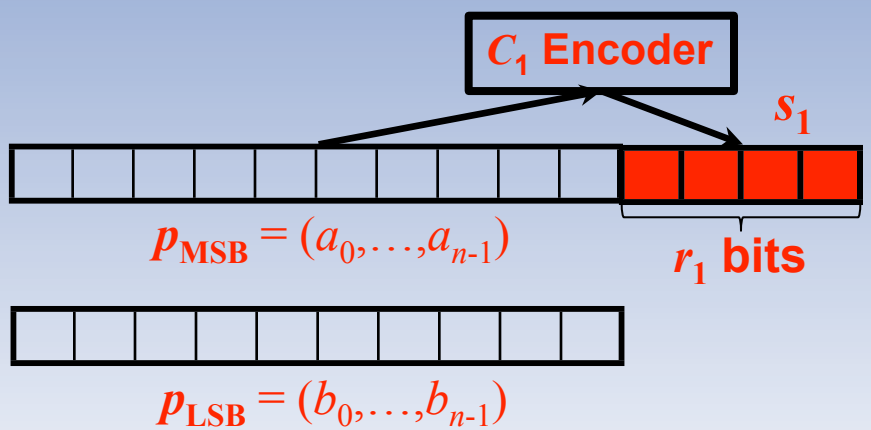

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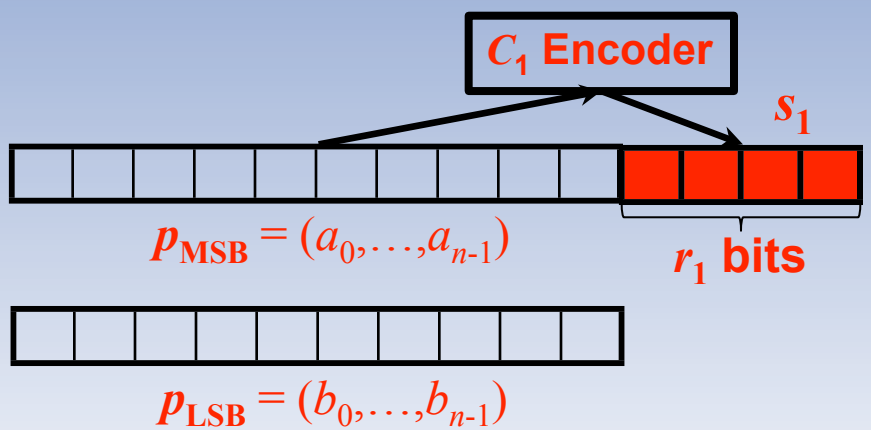

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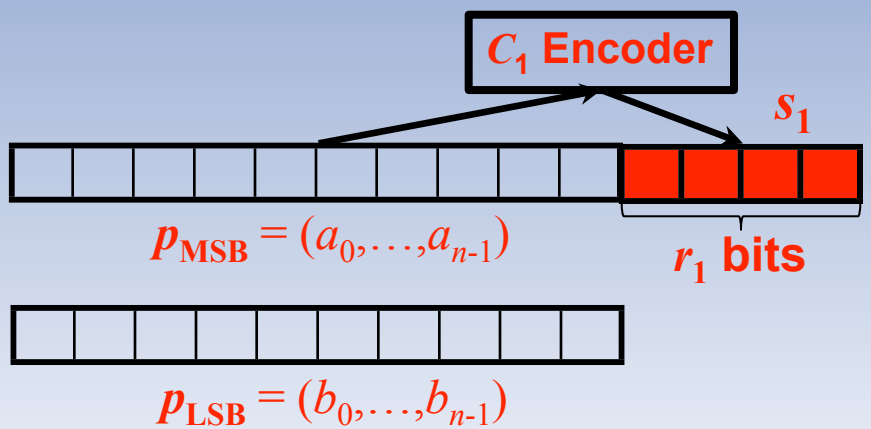

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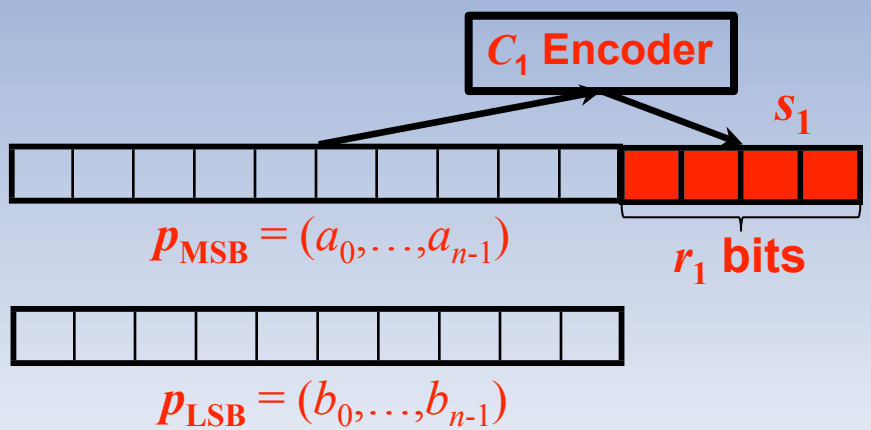

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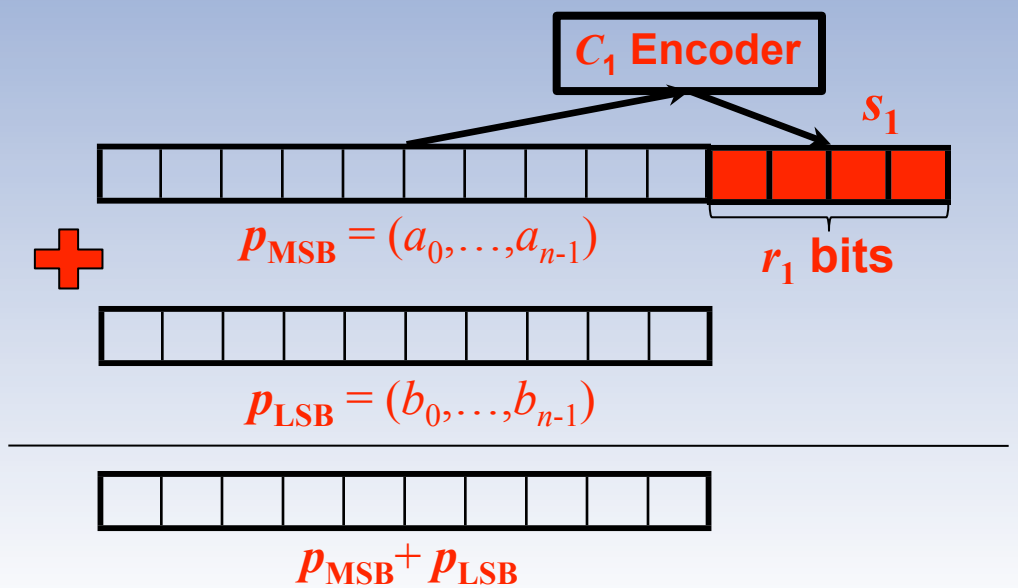

ECC scheme for MLC flash

- **Code construction**:
  - C_1 is a t_1-error-correcting BCH code, C_2 is a t_2-error-correcting BCH code, where $t_2 > t_1$, and the codes are compatible
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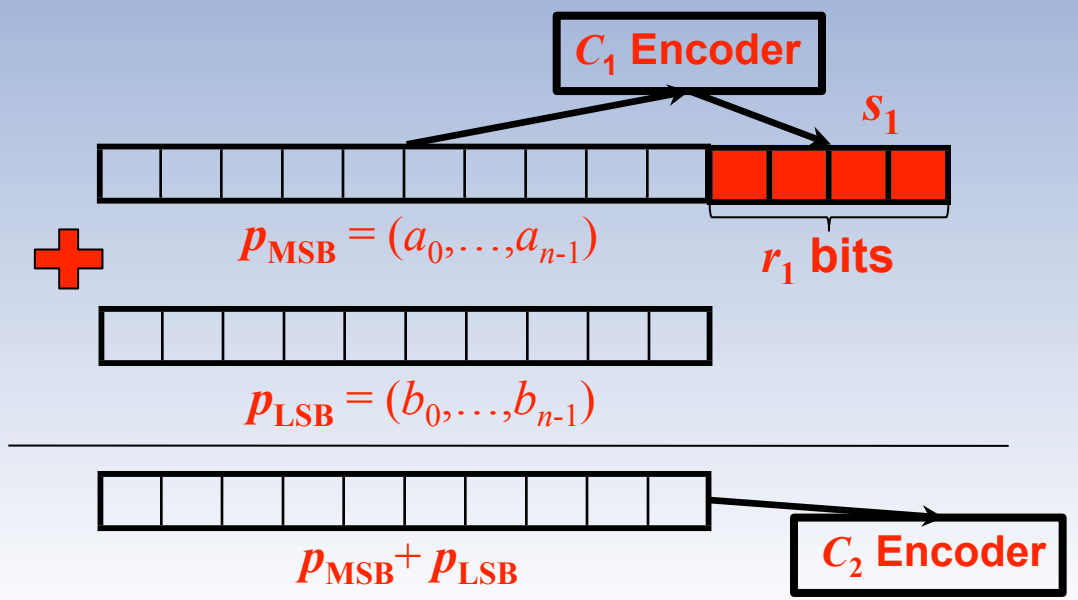

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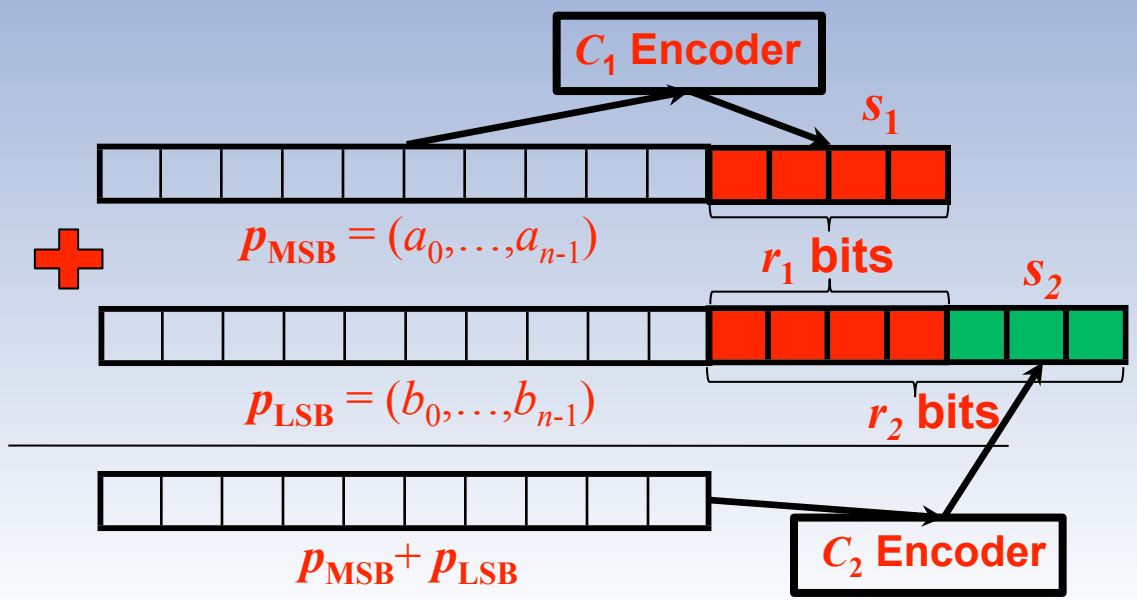

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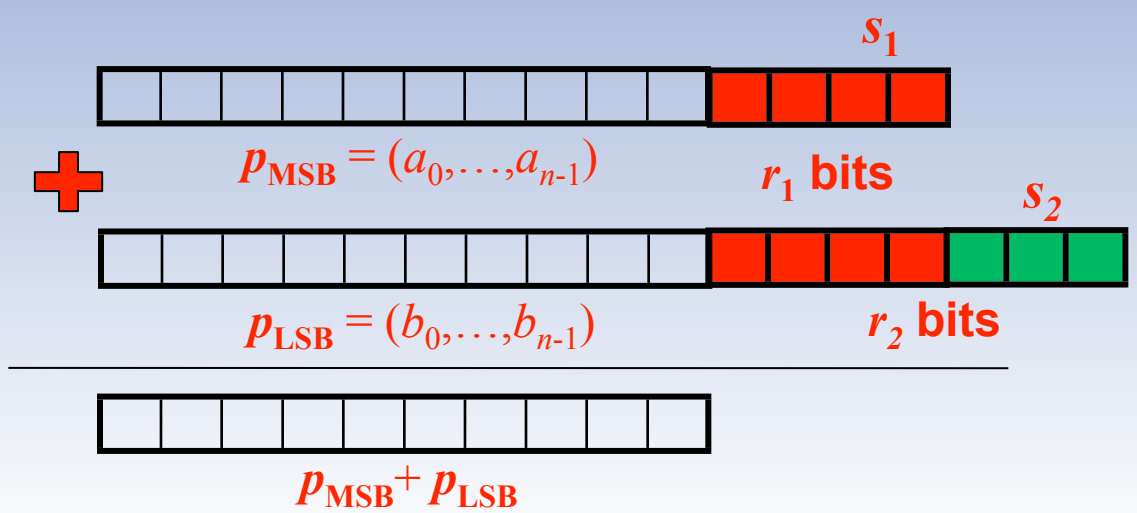

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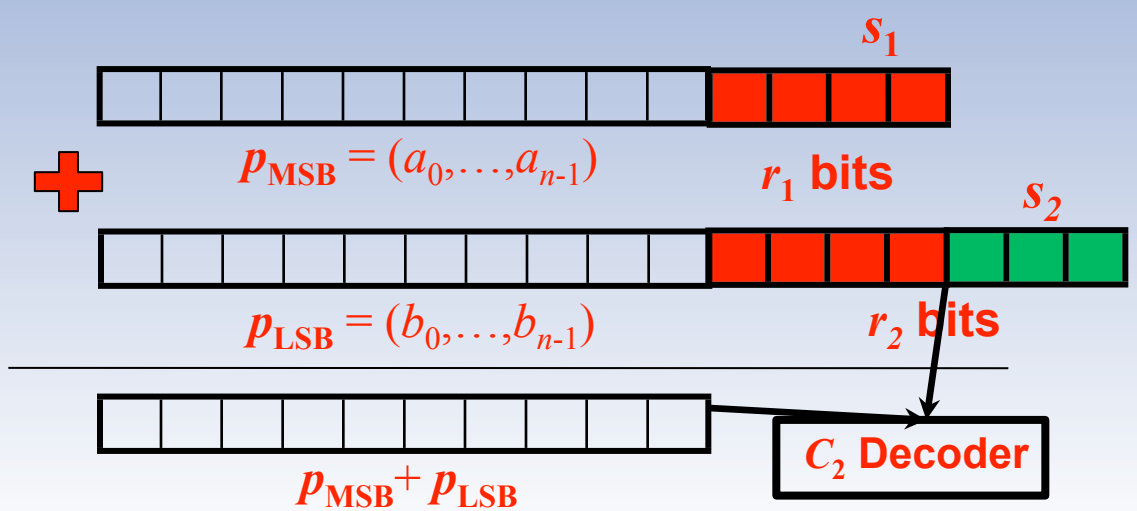

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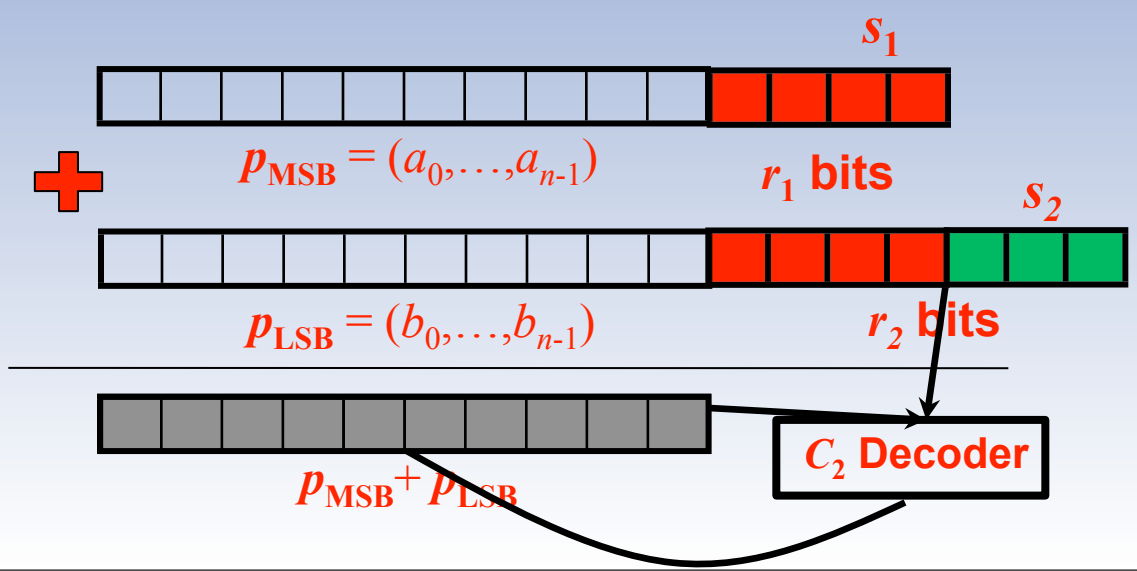

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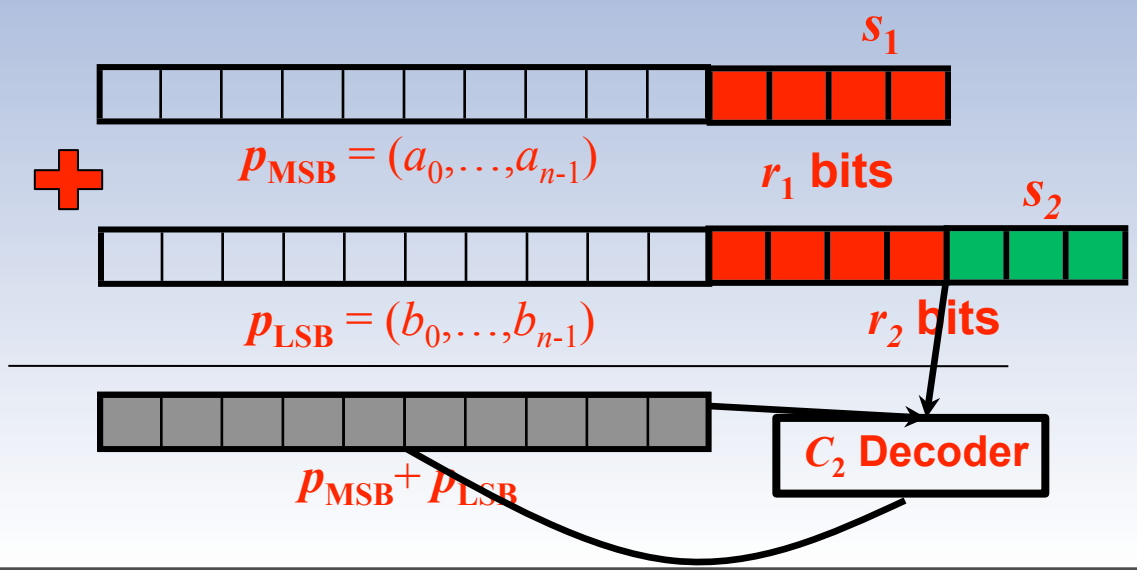

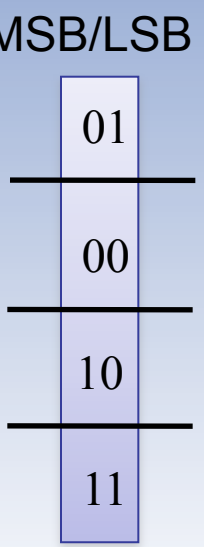

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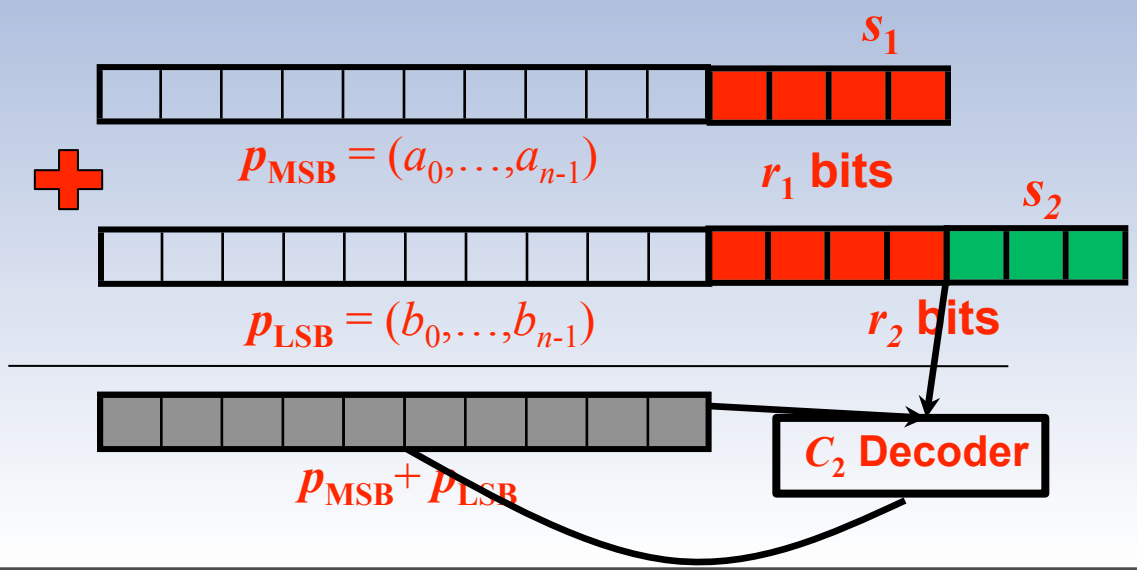

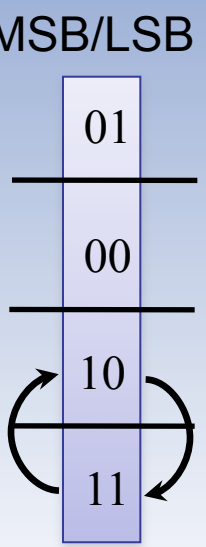

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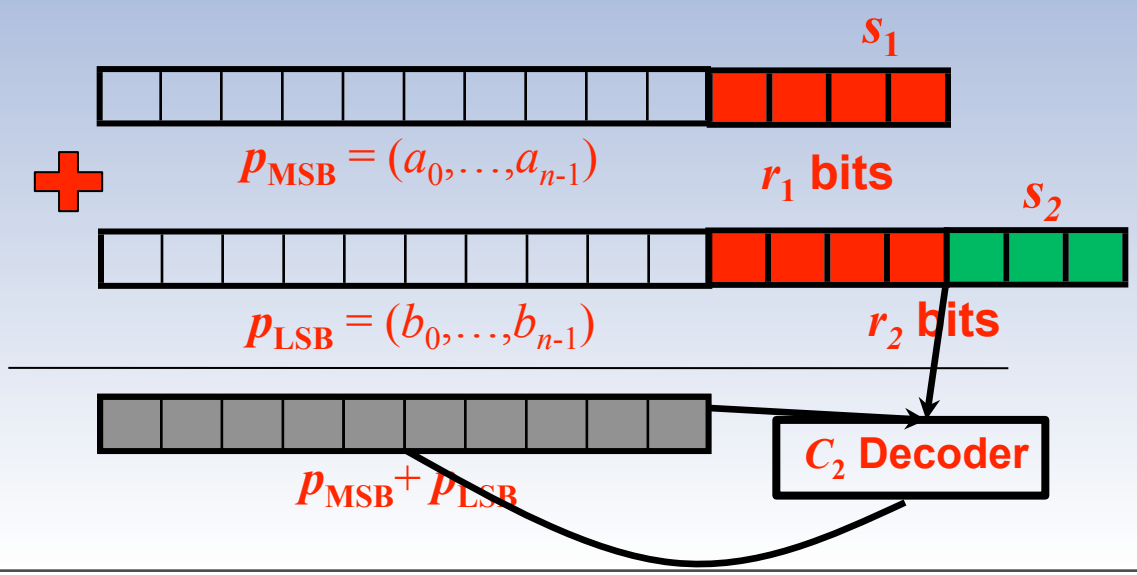

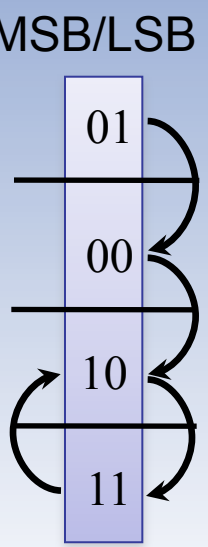

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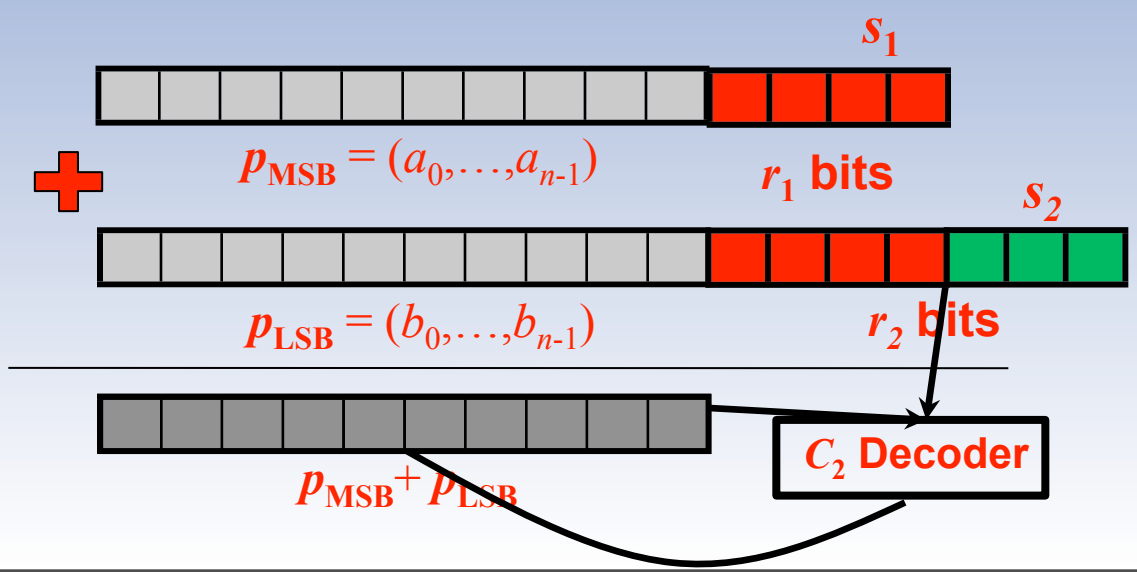

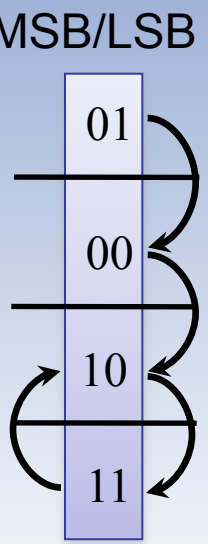

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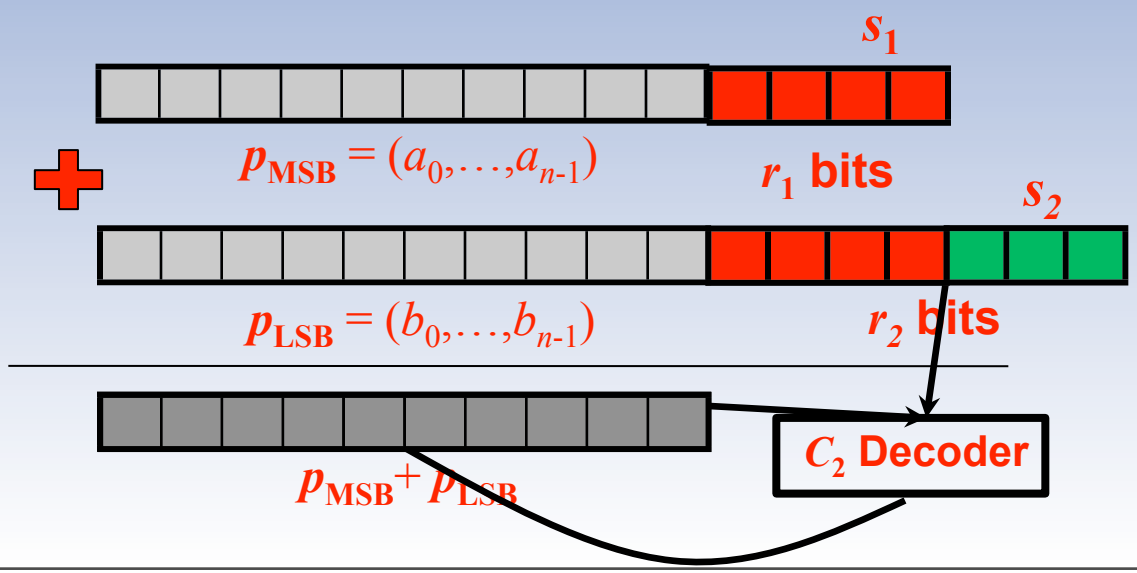

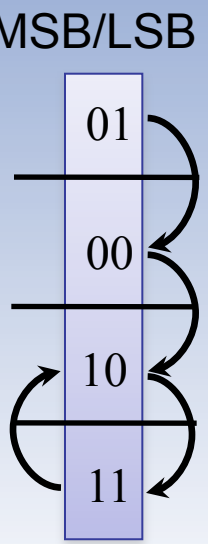

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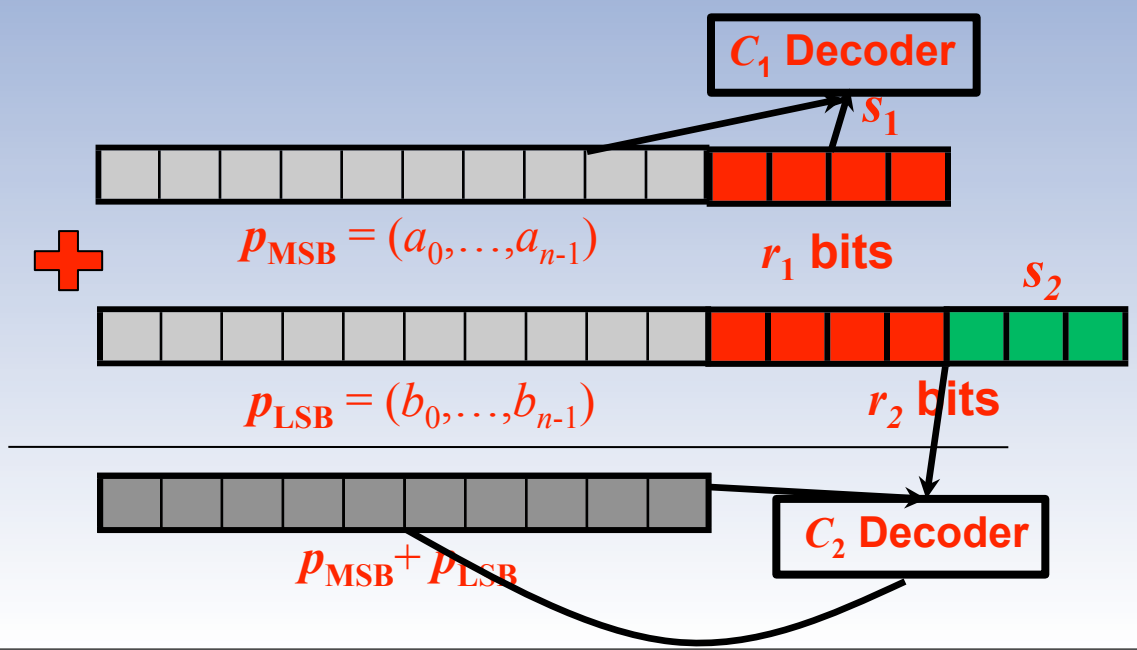

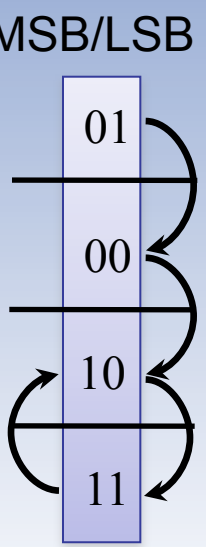

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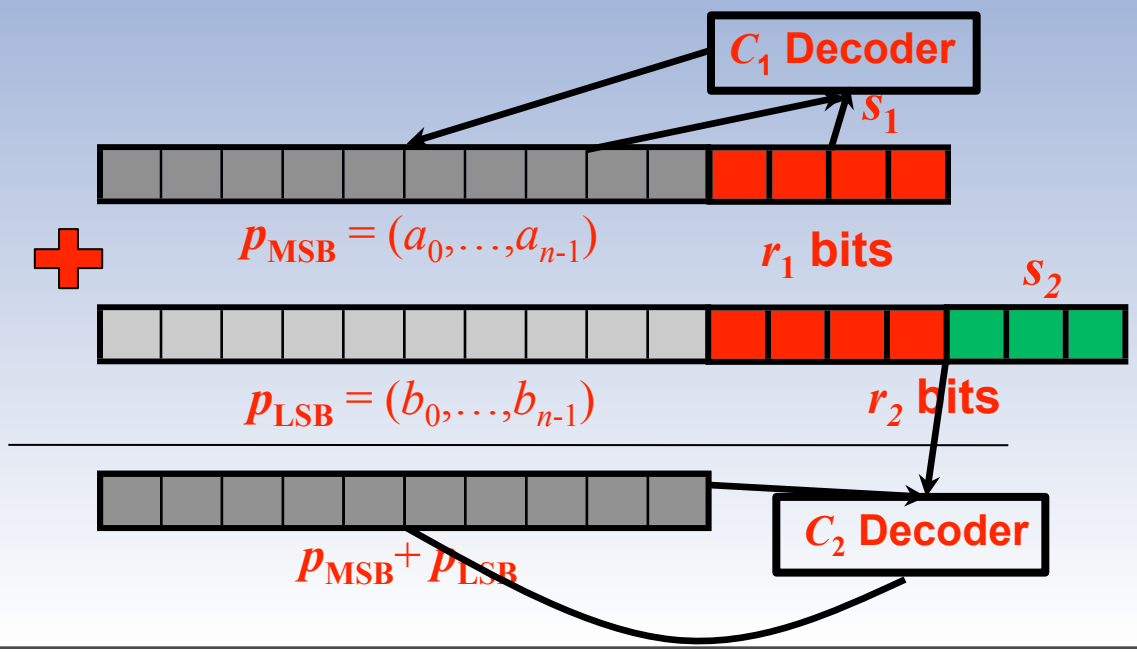

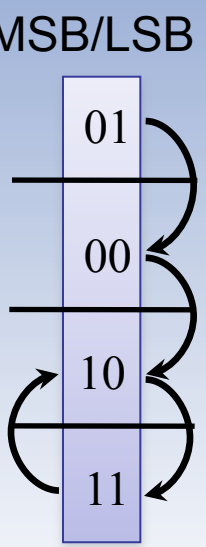

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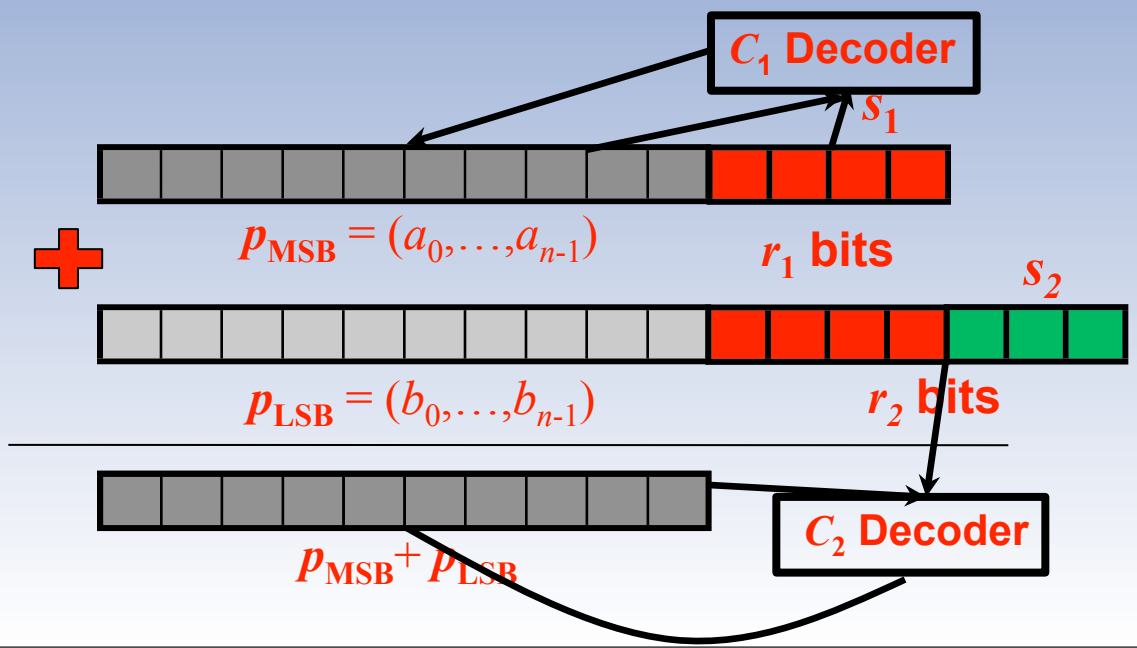

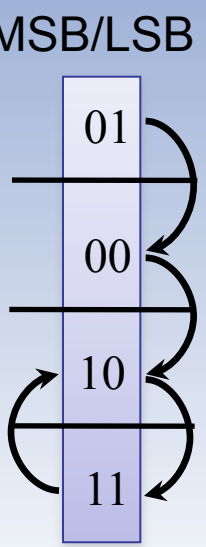

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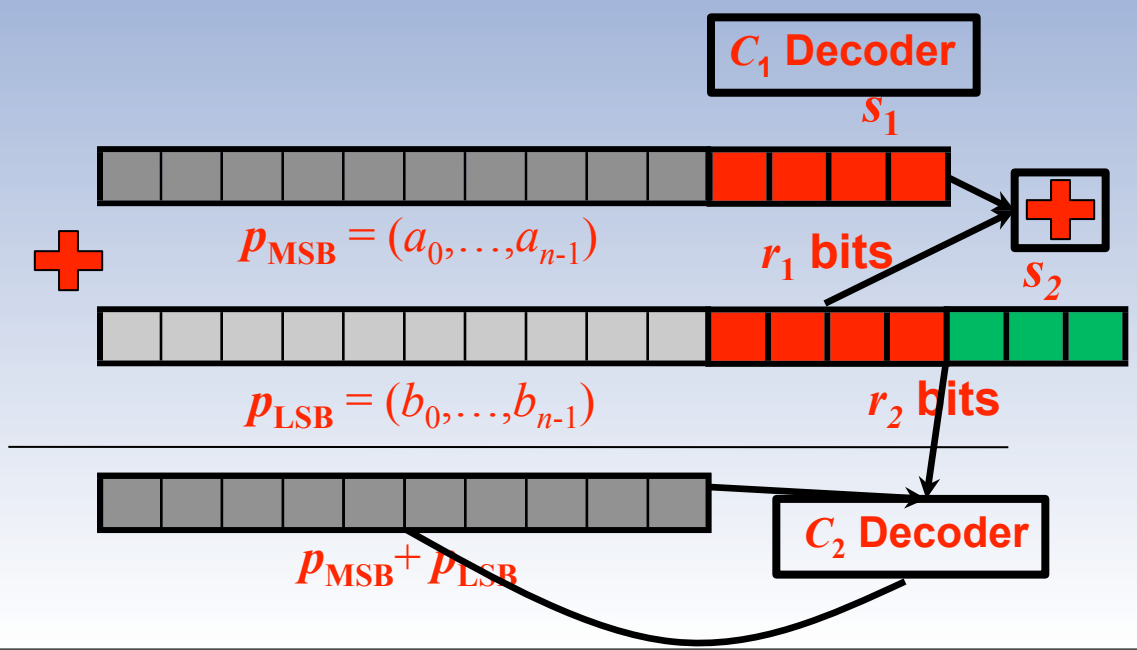

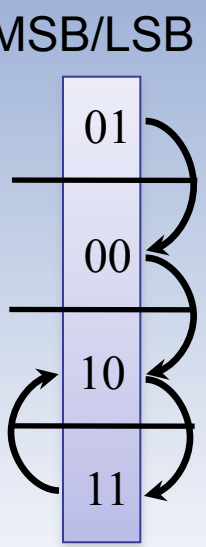

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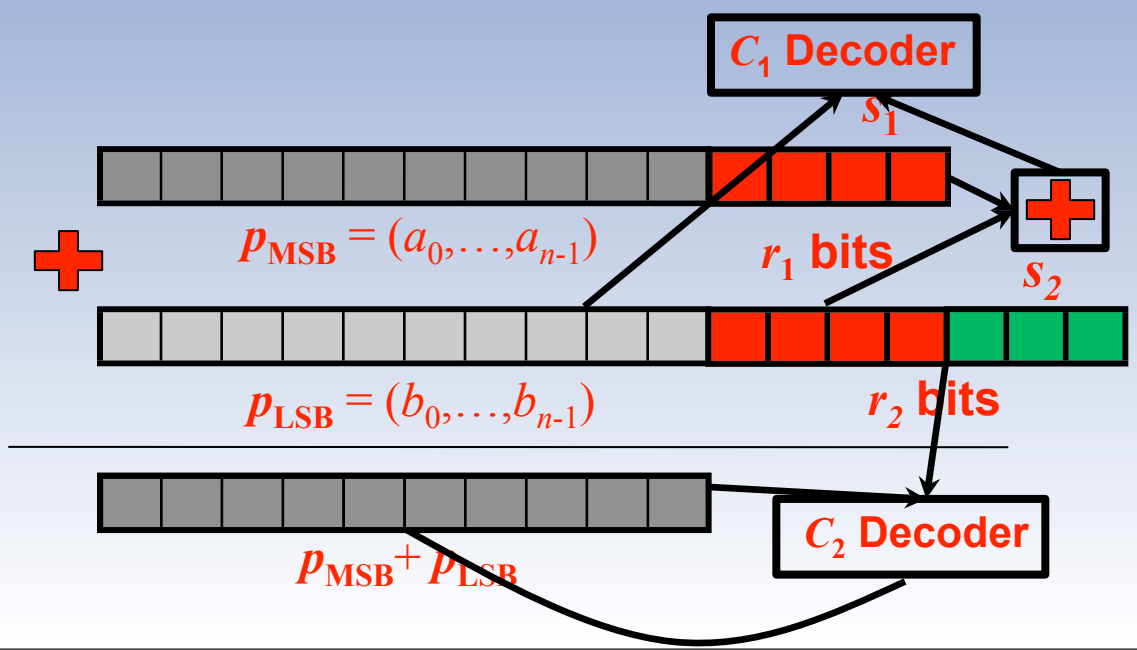

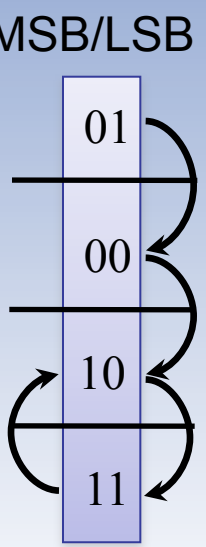

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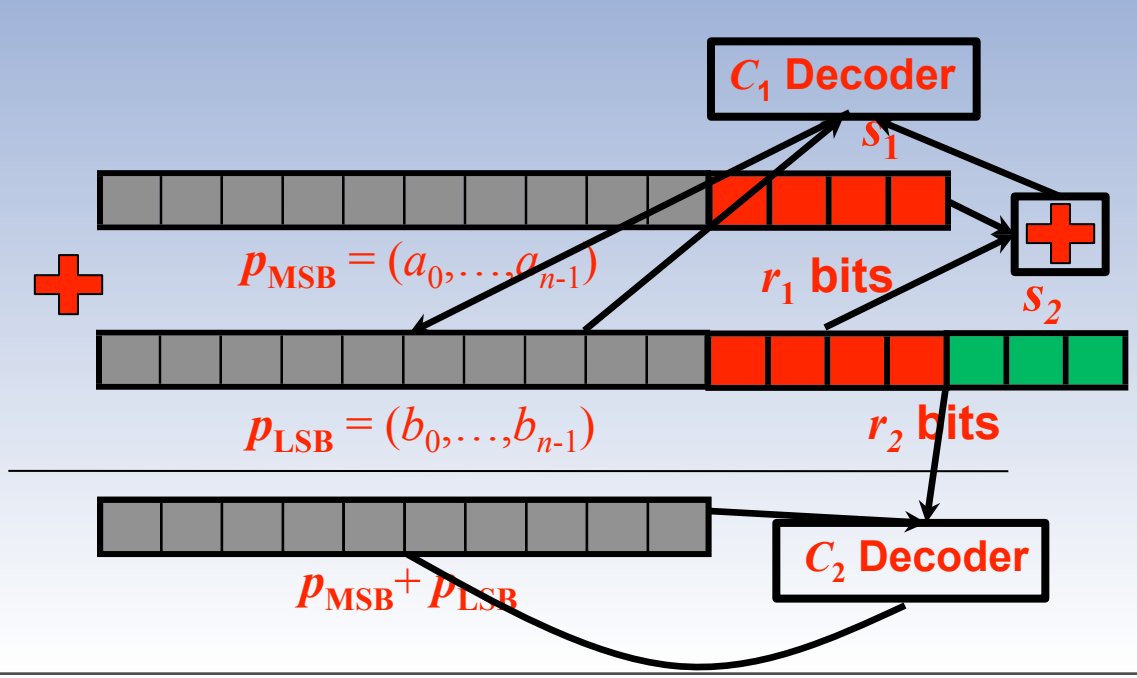
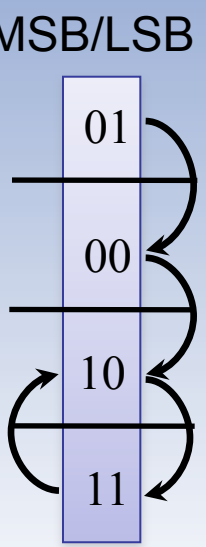
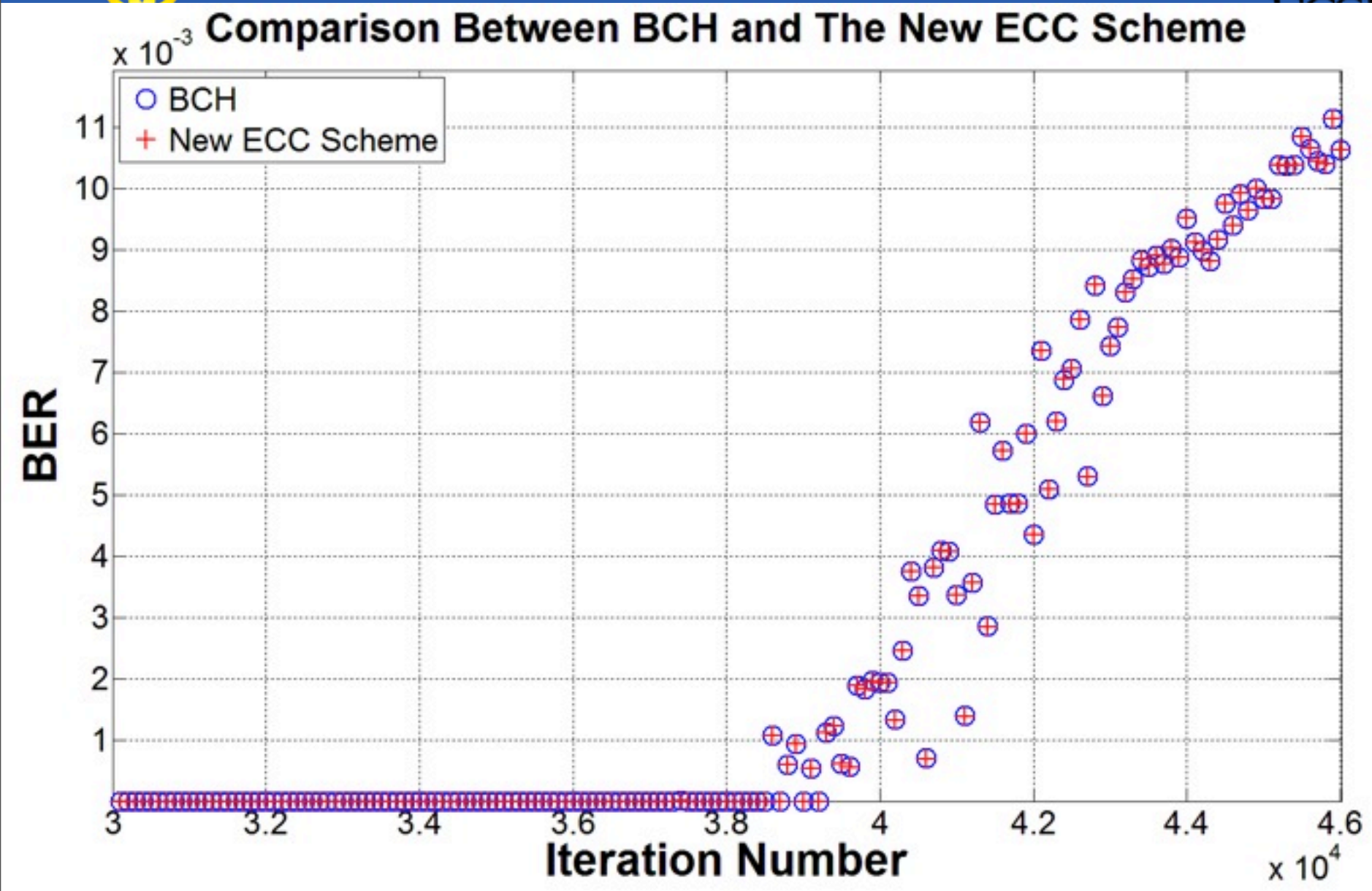
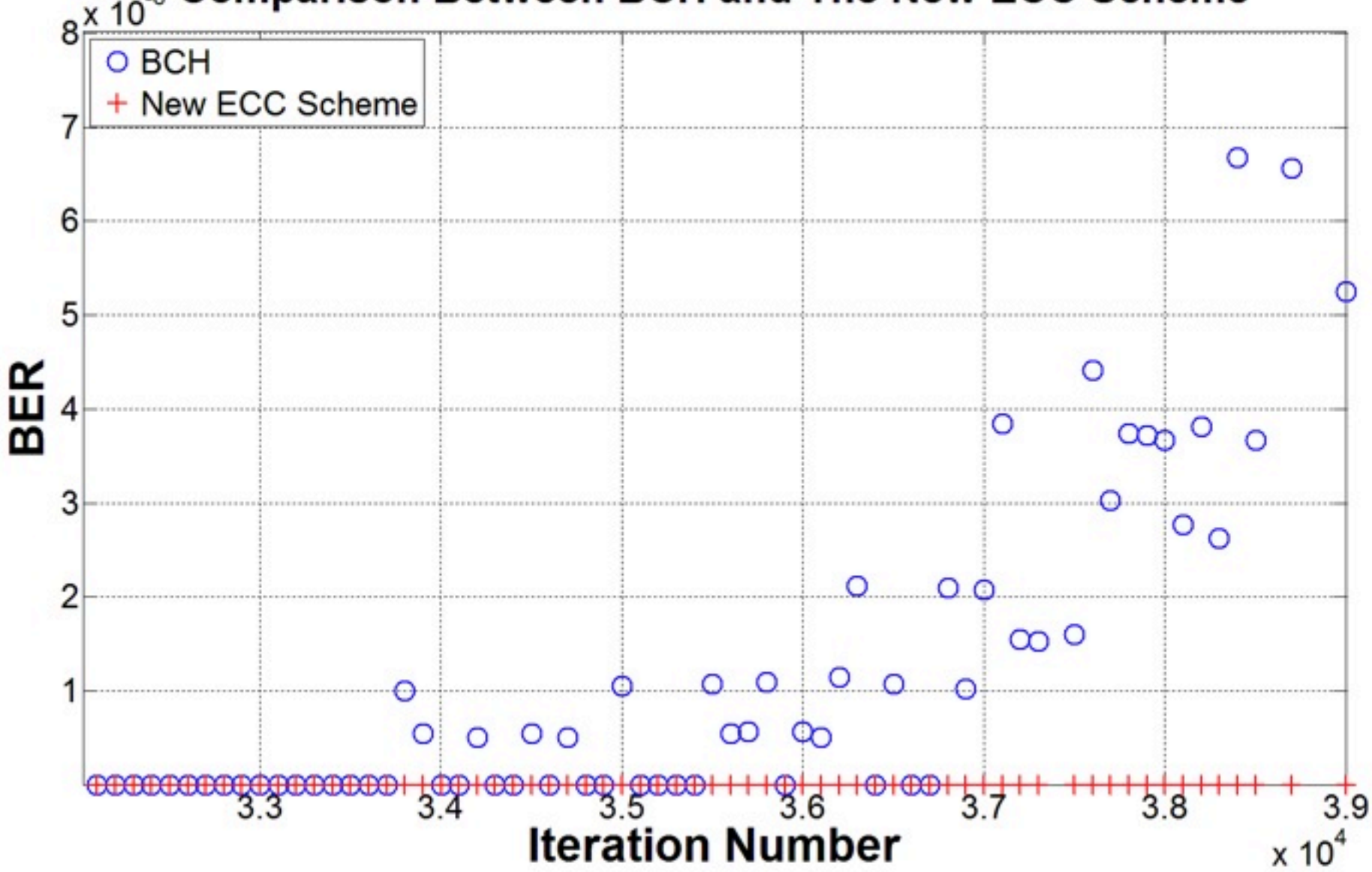





Comparison Between BCH and The New ECC Scheme
x 10^-3
BCH
New ECC Scheme
BER
11
10
9
8
7
6
5
4
3
2
1
3
3.2
3.4
3.6
3.8
4
4.2
4.4
4.6
Iteration Number
x 10^4

Comparison Between BCH and The New ECC Scheme



Write Once Memory (WOM) Codes for SLC

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data	1st write	2nd write
00	000	111
01	100	011
10	010	101
11	001	110

Write Once Memory (WOM) Codes for SLC

- A scheme for storing two bits twice using only three cells **before erasing the cells**

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Cells state

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data		
cells		

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Cells state

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data	01	
cells	100	

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Cells state

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cells	100	110

Write Once Memory (WOM) Codes for SLC

- A scheme for storing two bits twice using only three cells **before erasing the cells**
- The cells only **increase** their level

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Cells state

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cells	100	110

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- How to implement? (in **SLC** block)

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Cells state

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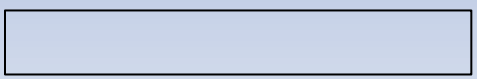

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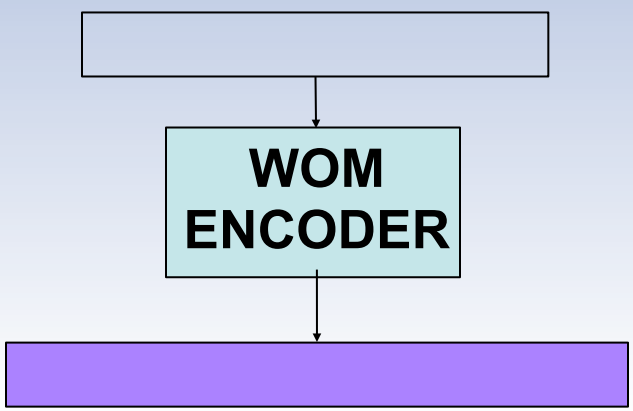

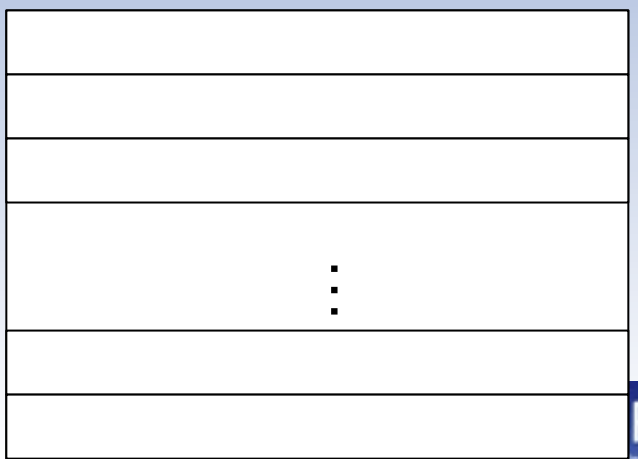

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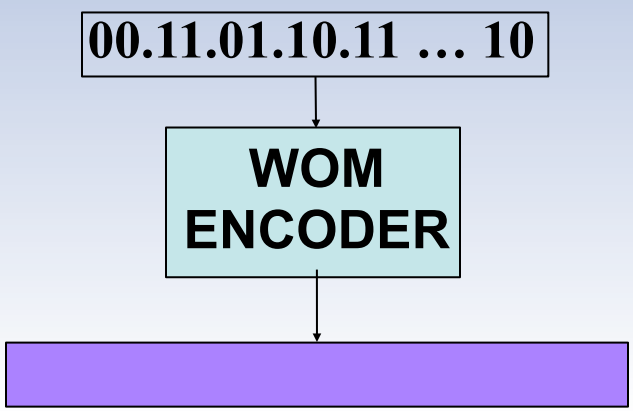

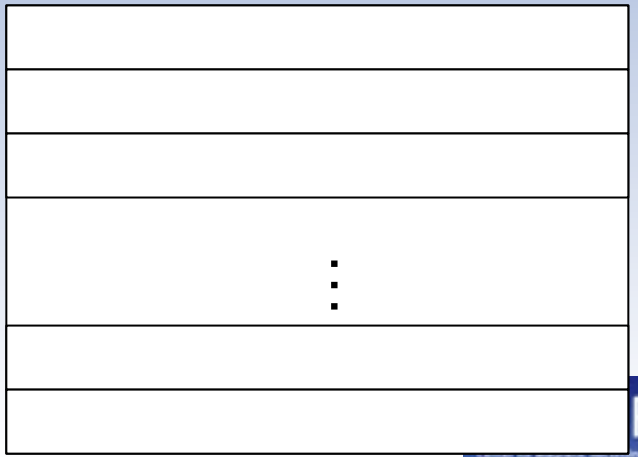

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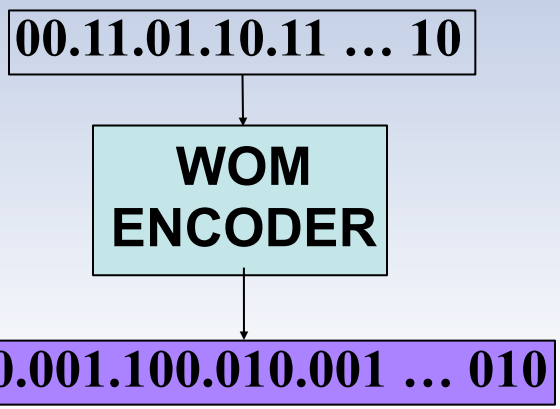

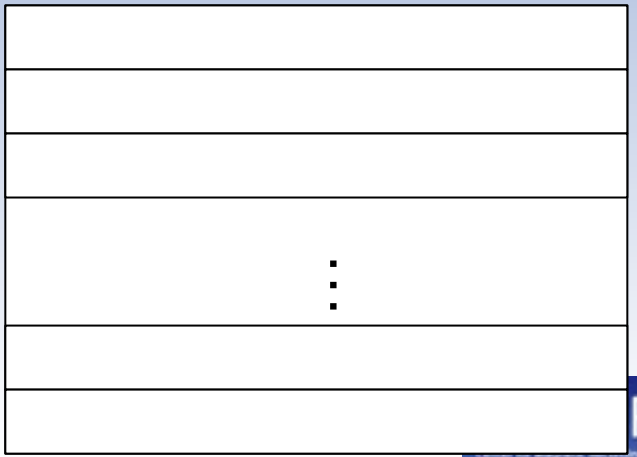

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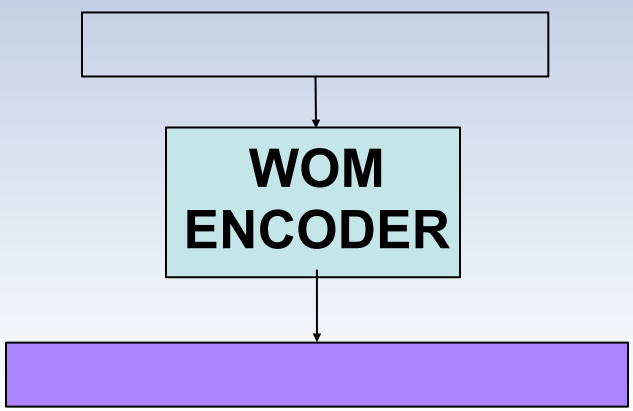

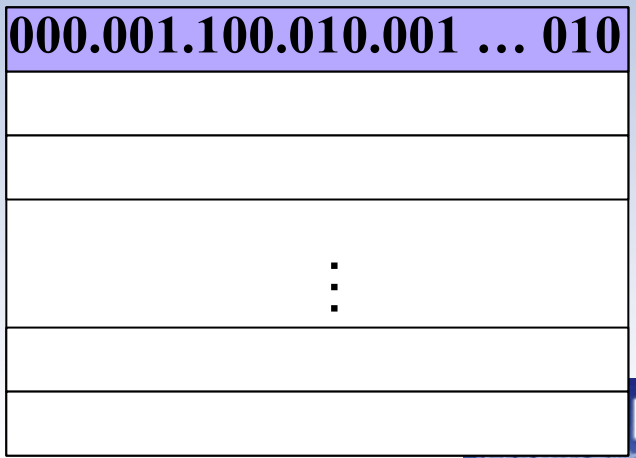

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data	1st write	2nd write
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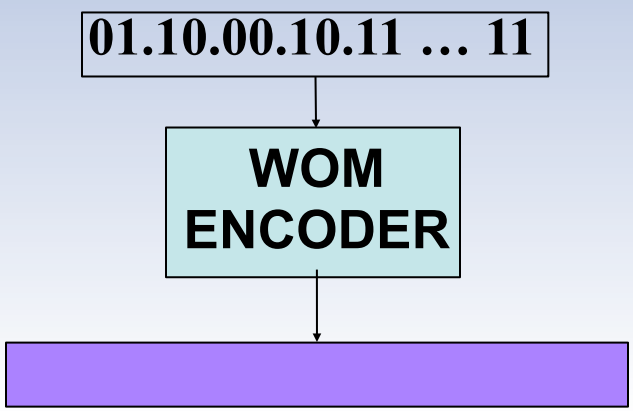
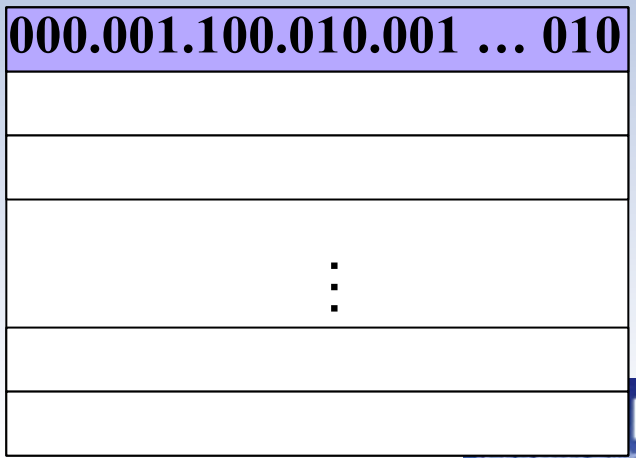
01	100	011
10	010	101
11	001	110

Cells state





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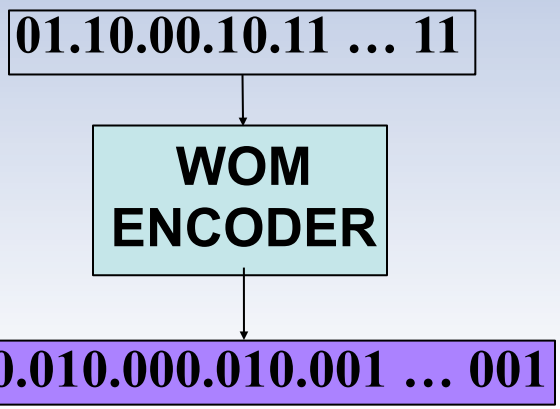

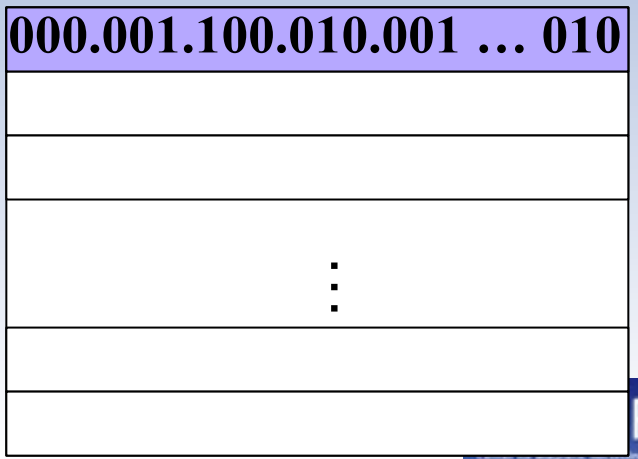

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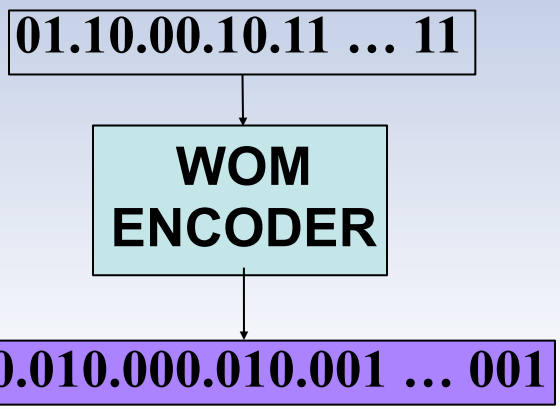

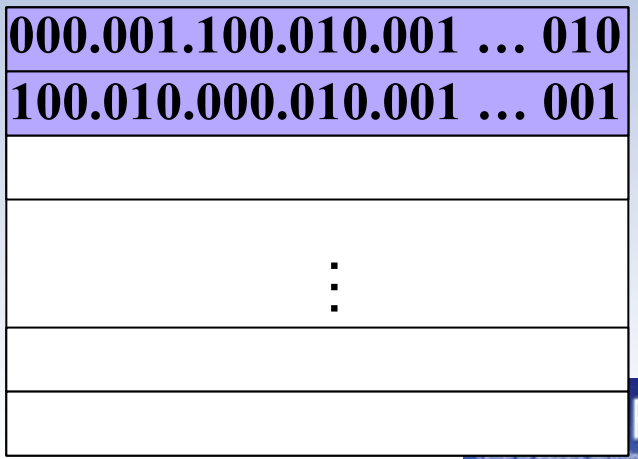

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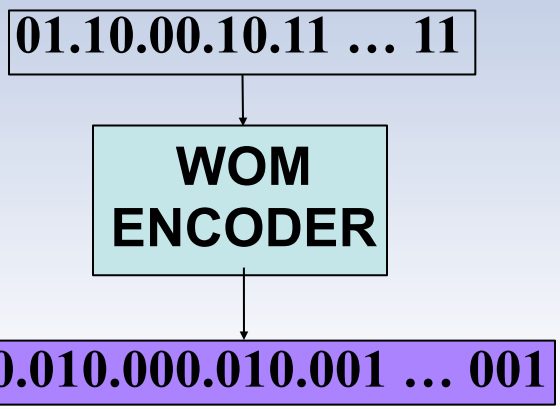

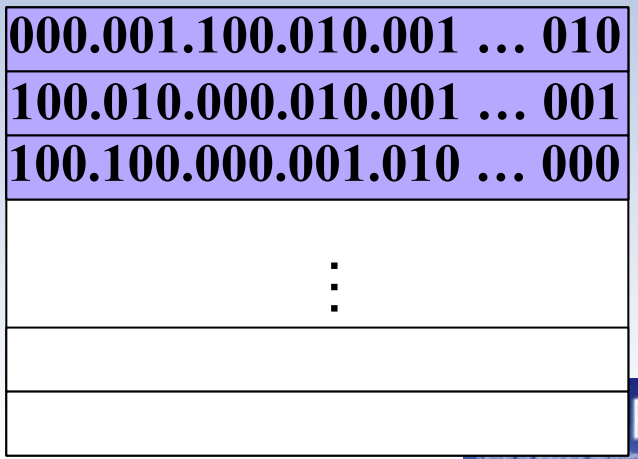

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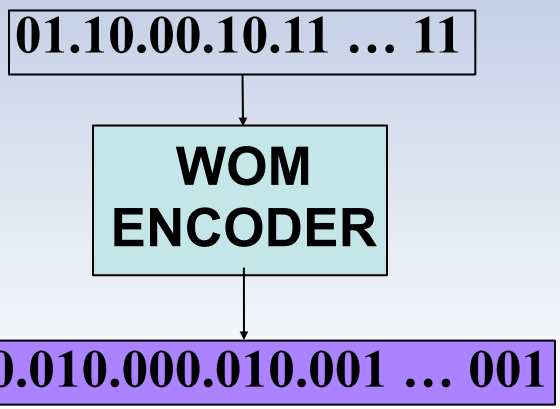

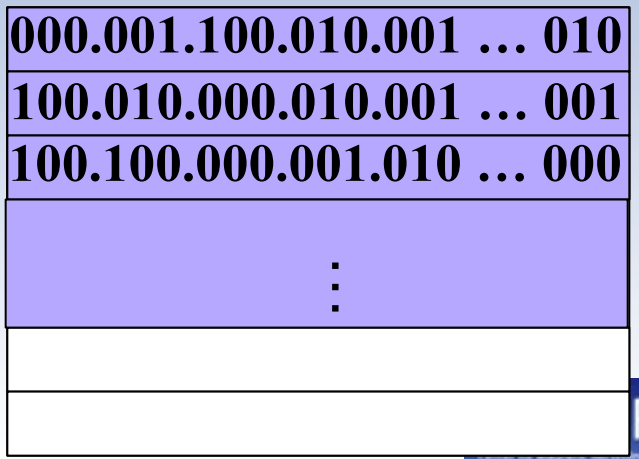

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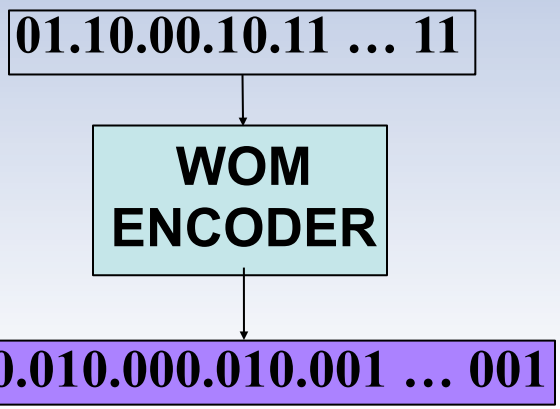

000.001.100.010.001 … 010
100.010.000.010.001 … 001
100.100.000.001.010 … 000
⋮
000.010.001.100.000 … 010

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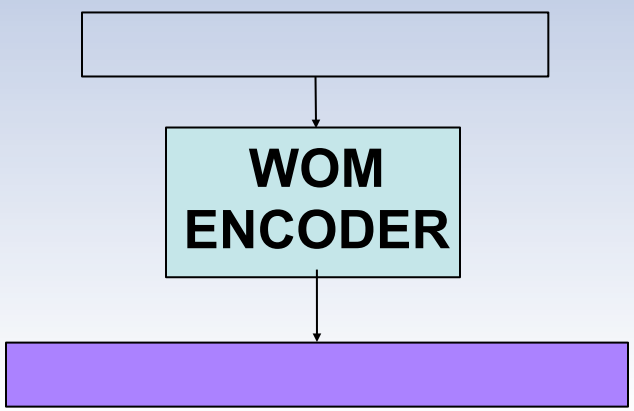

000.001.100.010.001 … 010
100.010.000.010.001 … 001
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⋮
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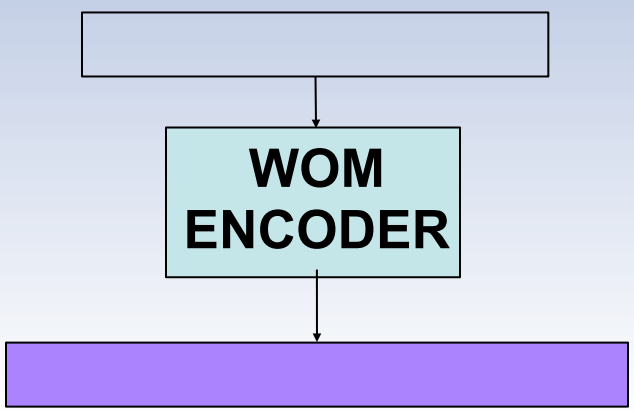

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100.010.000.010.001 … 001
100.100.000.001.010 … 000
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000.010.001.100.000 … 010
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INVALID

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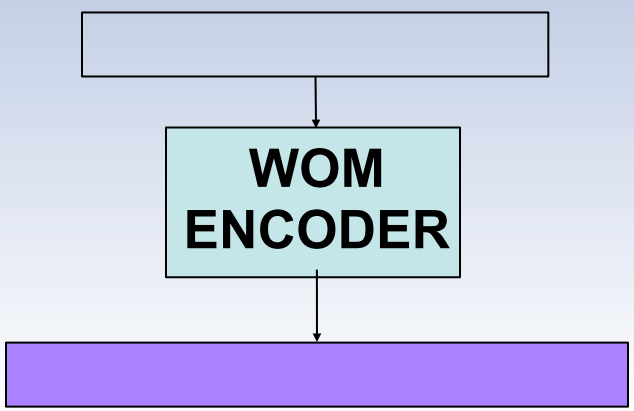

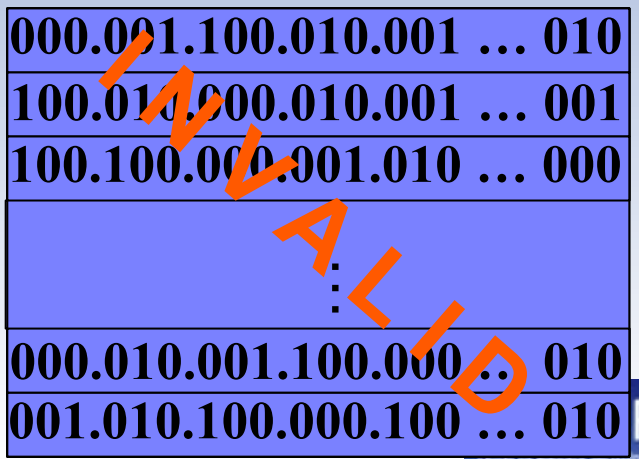

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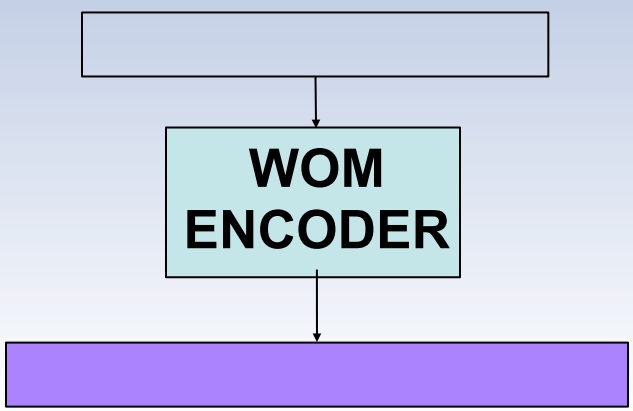

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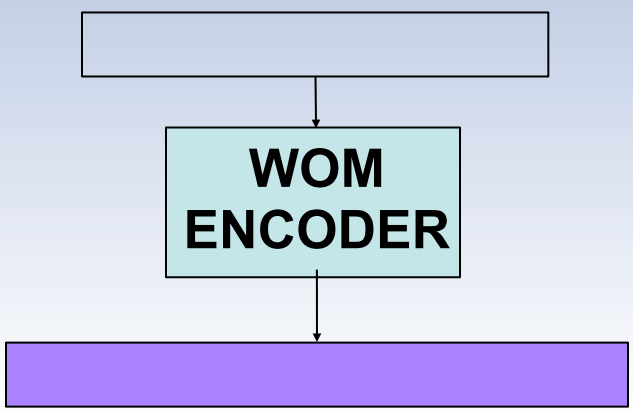

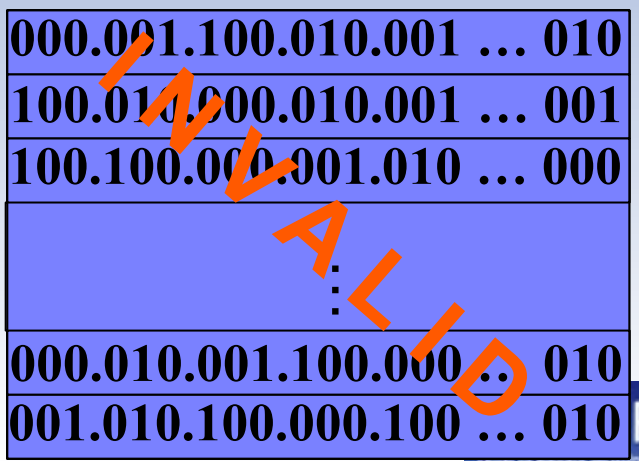

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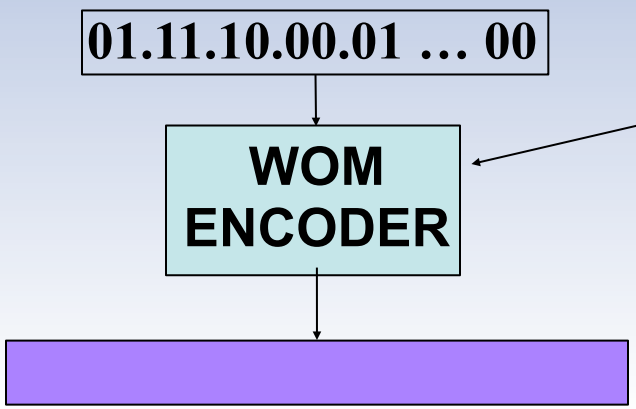

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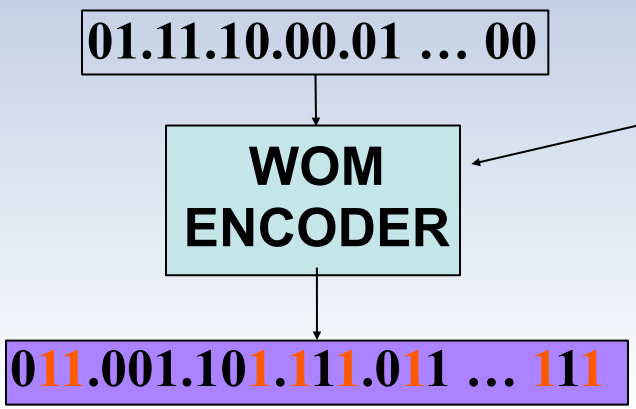

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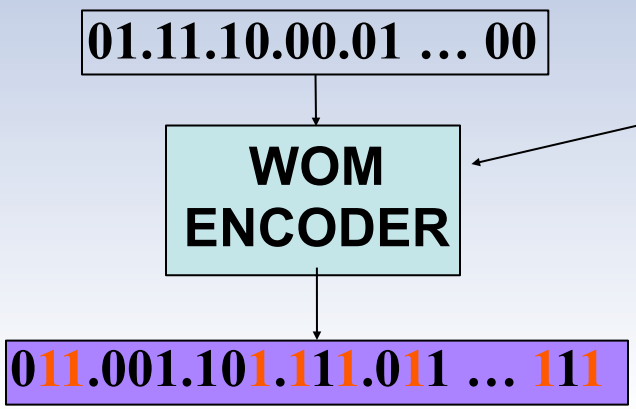

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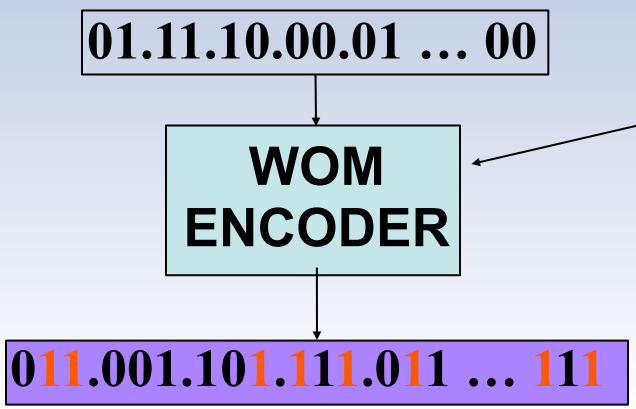

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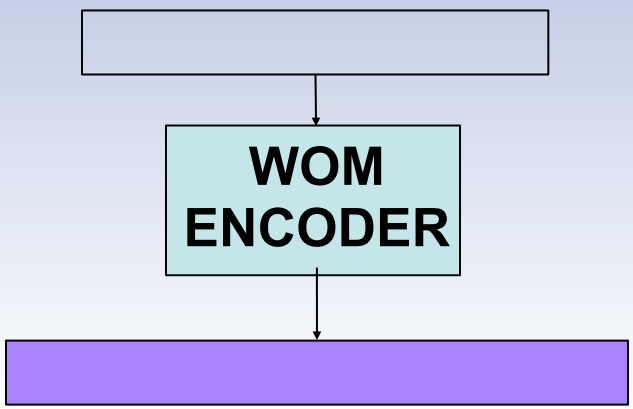

011.001.101.111.011 … 111
100.010.000.010.001 … 001
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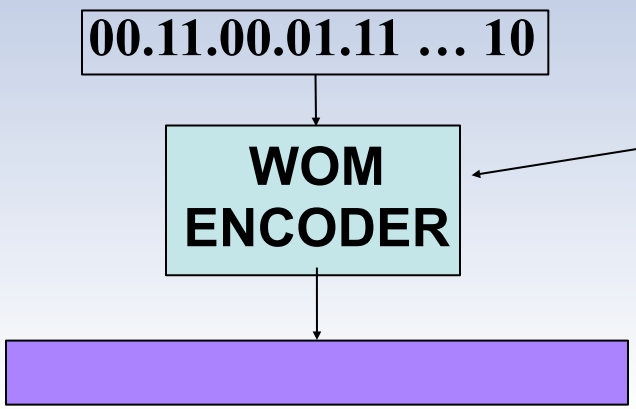

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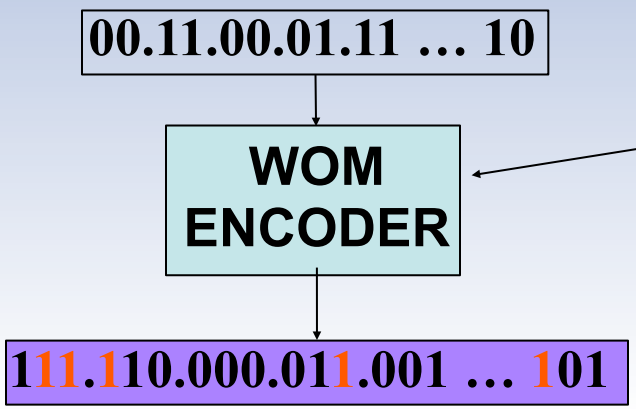

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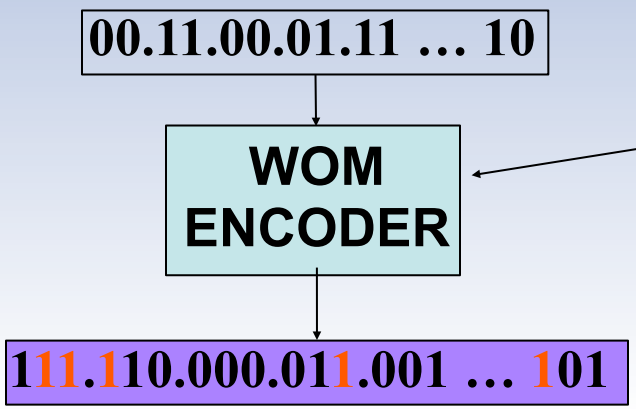

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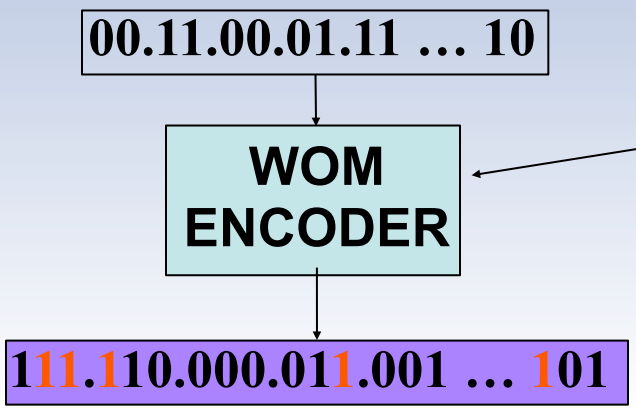

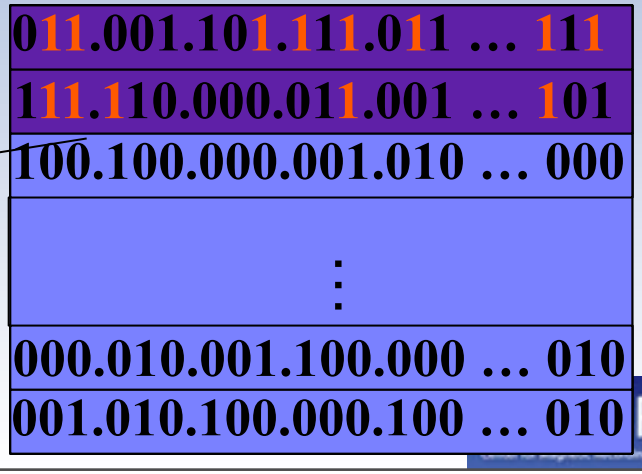

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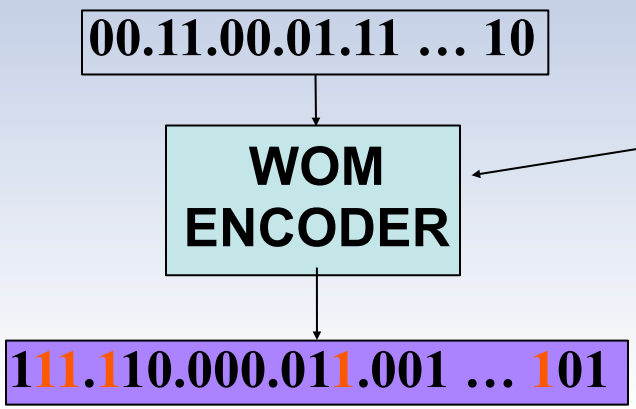

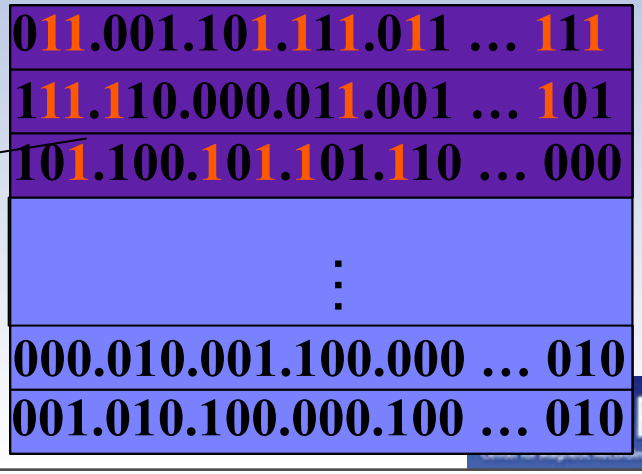

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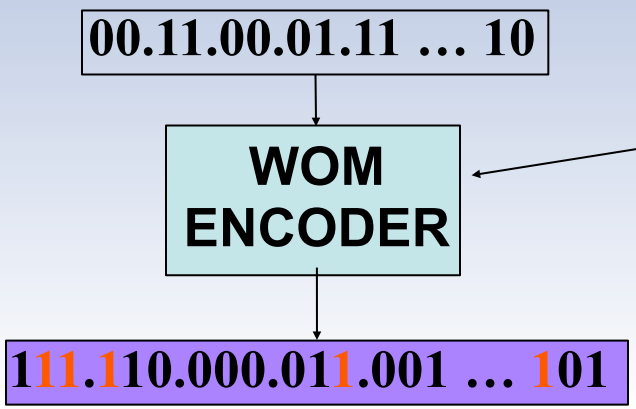

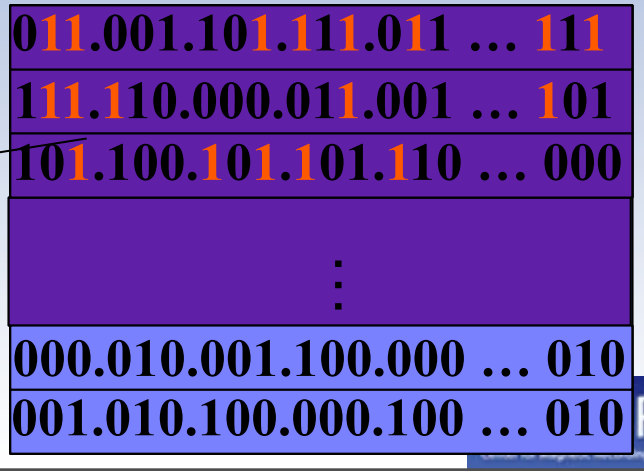

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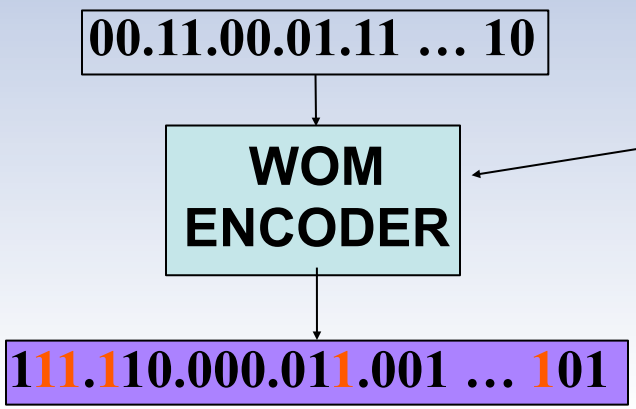

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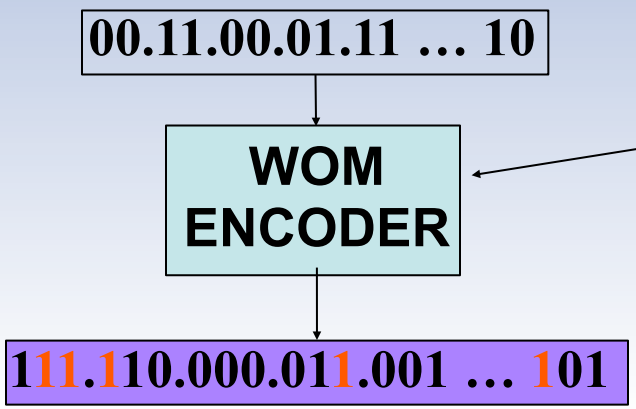

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Advantages:

• The number of bits written per cell is **4/3**

• Possible to write twice before a physical erasure

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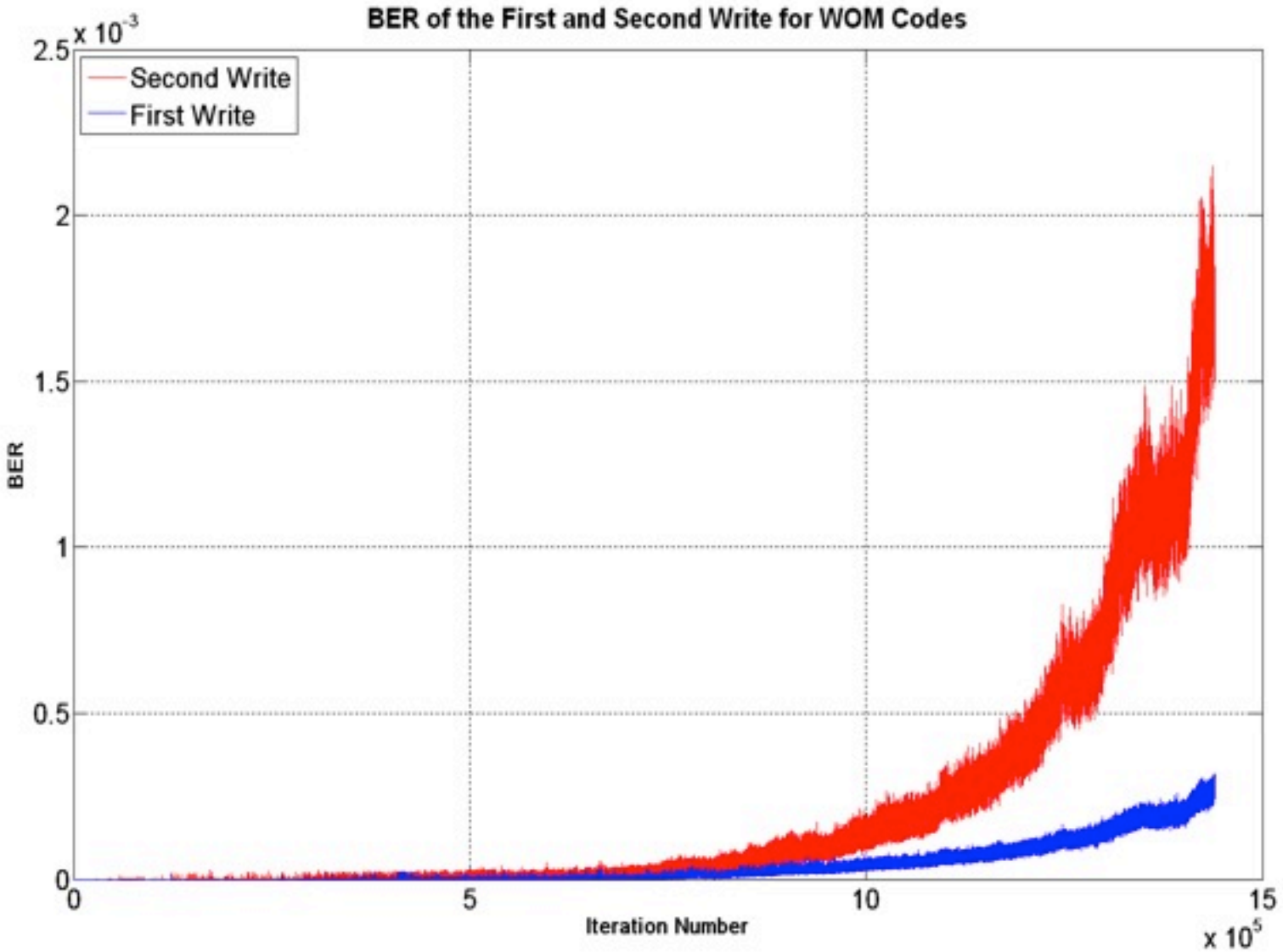
BER for the First and Second Writes



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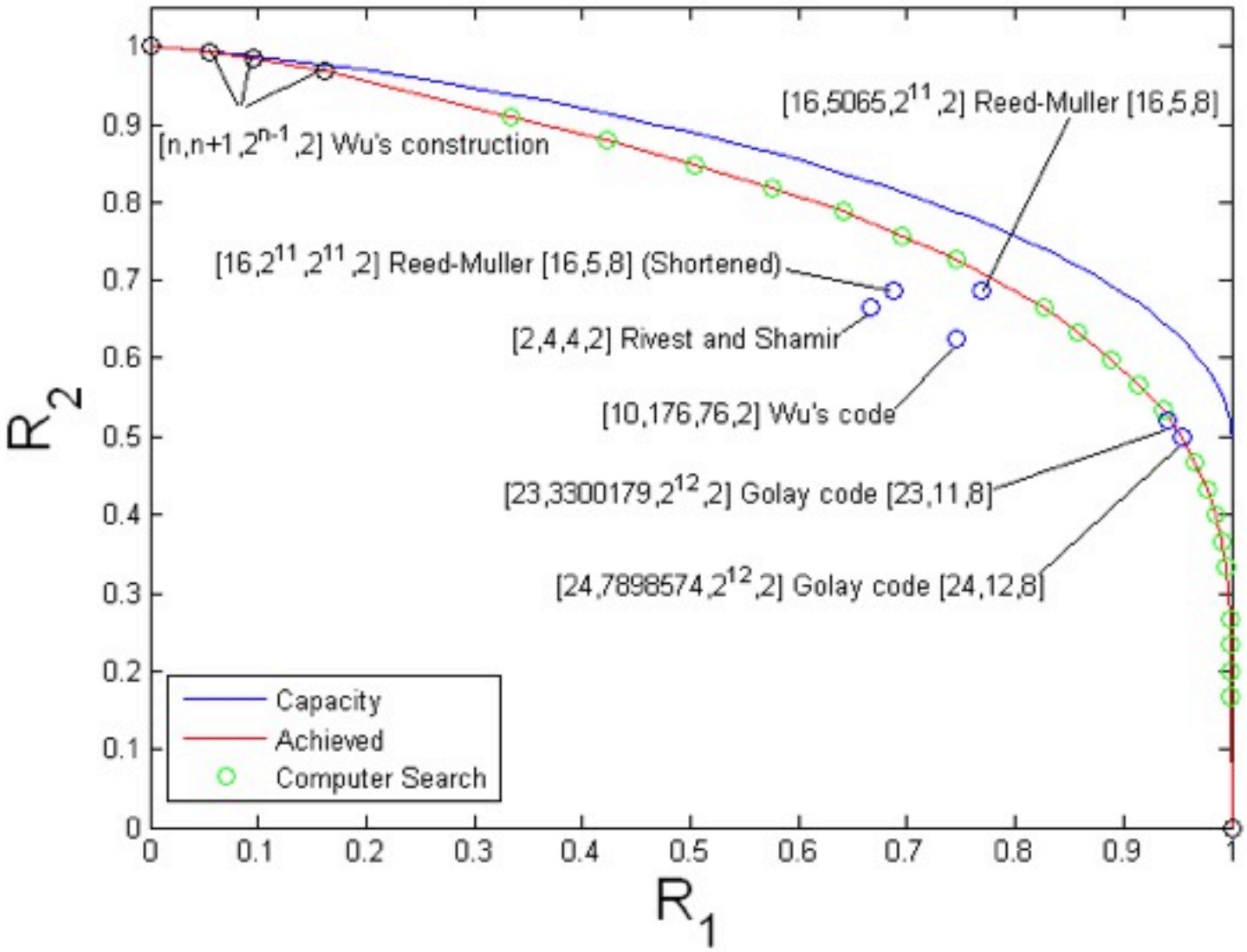
  - By computer search we found rate $(0.7273, 0.7273)$, $R = 1.4546$

WOM Capacity and Achievable Rates



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