Error Control Coding for MLC Flash Memories

Ying Y. Tai, Ph.D.

Cadence Design Systems, Inc.
ytai@cadence.com
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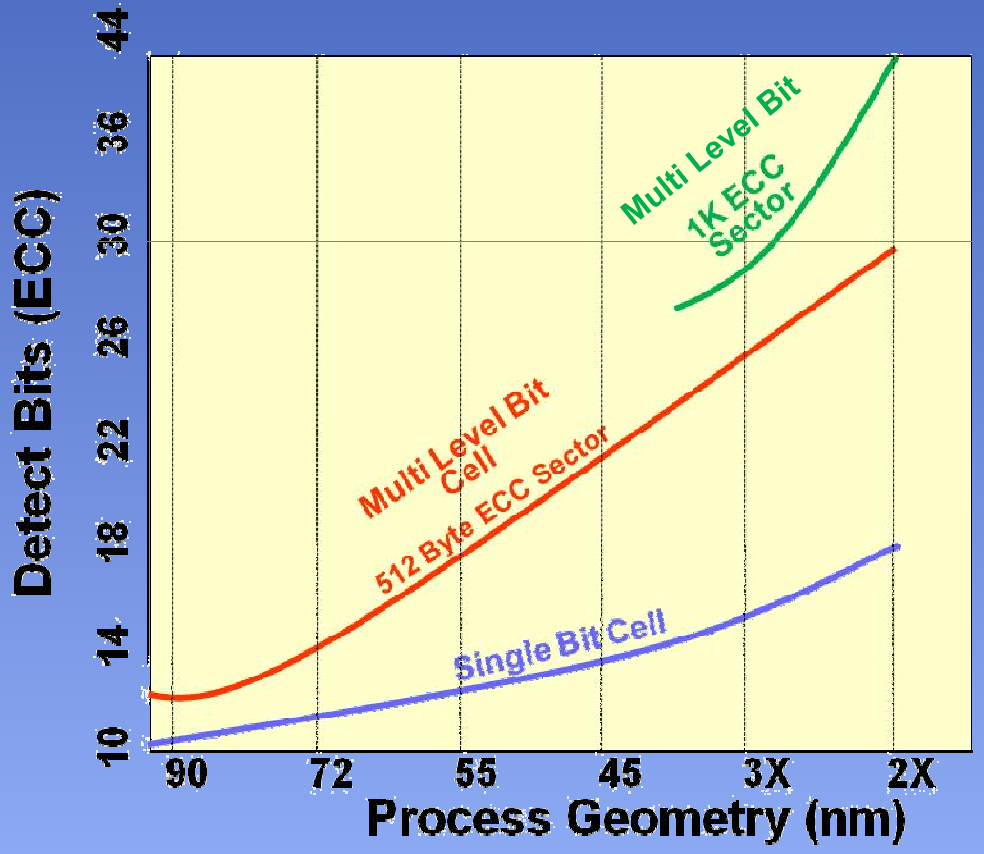
Outline

- The Challenges on Error Control Coding (ECC) for MLC Flash Memories
- Performance Measures on ECC
- Low-Density Parity-Check (LDPC) Codes Overview
- Performance of LDPC Codes for MLC Flash Memories
- Conclusions

Challenges on ECC for MLC Flash Memories

- MLC Flash Memory:
  - Multiple bits are stored in each memory cell
  - Storage density increases
  - Process geometry downscale
  - Worse reliability



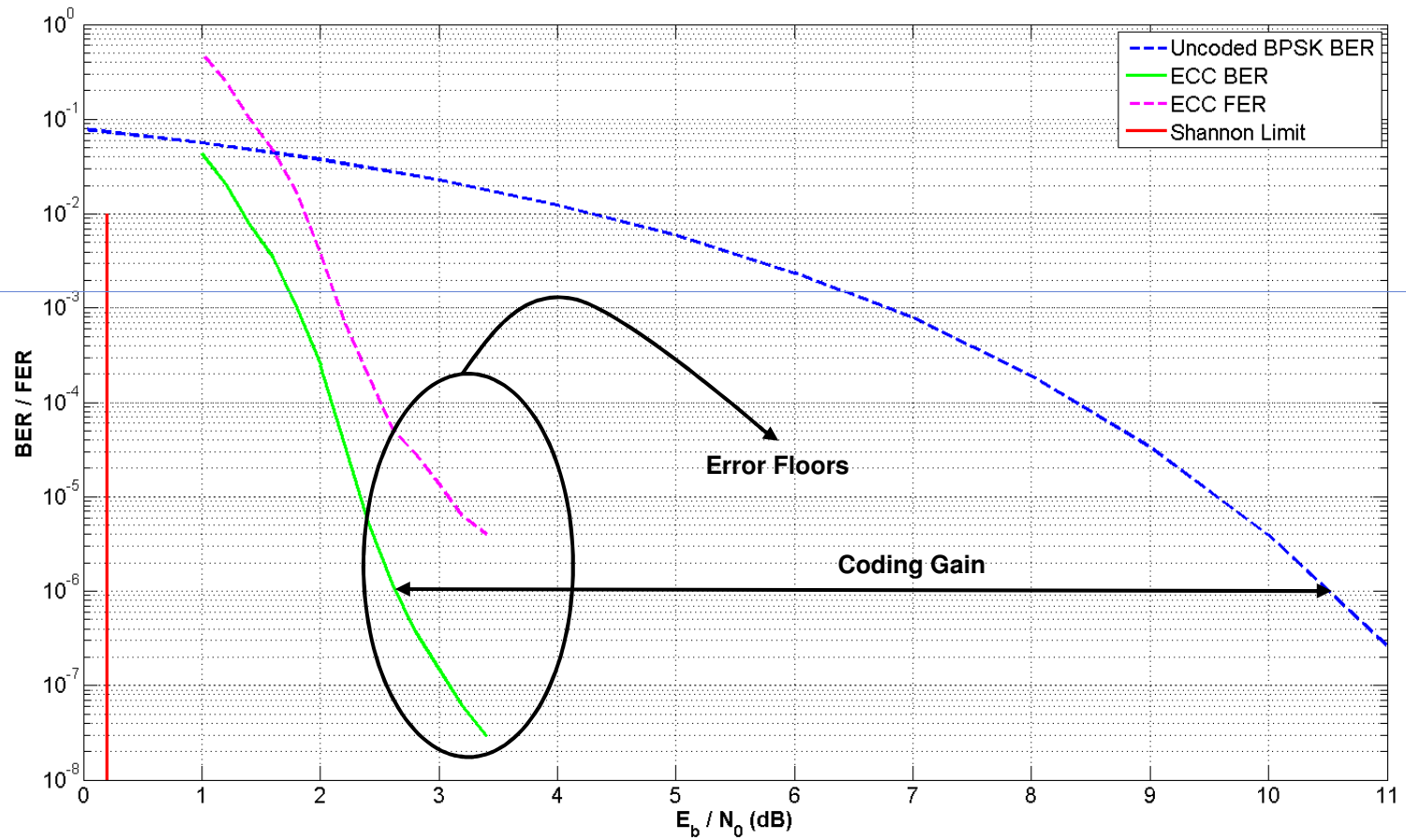
ECC for Flash Memories

- ECC Trend for Flash Memories:
  - Bit error rate (BER) requirement: $10^{-13} - 10^{-16}$
  - Hamming codes for SLC flash memory
  - BCH codes for MLC flash memory (codeword length increases from 512 to 1K to 2K bytes)
  - What is the next?
    - Reed-Solomon (RS) codes?
    - Low-Density Parity-Check (LDPC) codes?

Performance Measures on ECC

- Error Probability:
  - Bit error rate (BER)
  - Symbol error rate (SER)
  - Word (frame or block) error rate
  - Error floor
- Coding Gain
- Shannon Theoretical Limit

Performance Measures on ECC



LDPC Codes Overview

- A class of channel capacity approaching codes
- Employed by various applications:
  - IEEE 802.3 10G BASE-T Ethernet
  - Digital Video Broadcasting – DVB-S2
  - IEEE 802.16e WiMAX
  - Long Term Evolution (LTE)
  - Hard Disk Drive
  - NASA LandSat Data Continuation Mission
  - China Digital TV Standard – DTMB

What is LDPC Code?

- The null space of a sparse parity-check matrix H over GF(q), i.e. $\mathbf{c} \bullet \mathbf{H}^T = \mathbf{0}$
- Categories of LDPC codes:
  - Random LDPC codes
  - Structured LDPC codes
- Key properties on the performance:
  - Girth and cycle distribution
  - Degree distribution
  - Minimum distance
  - Trapping set structure

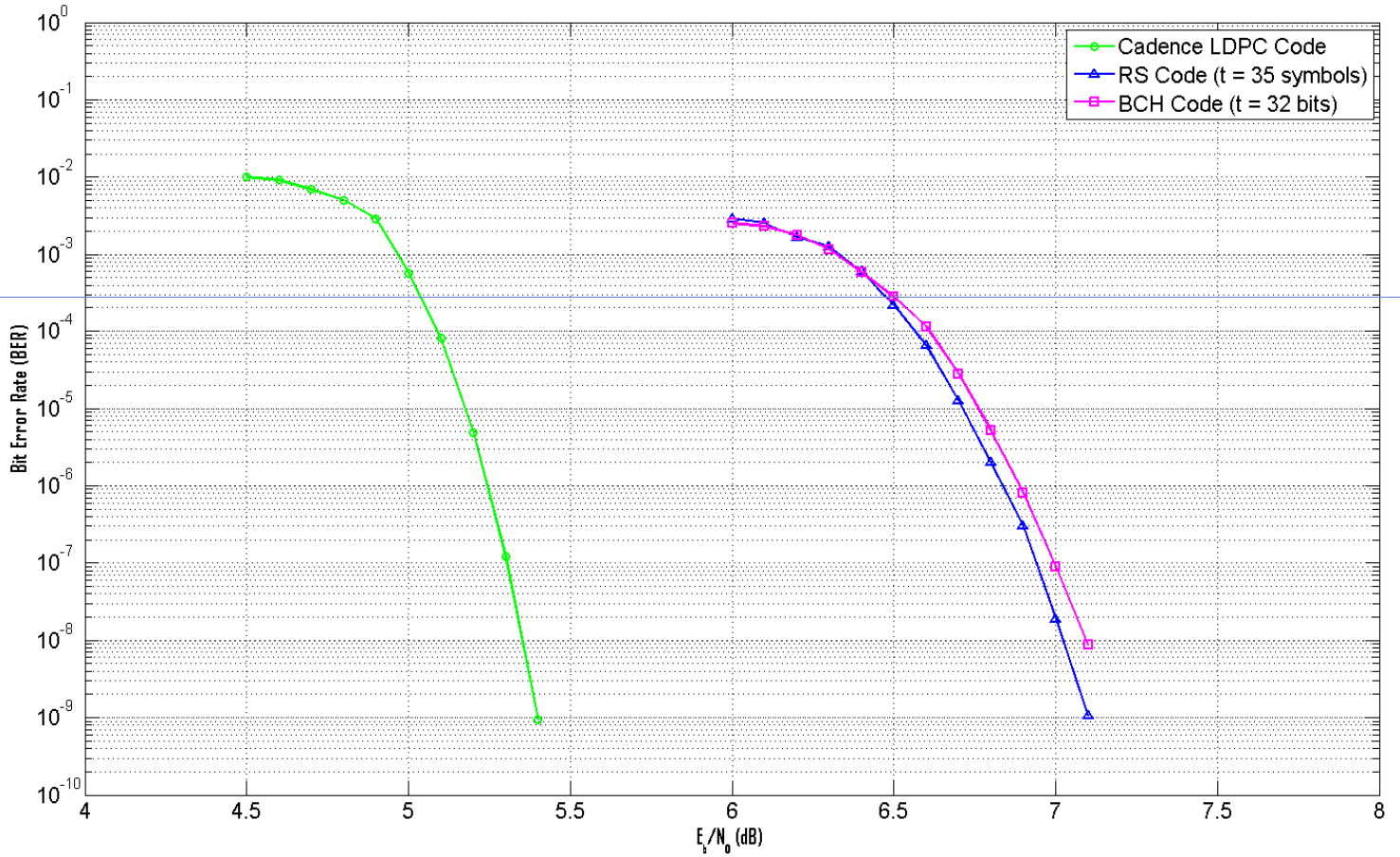
Quasi-Cyclic (QC) LDPC Codes

- The null space of an array of sparse circulants
- Why QC-LDPC codes?
  - Reduced complexity for encoding and decoding on hardware implementation
  - Well-designed QC LDPC codes perform very well
    - Good BER
    - Large coding gain
    - Low error floor
    - Fast decoding convergence rate
  - Systematic encoder

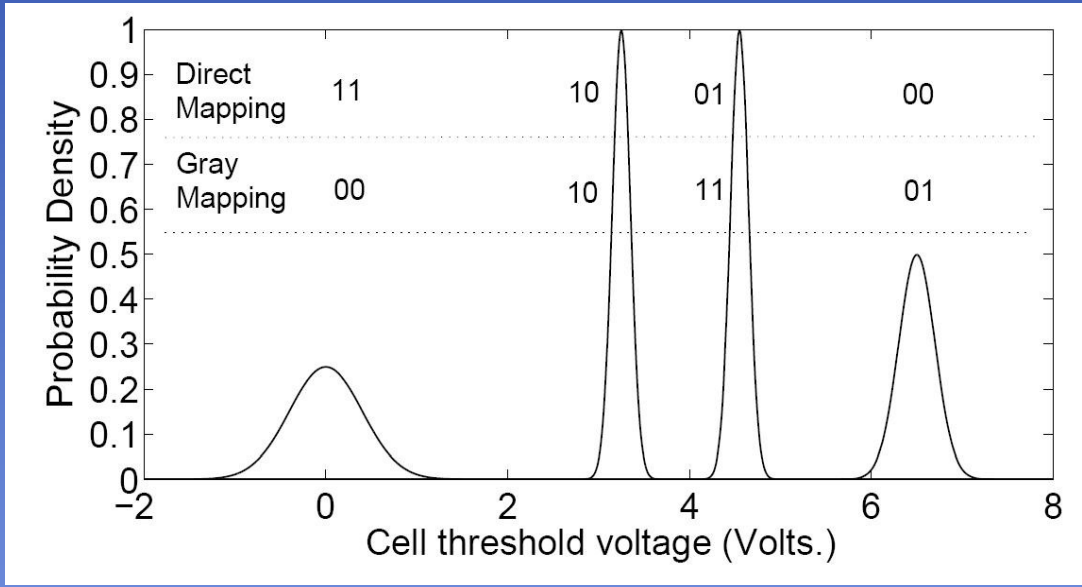
Example: Cadence/Denali LDPC on AWGN Channel

	Comparison	Cadence/Denali LDPC Code	RS Code	BCH Code
Code Parameters	**Data Size**	2K Bytes	2K Bytes	2K Bytes
	Overhead Size	< 5 %	< 5 %	< 5 %
	Error Correction Capability (t)	N/A	35 Symbols	32 Bits
	Type	Quasi-Cyclic	Cyclic	Cyclic
	Encoder Format	Systematic	Systematic	Systematic
Setup	**Simulation (Emulation)**	C & FPGA	C	C
	Decoding Type	Iterative Belief Propagation	Algebraic Decoding	Algebraic Decoding
	Transmission	BPSK	BPSK	BPSK
	Channel	AWGN	AWGN	AWGN

Example: Cadence/Denali LDPC on AWGN Channel

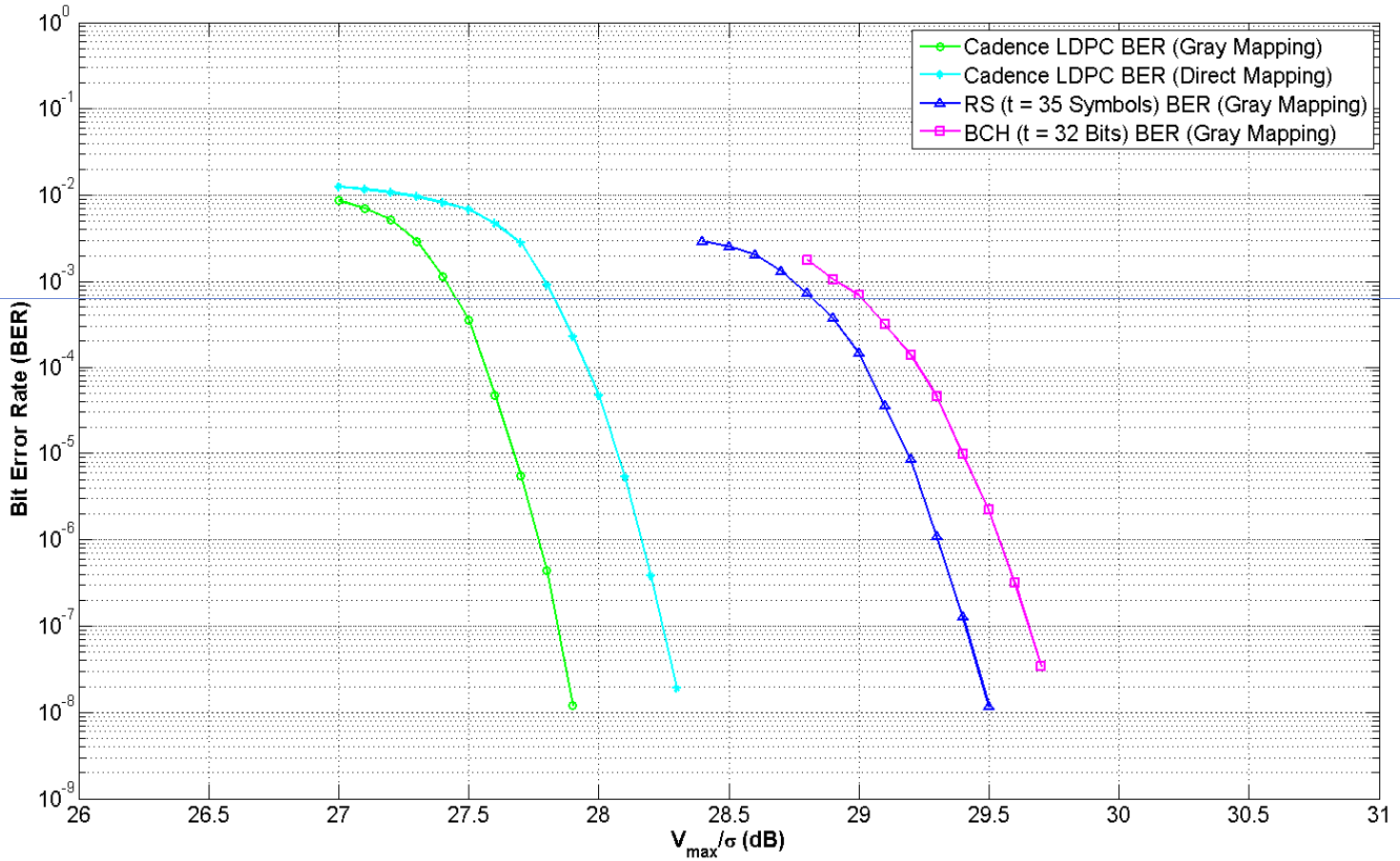


MLC Flash Memories

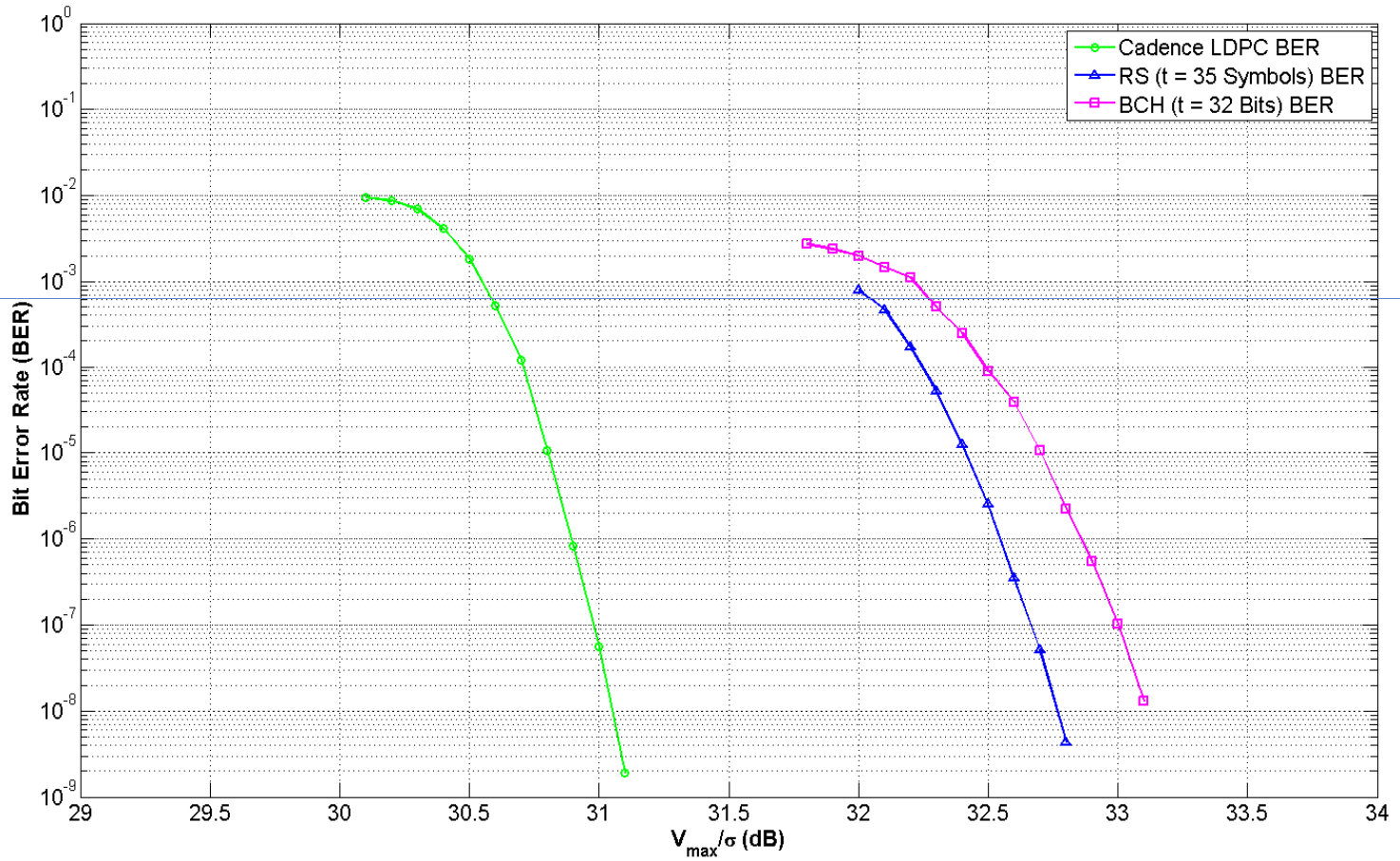


Level	0	1	2	3
Mean (V)	6.50	4.55	3.25	0.00
Deviation (V)	2σ	σ	σ	4σ
Direct Mapping	00	01	10	11
Gray Mapping	01	11	10	00

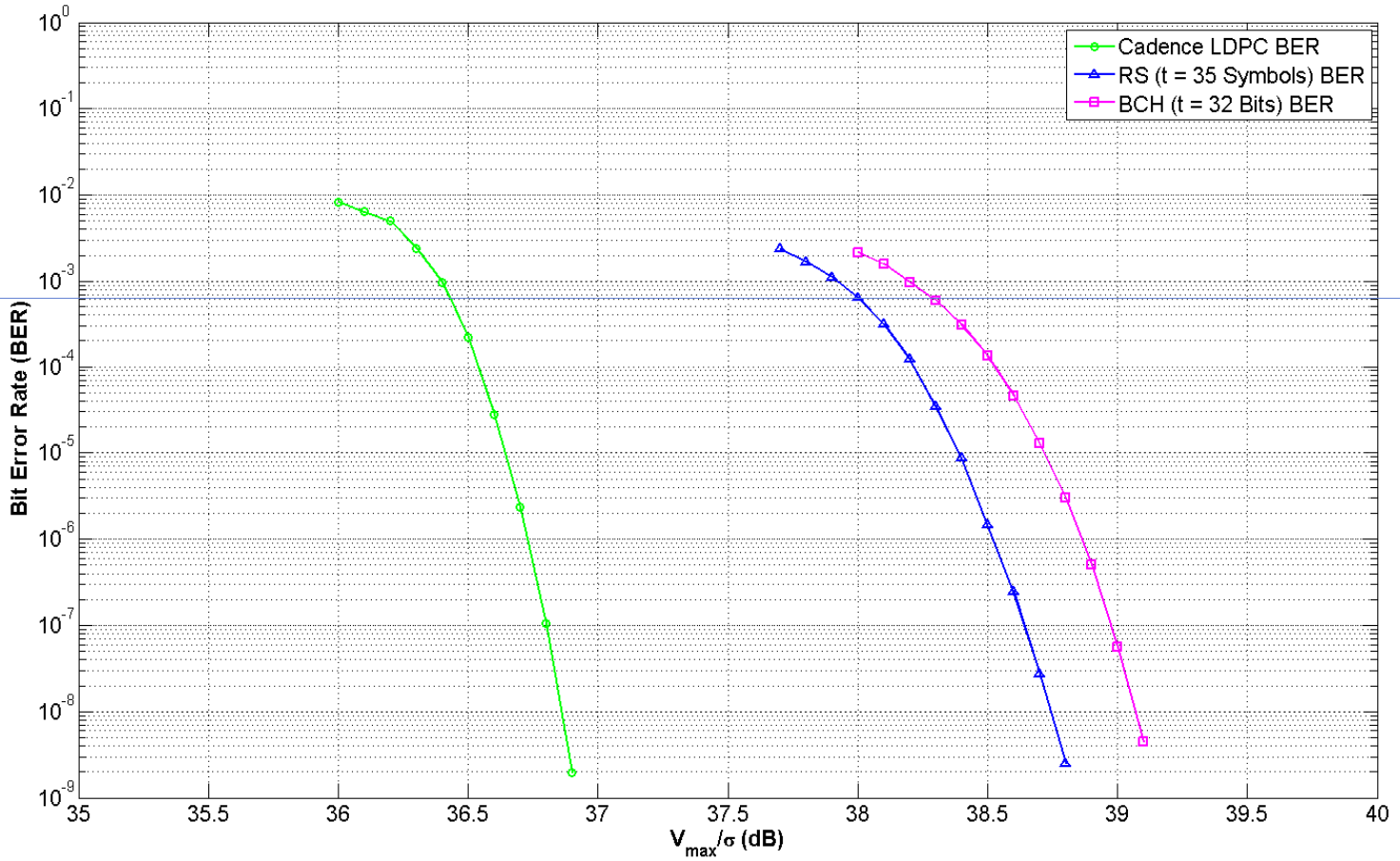
Performance of LDPC on MLC Flash Memories (2 Bits / Cell)



Performance of LDPC on MLC Flash Memories (3 Bits / Cell)



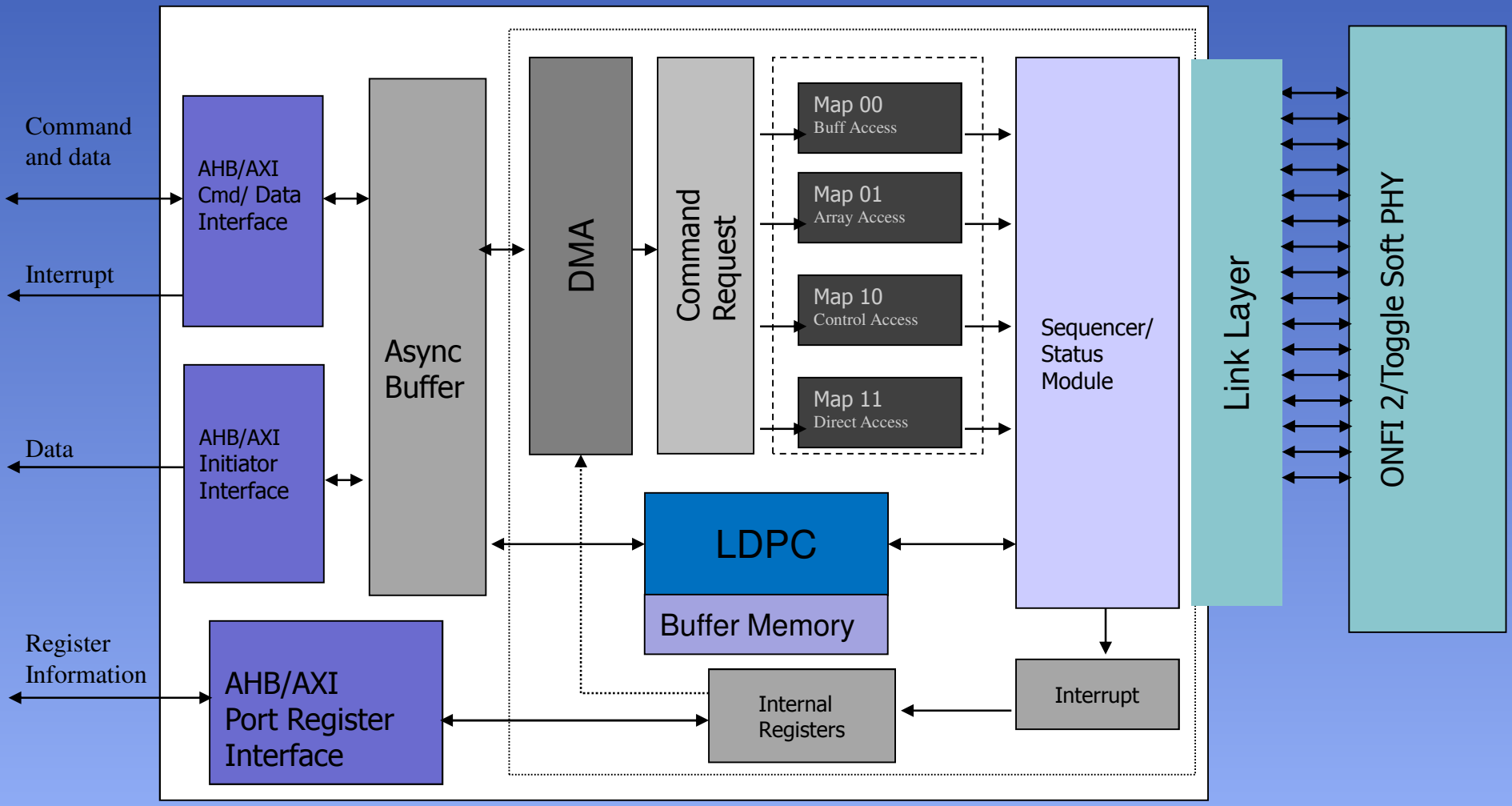
Performance of LDPC on MLC Flash Memories (4 Bits / Cell)



Performance Comparison on MLC Flash Memories

Coding Gain at 10^{-7} of BER			
	2 Bits / Cell	3 Bits / Cell	4 Bits / Cell
LDPC vs RS	1.55 dB	1.67 dB	1.85 dB
LDPC vs BCH	1.80 dB	2.00 dB	2.20 dB
RS vs BCH	0.25 dB	0.33 dB	0.35 dB

Cadence/Denali NAND Controller w PHY Support



Conclusions

- Well-designed LDPC codes have good error performance and low error floor for MLC flash memories.
- QC-LDPC codes have advantages on implementation complexity for encoder and decoder.
- Gray mapping leads to extra coding gain.
- Cadence/Denali NAND Flash IP Solution provides the most advanced ECC technologies for memory systems.

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