Geometry and Operation scheme for Reliable 3-bits NAND

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Intro.

- Physical size reduction
  - reliability degradation
    (IPD scaling, small number of electrons in floating gate)
  - fluctuation in device structure

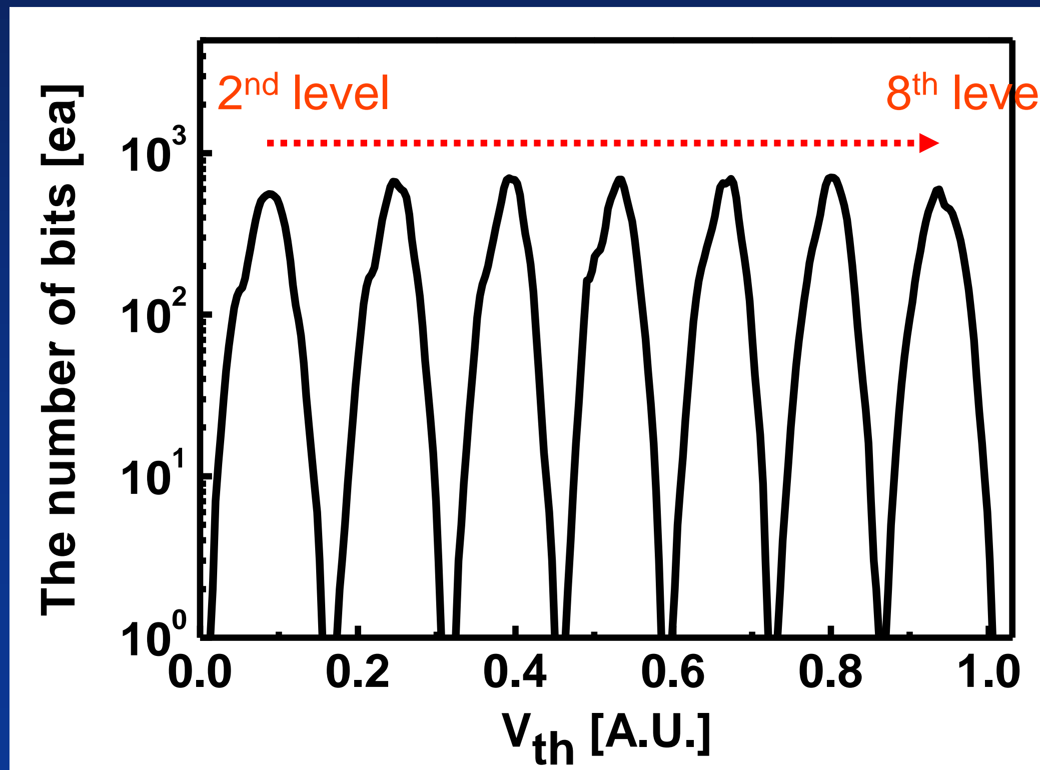
- Multi levels per cell
  - device window narrower
  - Increased pulse numbers for PGM and Read operation

Contents

- Geometry
  - IPD layer, Control gate- Active space, dopant concentration, Floating gate height
- Operation
  - program and read disturb
  - erase pulse

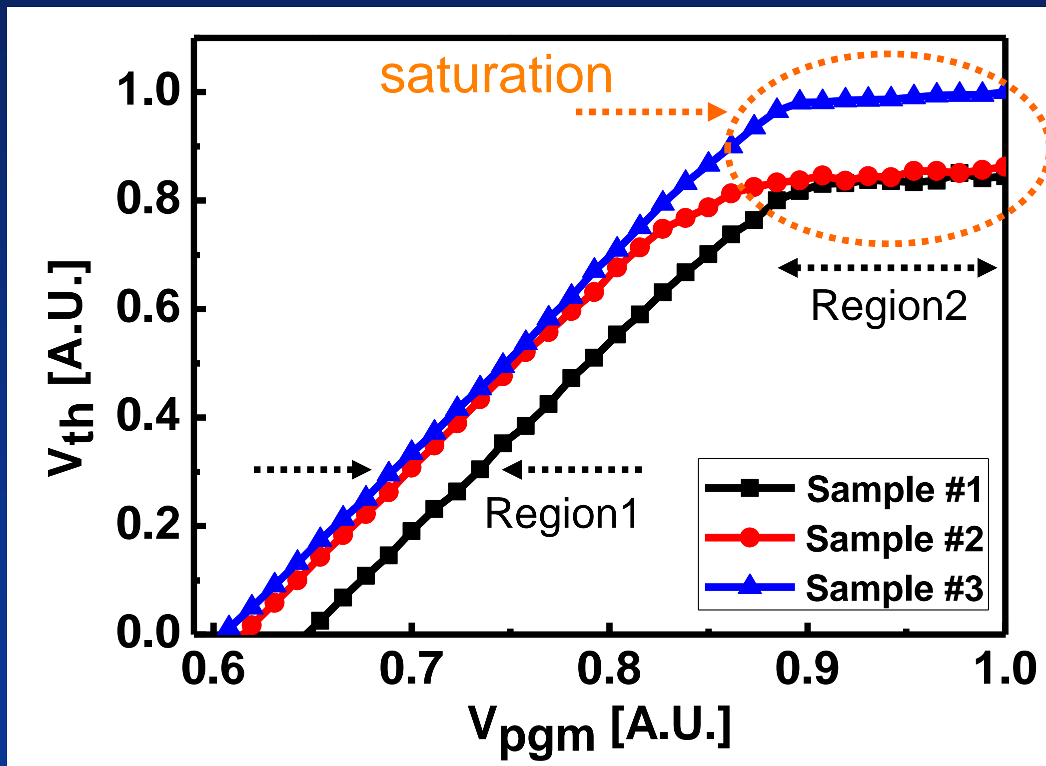
Vth distributions of 3x nm TLC

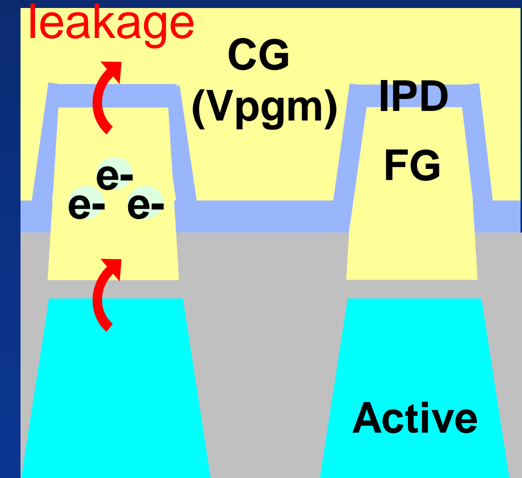
- 7 levels should be positioned above 0V.
  → narrower distribution, higher programmed Vth.



Programmed Vth saturation

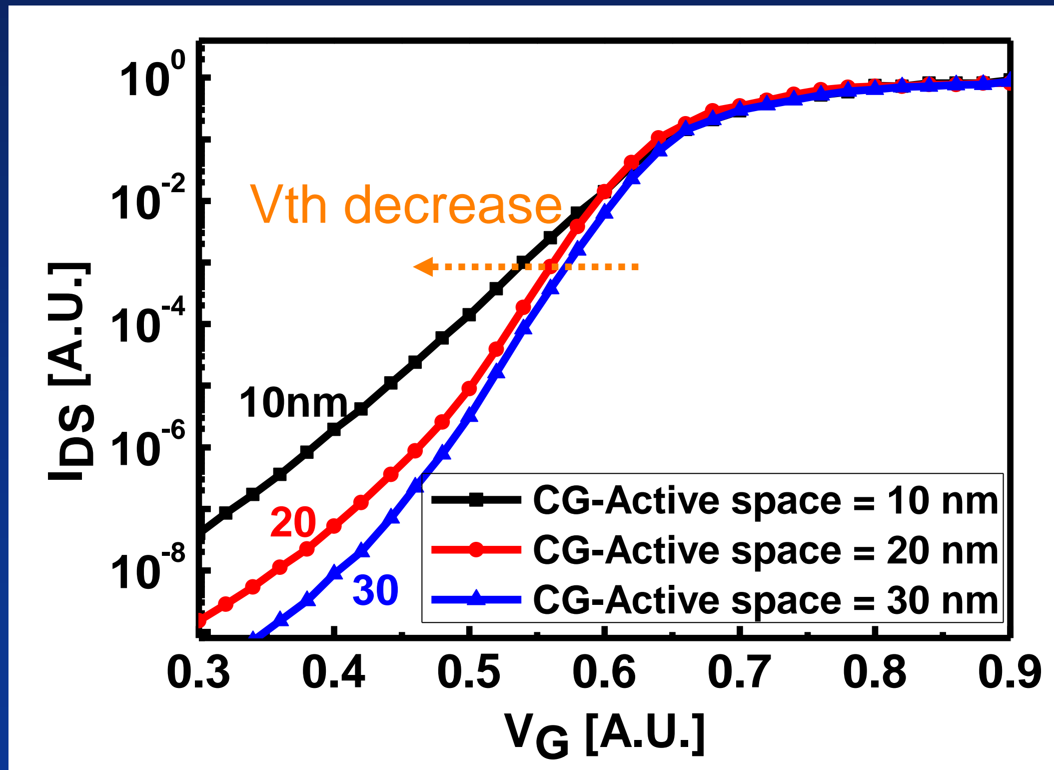
- Hard to reach programmed Vth over 5V.
  - leakage current through IPD during PGM operation.

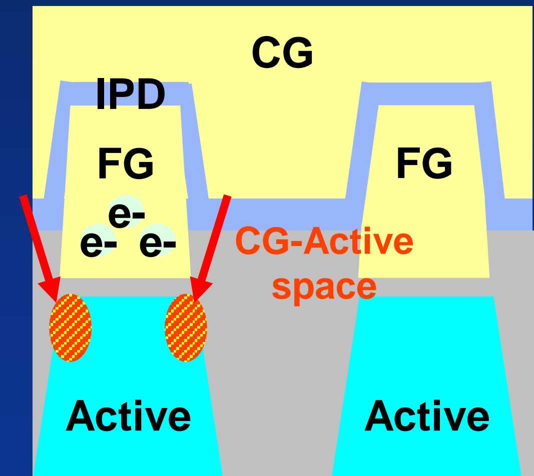




Channel edge direct inversion

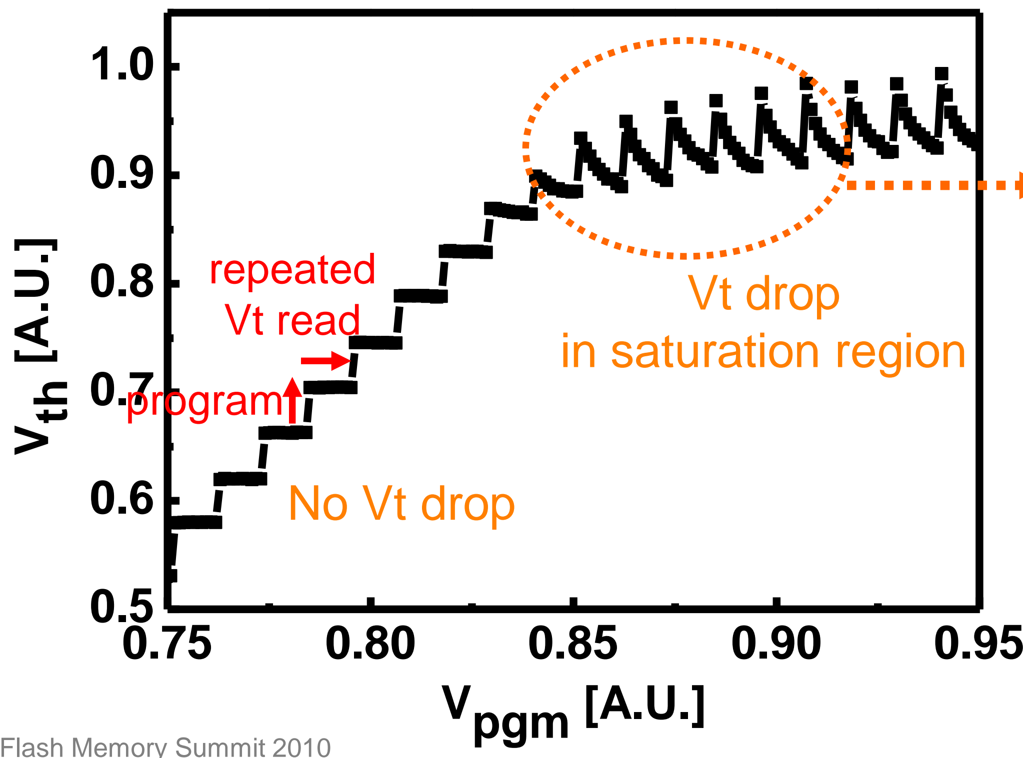
- Channel edge is directly inverted by CG during read.
  → Higher doping concentration in active edge is required.

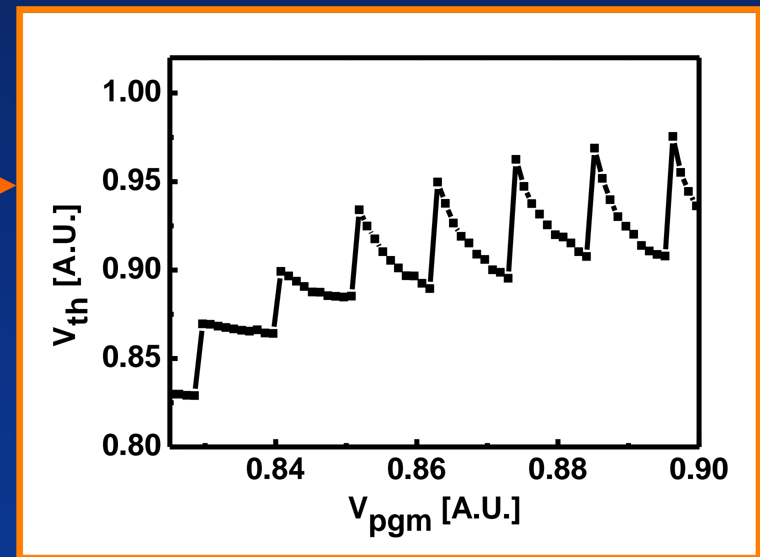




Vt drop at Vt saturation region

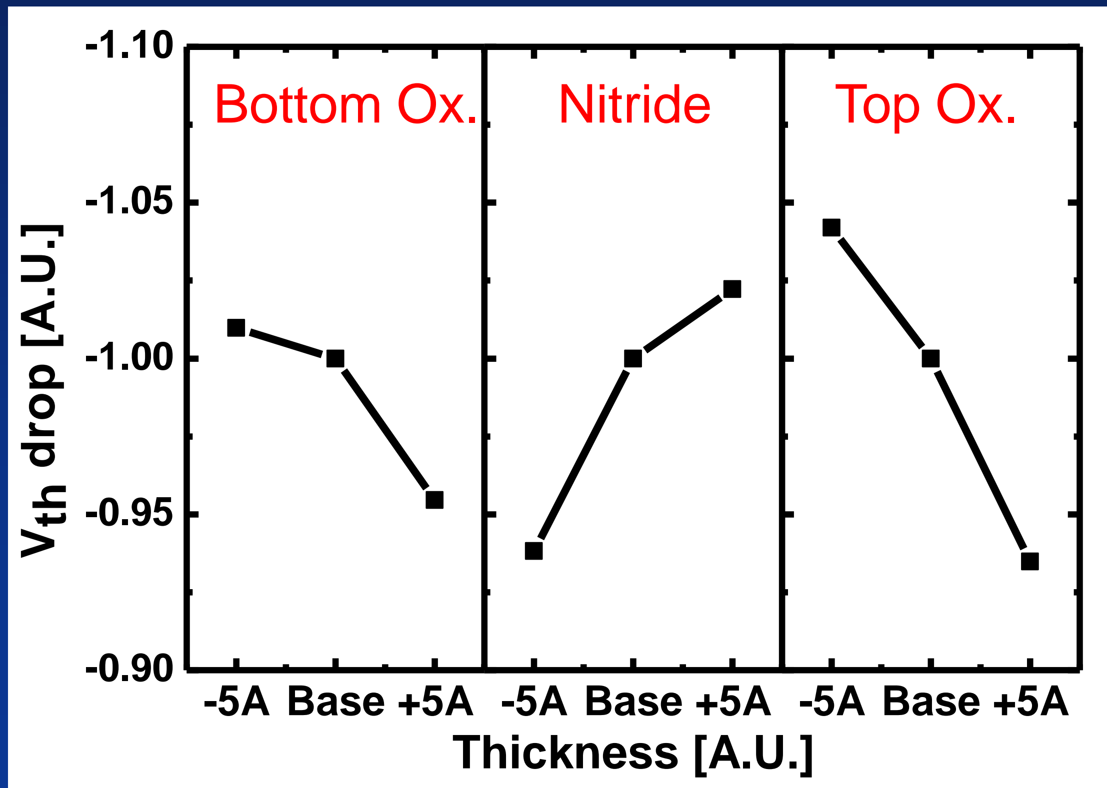
- Vt drop with repeated Vt read at saturation region.
  - charge detrapping from IPD layer.
  - leakage from FG to CG even by small read voltage.





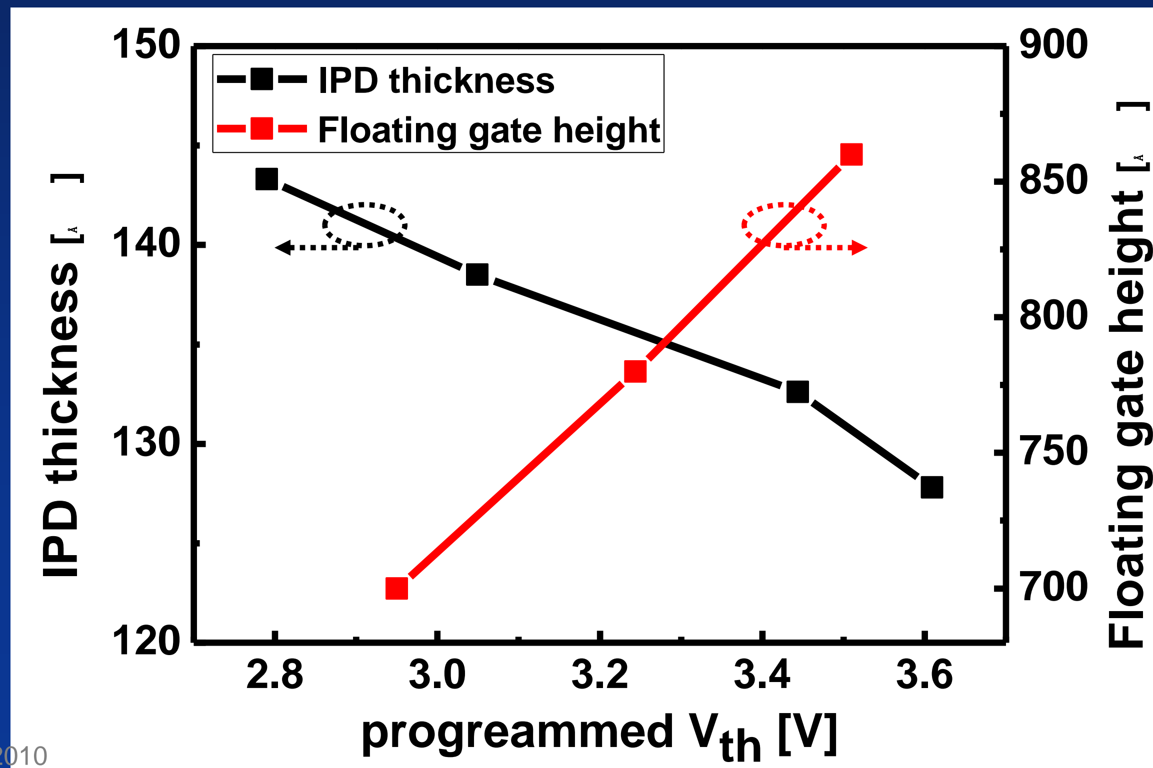
Vt drop dependency on IPD thickness

- Thicker Bottom Ox. and Top Ox. → smaller Vt drop
- Thicker Nitride → larger Vt drop



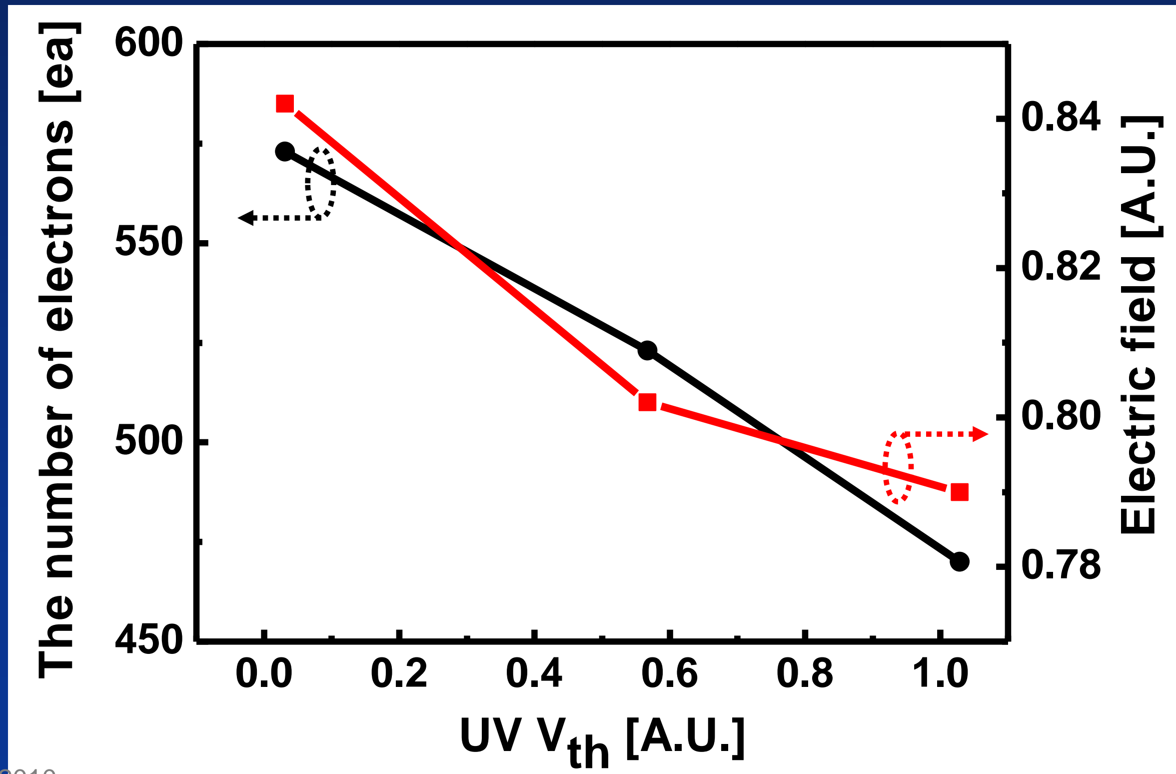
Programmed Vt

- Thicker IPD
  → low CG-channel coupling and programmed Vt.
- High FG height



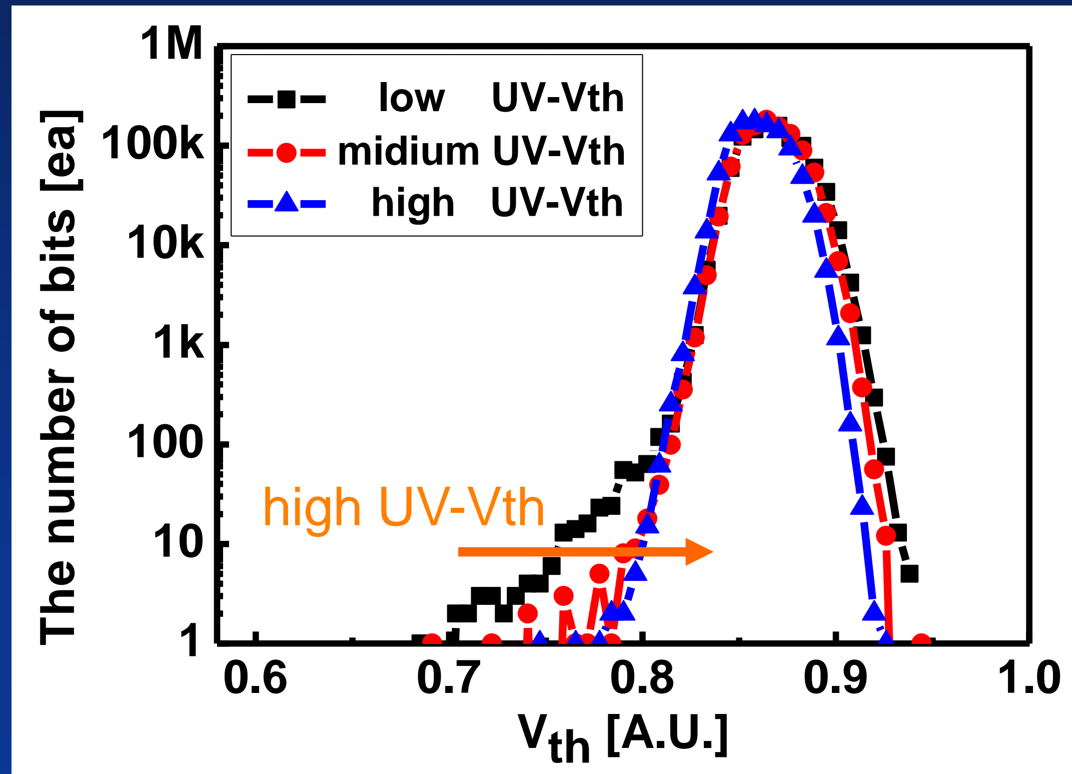
UV-Vth

- UV Vth increase
  → low electric field, small number of electrons in FG



UV-Vth vs. Retention

- Retention characteristic is improved in higher UV-Vth structure.



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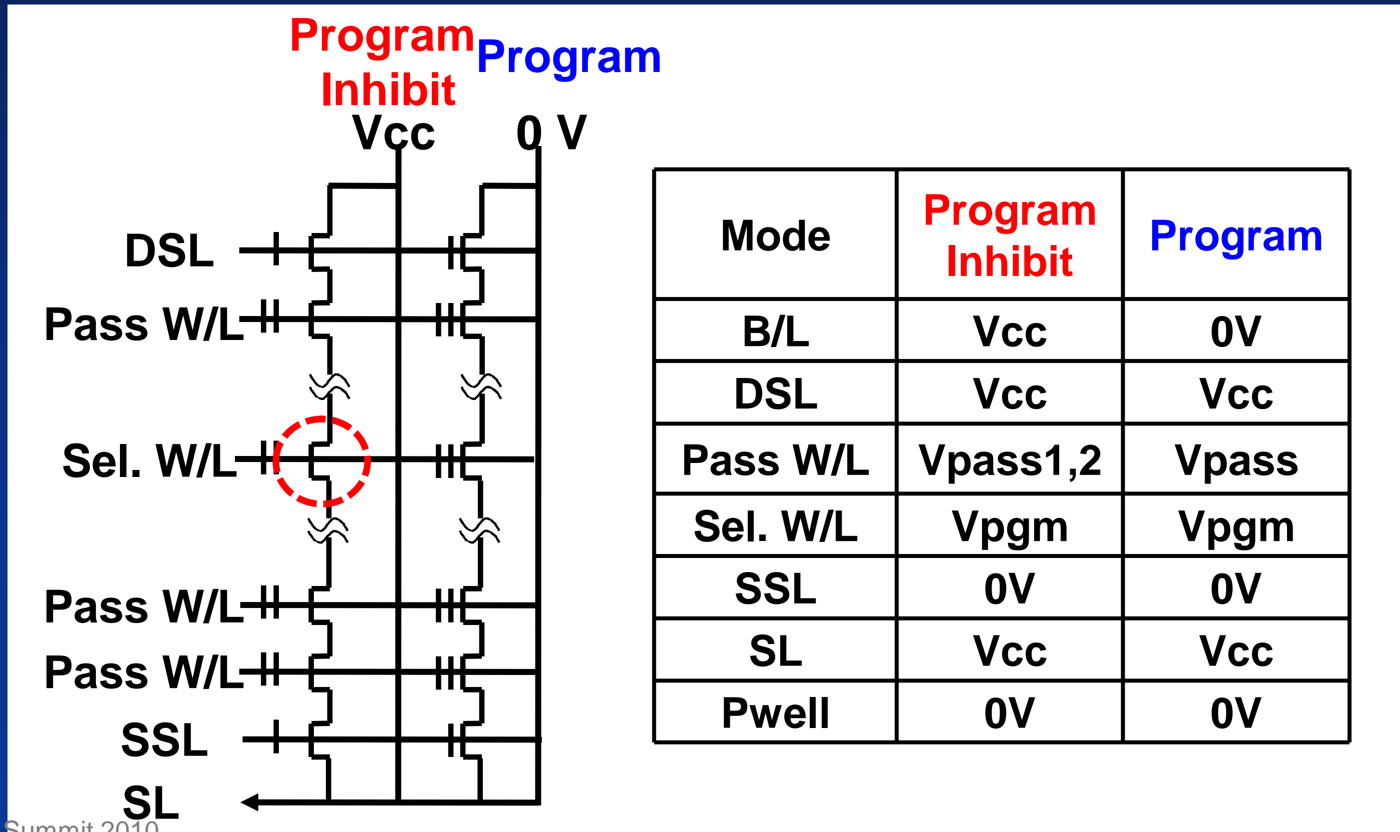
Contents

- Geometry
  - IPD layer, Control gate- Active space, dopant concentration, Floating gate height
- Operation
  - PGM and read disturb
  - erase pulse

Program disturb

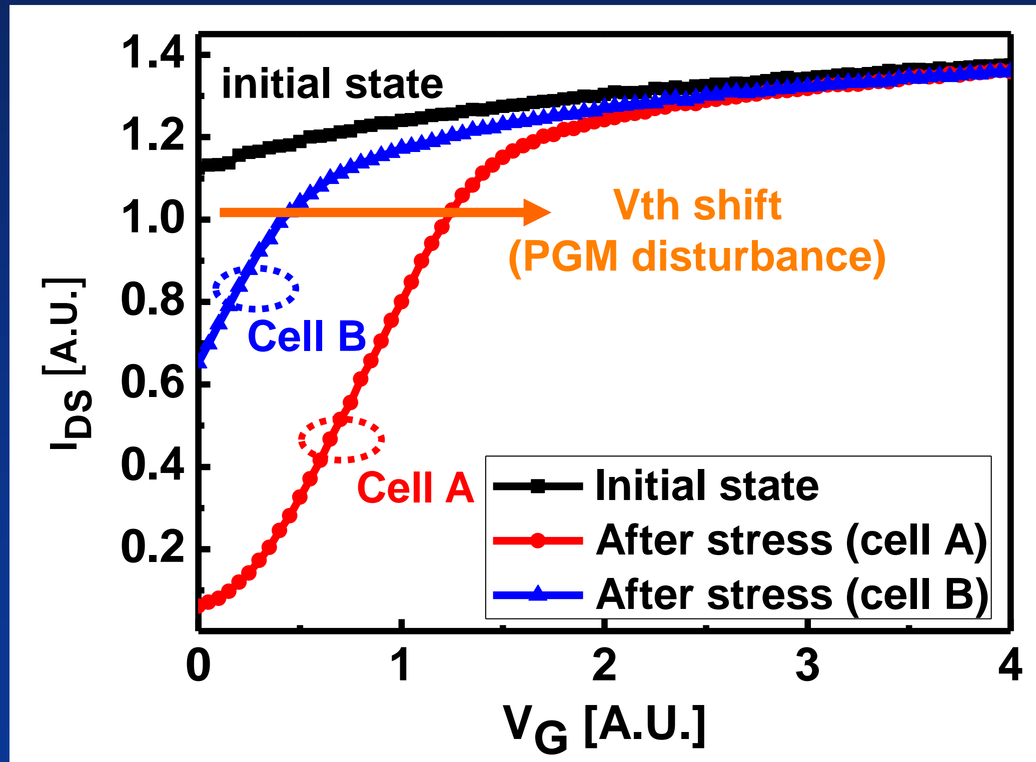
- Low boosting level → FN tunneling disturb
- High boosting level → edge cell HCI disturb



Mode	Program Inhibit	Program
B/L	Vcc	0V
DSL	Vcc	Vcc
Pass W/L	Vpass1,2	Vpass
Sel. W/L	Vpgm	Vpgm
SSL	0V	0V
SL	Vcc	Vcc
Pwell	0V	0V

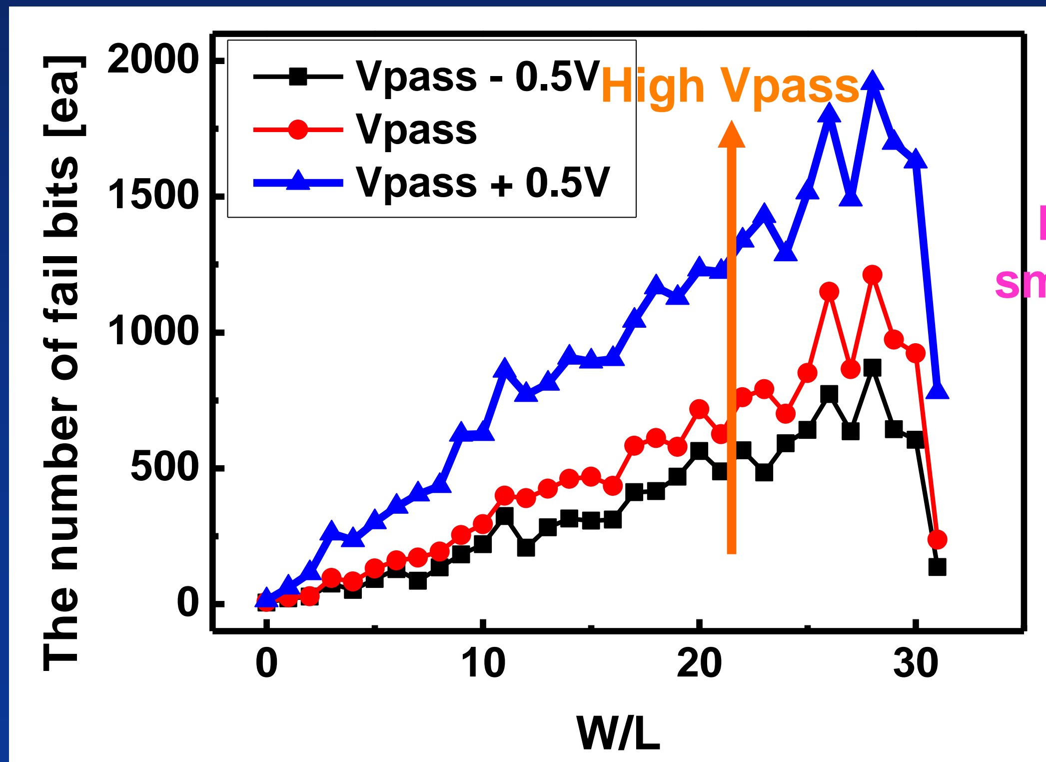
Ids-Vg curves of disturbed cell

- Vth of erase cells are increased as proceeding of program operation.



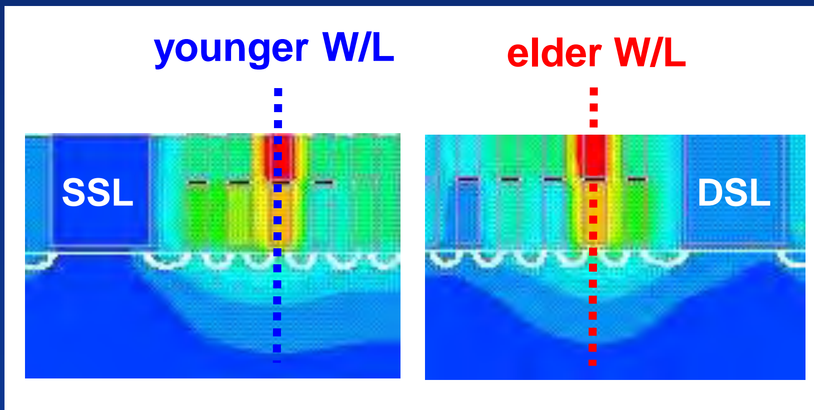
W/L dependency of program disturb

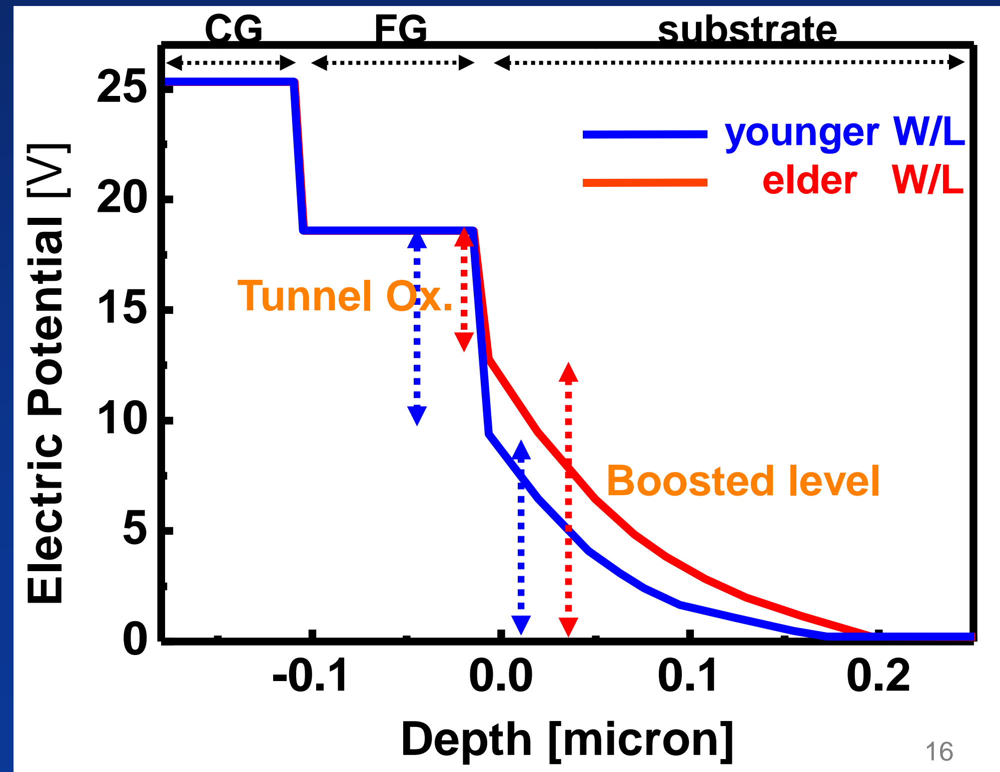
- Severe disturbance in elder W/L.
- Edge cell HCI is negligible.
- Increasing Vpass → larger fail bits



Electric potential

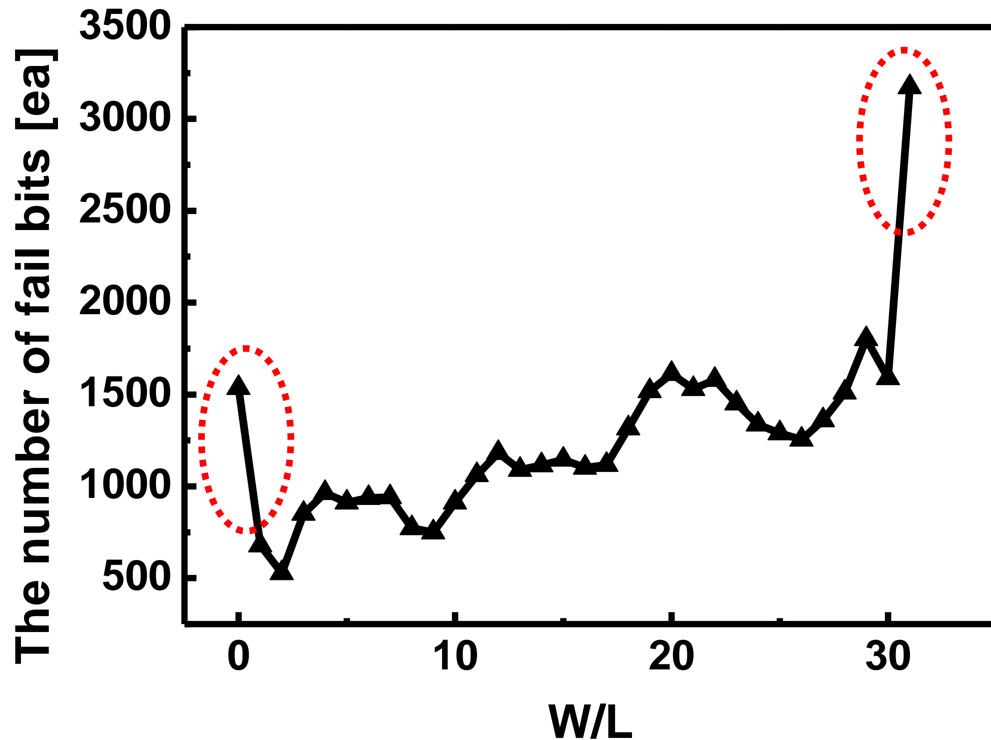
- Tunnel Ox. voltage: younger W/L > older W/L
- Channel boosting : younger W/L < older W/L
  → HCI due to boosting level cut off,
  → HCI from substrate ?

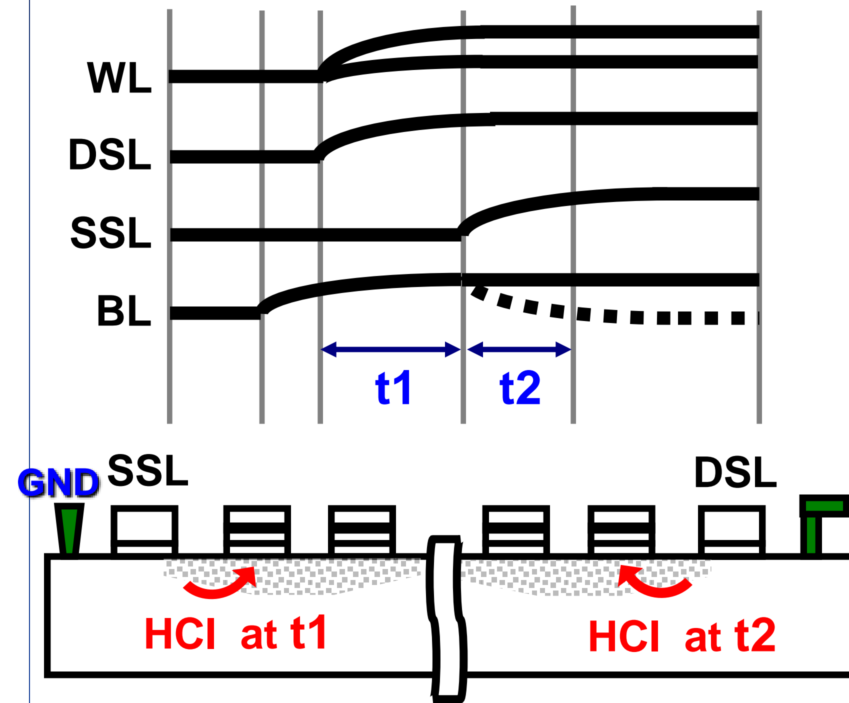




Read disturb

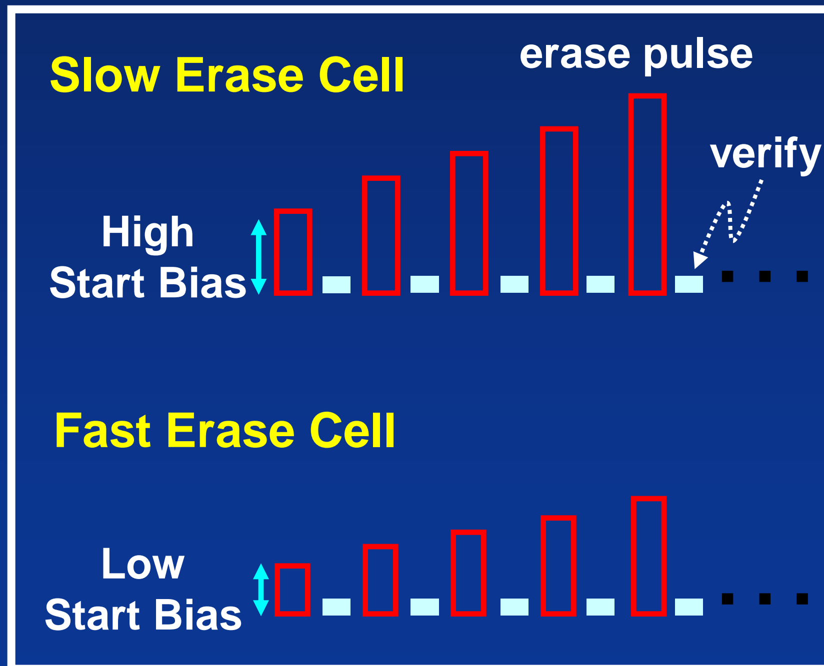
- Edge W/L worst : edge HCI injection
- Pulse sequence optimization

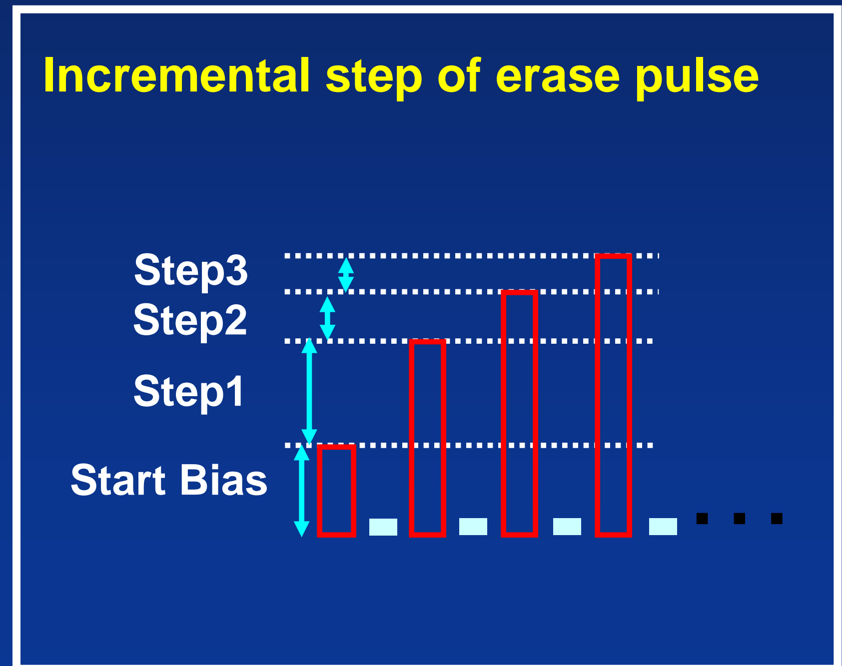




Erase pulse

- Starting bias and an incremental step of erase pulse should be adjusted for each block and chip.





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Summary

- Structure
  - IPD
  - Floating-gate height
  - Active edge dopant profile
  - UV-Vth
- Operation
  - Program disturb
  - Read disturb
  - Erase pulse