STT-RAM: Advantages & Applications

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Grandis, Inc.

Flash Memory Summit

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Existing Memories in Crisis

- Mobile RAM – power consumption now a real issue
  - High power consumption during writing and in standby
- Embedded SRAM – performance and cost deteriorating
  - Very large cell size, plus leakage, instability and noise
- Standalone DRAM – very challenging to scale
  - Storage capacitance, retention time, leakage current

Memory performance fast becoming the key bottleneck that limits system performance, no existing technology can deliver the required performance

Current Flash Challenges

- Flash memory evolution
  - High capacity and low cost, 2, 3 & 4 bit MLC
  - Large page size, increased resource for block management
  - Aggressive scaling, reduced performance and reliability
  - Meeting endurance target becomes more difficult

  These problems create an opening for an alternative, high density Non-Volatile Random Access Memory

- Grandis STT-RAM will be the only solution within 1–2 years with speed fast enough to replace DRAM.
  - Initially, embedded memory & low power mobile RAM replacement
  - In medium term, DRAM replacement
  - Ultimately, a storage class memory that can compete with NAND

Grandis Corporation Overview

- Grandis develops & licenses proprietary NVM solutions
  - Grandis' STT-RAM enables a wide variety of low-cost and high-performance memory products at 45 nm and beyond
- Headquarters: Silicon Valley, CA
- Strong & broad STT-RAM patent portfolio and know-how
  - Total 192 patents filed and 68 granted worldwide

Our mission is to establish Grandis STT-RAM as the #1 choice for memory solutions beyond 45 nm

Grandis Milestones in STT-RAM

2002: Grandis files first key patents in STT-RAM

2004: Grandis reports world's first STT switching in MTJs

2005: Renesas Technology licenses Grandis IP

2007: Grandis wins NIST ATP award to develop STT-RAM

2008: Hynix Semiconductor licenses Grandis IP and begins developing standalone STT-RAM

Grandis wins $15M DARPA contract to develop STT-RAM chips

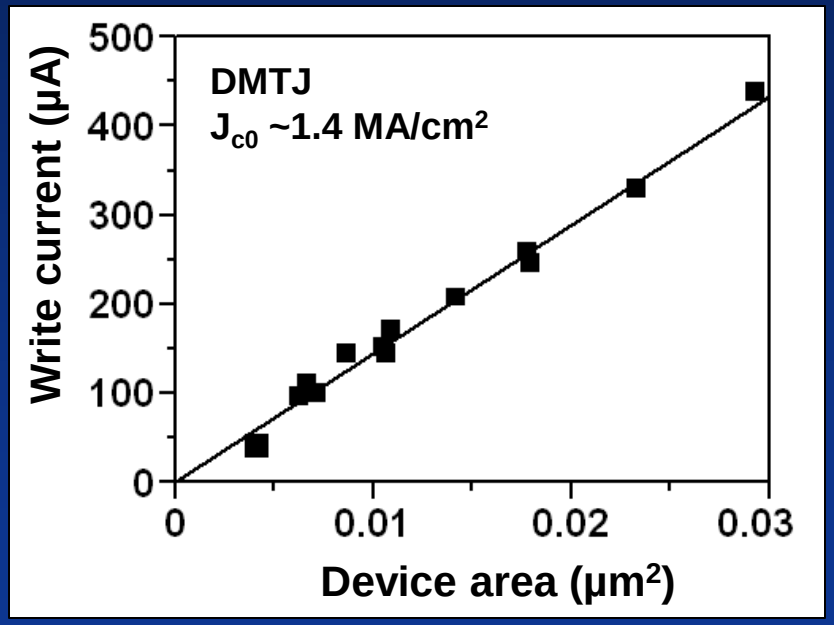
2009: Grandis upgrades MTJ Fab to handle 300 mm customer wafers

2010: Grandis achieves DARPA Phase I milestones (<0.25 pJ)

Grandis Development Partners

STT-RAM Scalability

- STT-RAM write current scales linearly with device area
  - Write current ~40 µA at 45 nm



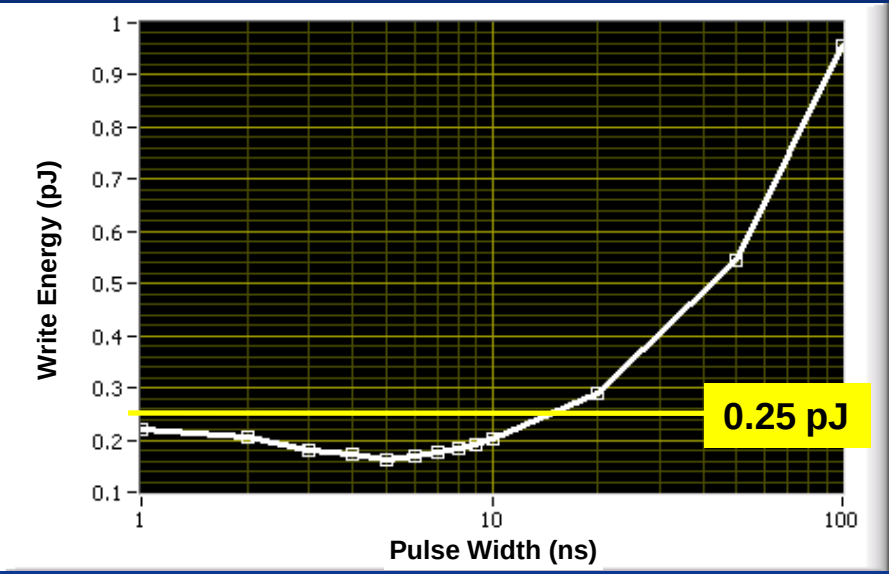
- In-plane STT-RAM is scalable beyond 20 nm
- Perpendicular STT-RAM is scalable beyond 10 nm

Latest Advances in Write Energy

- Write energy <0.25 pJ demonstrated in March 2010
  - Pulse widths 1-10 ns, MTJ dimension 60 nm, thermal stability Δ >60
  - Meets DARPA Phase I milestones, Phase II begins Sep 2010

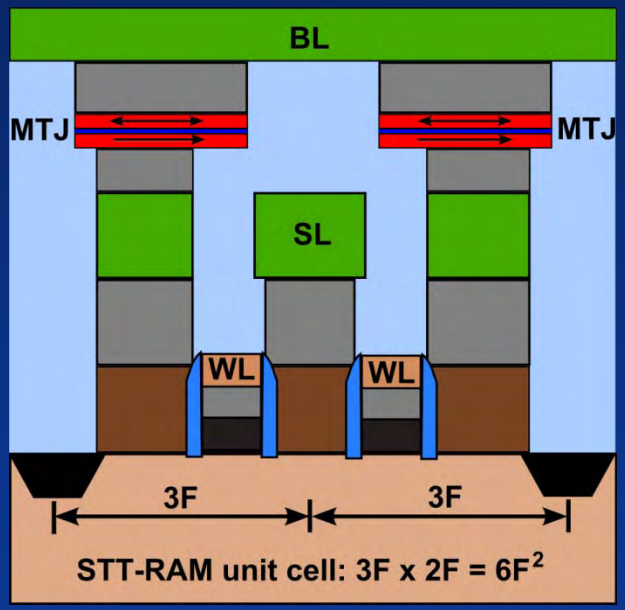
DARPA STT-RAM Project Metrics

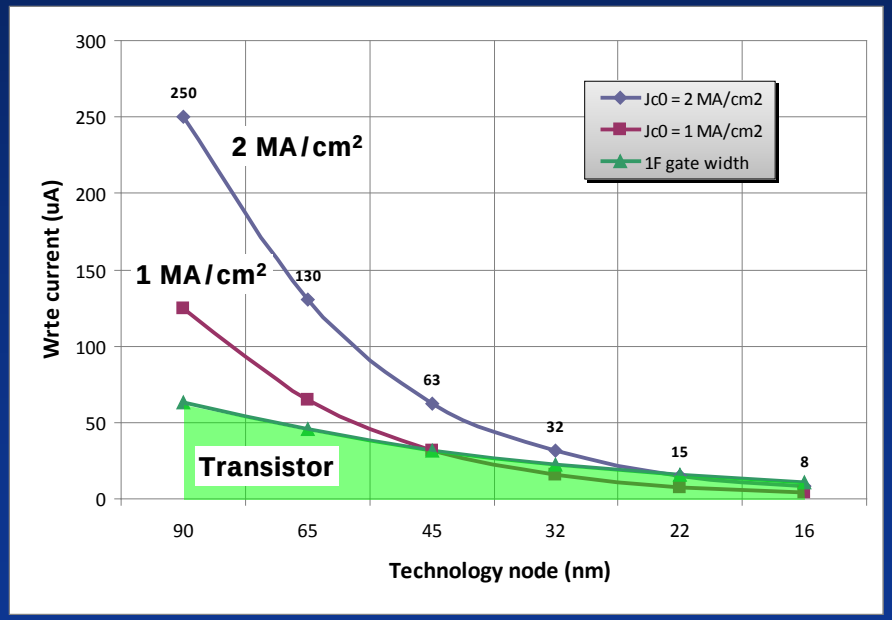
	Phase 1	Phase 2
Write Energy	0.25 pJ/bit	0.06 pJ/bit
Write/Read Speed	5 ns/bit	5 ns/bit
Cell Size	0.24 sq. µm	0.12 sq. µm
Memory Bit Area	0.02 sq. µm	0.02 sq. µm
Thermal Stability (Δ)	60	80
Endurance (cycles)	1.00E+16	>3.00E+16
Wafer Yield	40% operational memory bits	40% operational 1 MB memory die



STT-RAM Minimum Cell Size

- 6 F^2 minimum cell size with shared source line architecture
  - Minimum 1 F gate width transistor can drive 6 F^2 cell beyond 45 nm

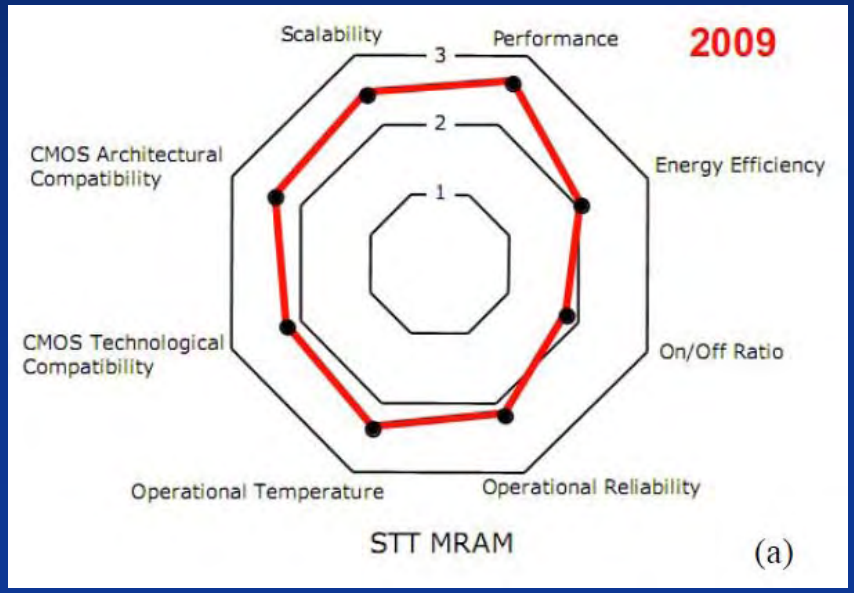




- Vertical transistors, multi-level cells and/or cross-point architectures enable further cell size reduction beyond 4 F^2

STT-RAM Technology Acceptance

- Major companies across the semiconductor industry accept that STT-RAM is the leading next-generation memory
  - STT-RAM leads all other memory technologies across the eight ITRS key attributes



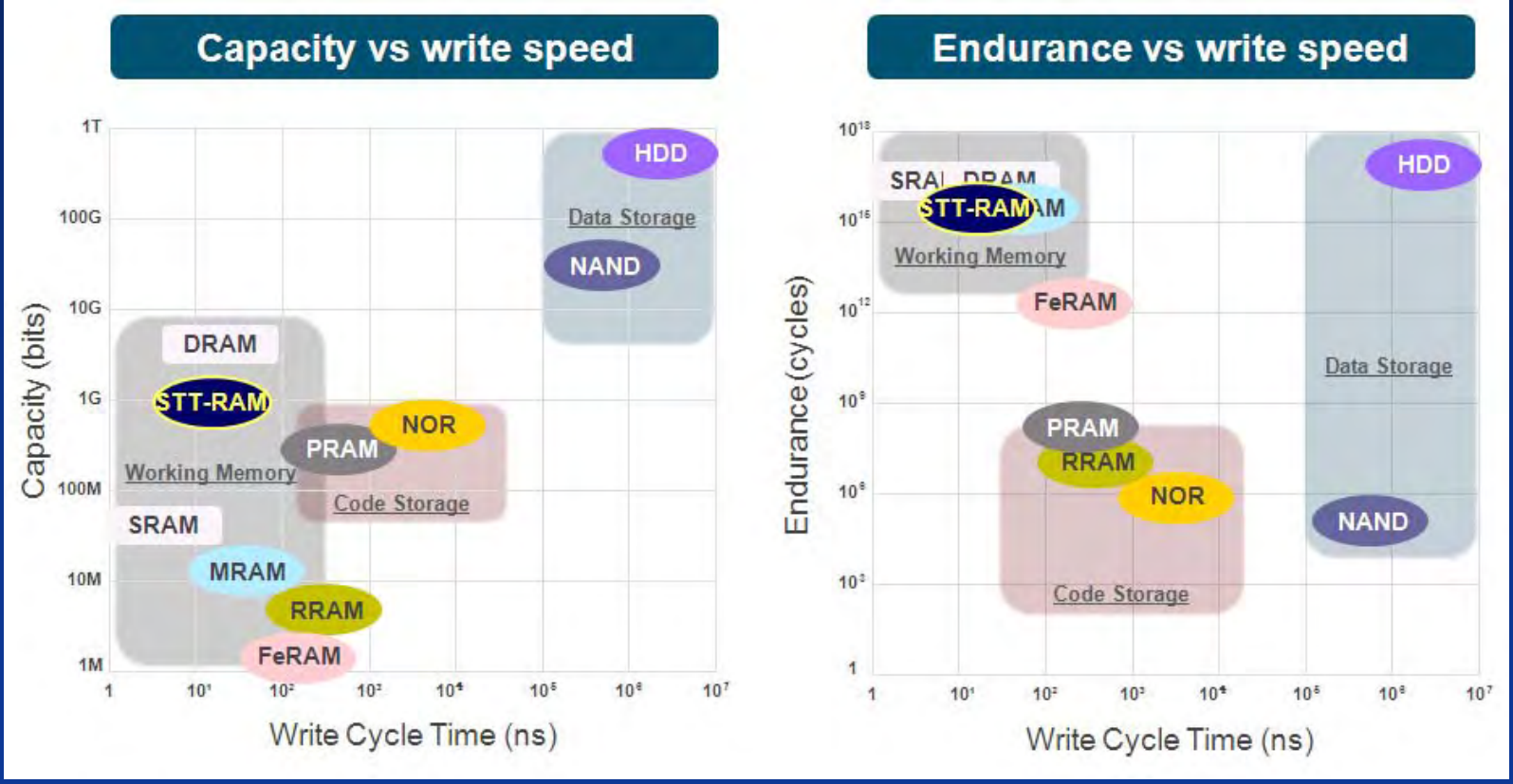
Source: ITRS Roadmap for Semiconductors, Dec. 2009

Intensified Development of STT-RAM

- **Nov. 2009:** Korean Government updates on $50M STT-RAM program with **Samsung** and **Hynix**
- **Dec. 2009:** **TSMC** and **Qualcomm** describe 45 nm low power embedded STT-RAM process and design at IEDM
- **Dec. 2009:** Also at IEDM, **Hitachi** presents MTJ SPICE model, and **Intel** presents design space study for STT-RAM
- **Feb. 2010:** **Toshiba** describes 64 Mb STT-RAM using perpendicular MTJs and 65 nm CMOS at ISSCC conference
- **Apr. 2010:** **Everspin** takes MRAM to higher densities, begins sampling 16 Mb MRAM, targeted at the aerospace, automotive, industrial and RAID storage markets, continues to develop STT-RAM
- **Jun. 2010:** **Grandis**, **Hitachi** and **Fujitsu** all present papers on STT-RAM at VLSI symposium covering thermal stability, scalability and MLC
- **Dec. 2010:** **Hynix** and **Grandis** to present joint paper on high-density STT-RAM chip operation at IEDM

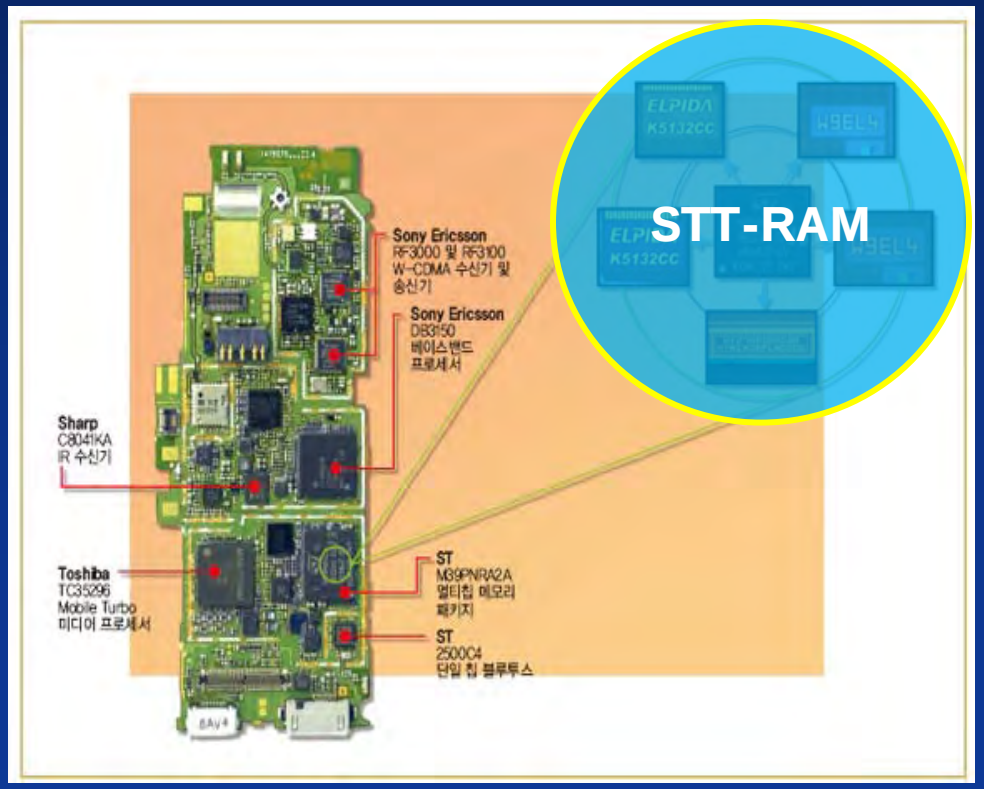
Memory Technology Comparison

- STT-RAM has the *capacity* of and *density* of working memory, plus it is *non-volatile* & has *low power consumption*



Mobile RAM Application

- STT-RAM can replace MCPs with a single chip
  - Non-volatile, higher-speed, lower power consumption, and lower cost



Handset Solution
Sharp 922SH

Multi-Chip Package (MCP)
(ST M39PNRA2A)

NOR: STMicro 512Mb 2pcs

NAND: Hynix 2Gb
SLC(single-level-cell)
1Pcs

DRAM: Elpida 512Mb DDR2
SDRAM 2Pcs

Smart Phone with Standard Memory

Image sensor

FRAME BUFFER (LP-SDR e.g. 64Mb)

Media Processor

ARM9

SiP

LCD Display

RF

Baseband/ Modem

Memory Cntrl

Serial i/f

Application Processor

Memory Cntrl

Audio/ Video/ TVout

MMC/ SD

x16 (mux)

x16(mux)

x16/x32

x8/x16

Store & run radio protocol stack

NOR

PSRAM

MCP

NOR

LP-DDR

NAND SLC/MLC

MCP

on-chip level 1(2) cache sizes are a function of ext. memory access latency and required bandwidth

Smart Phone with STT-RAM Memory

Image sensor

On-chip STT-RAM Frame Buffer e.g. 64Mb)

Media Processor

ARM9

LCD Display

RF

Baseband/ Modem

Memory Cntrl

Serial i/f

Application Processor

Memory Cntrl

Audio/ Video/ TVout

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Store & run radio protocol stack

STT-RAM

STT-RAM

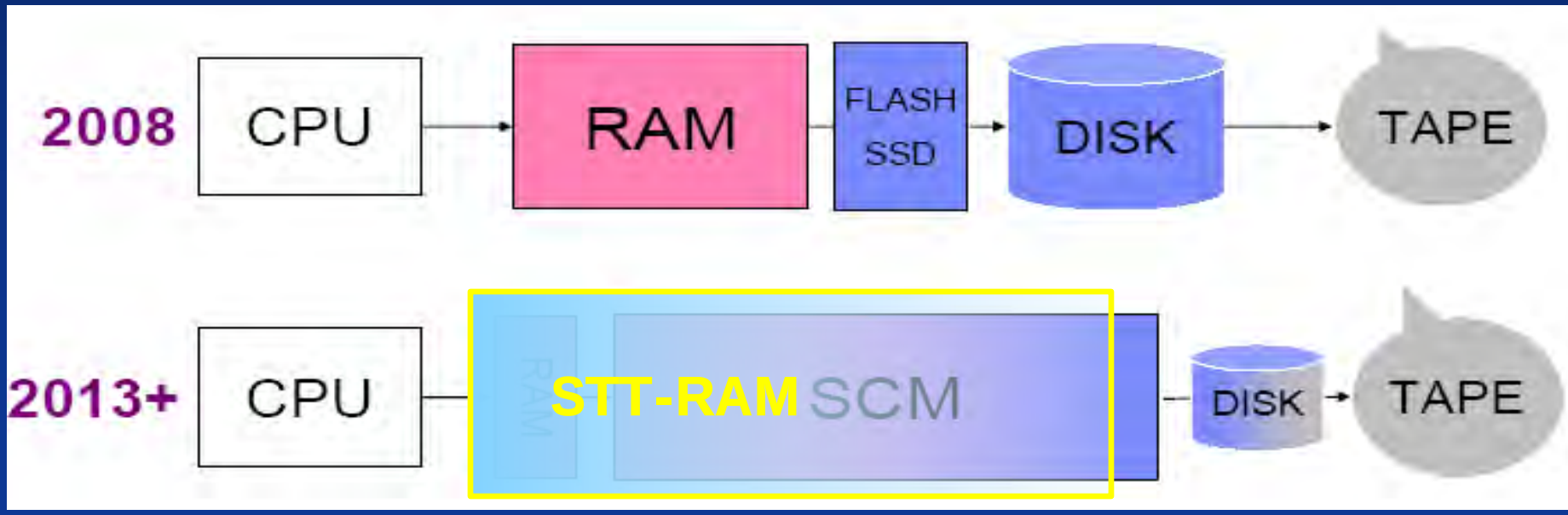
NAND SLC/MLC

MCP

on-chip level 1(2) cache sizes are a function of ext. memory access latency and required bandwidth

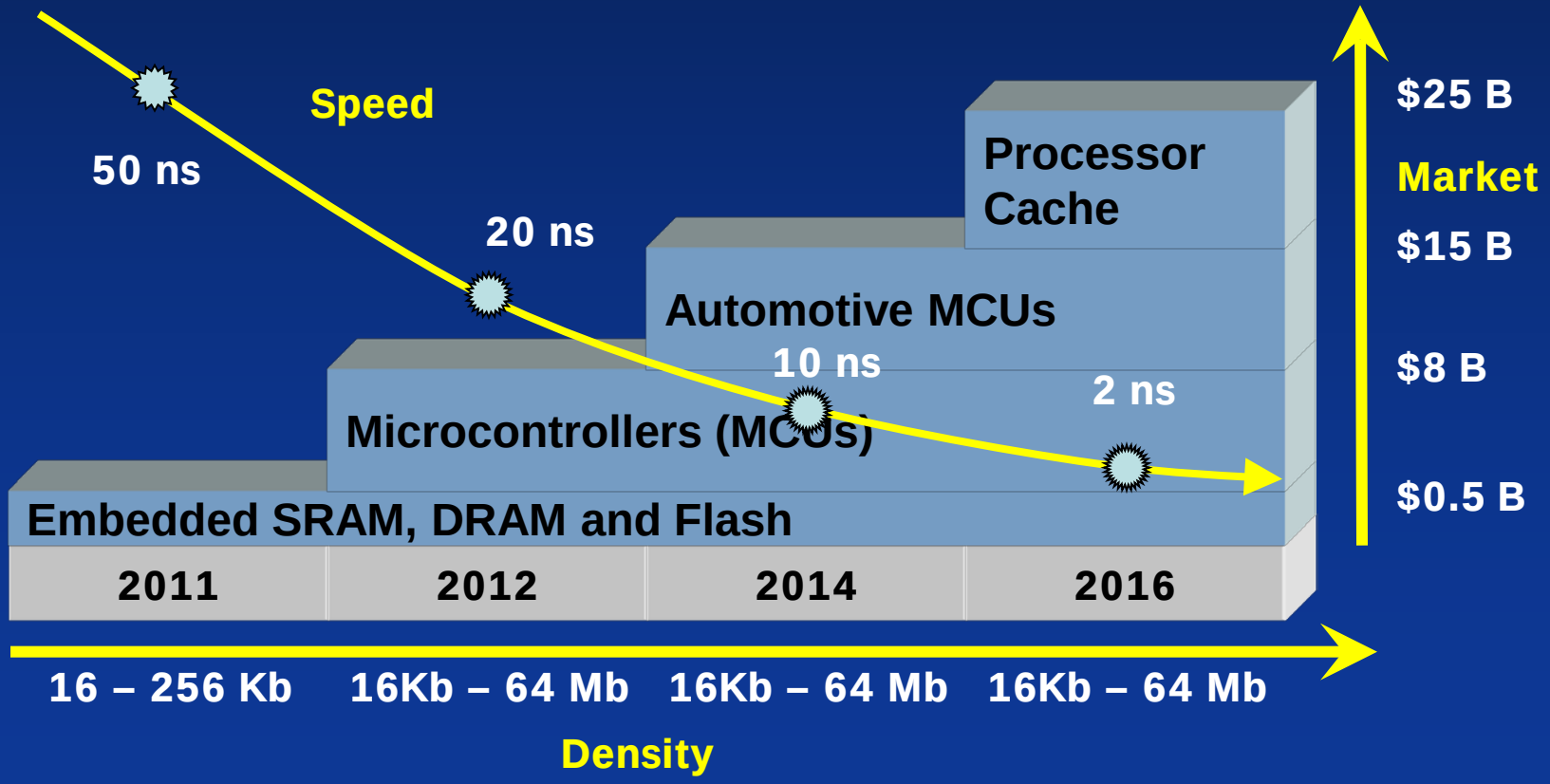
Enterprise SSD Application

- Urgent need for a high-performance, storage class memory for enterprise applications
  - STT-RAM can be a combined low latency RAM and non-volatile cache for enterprise storage applications

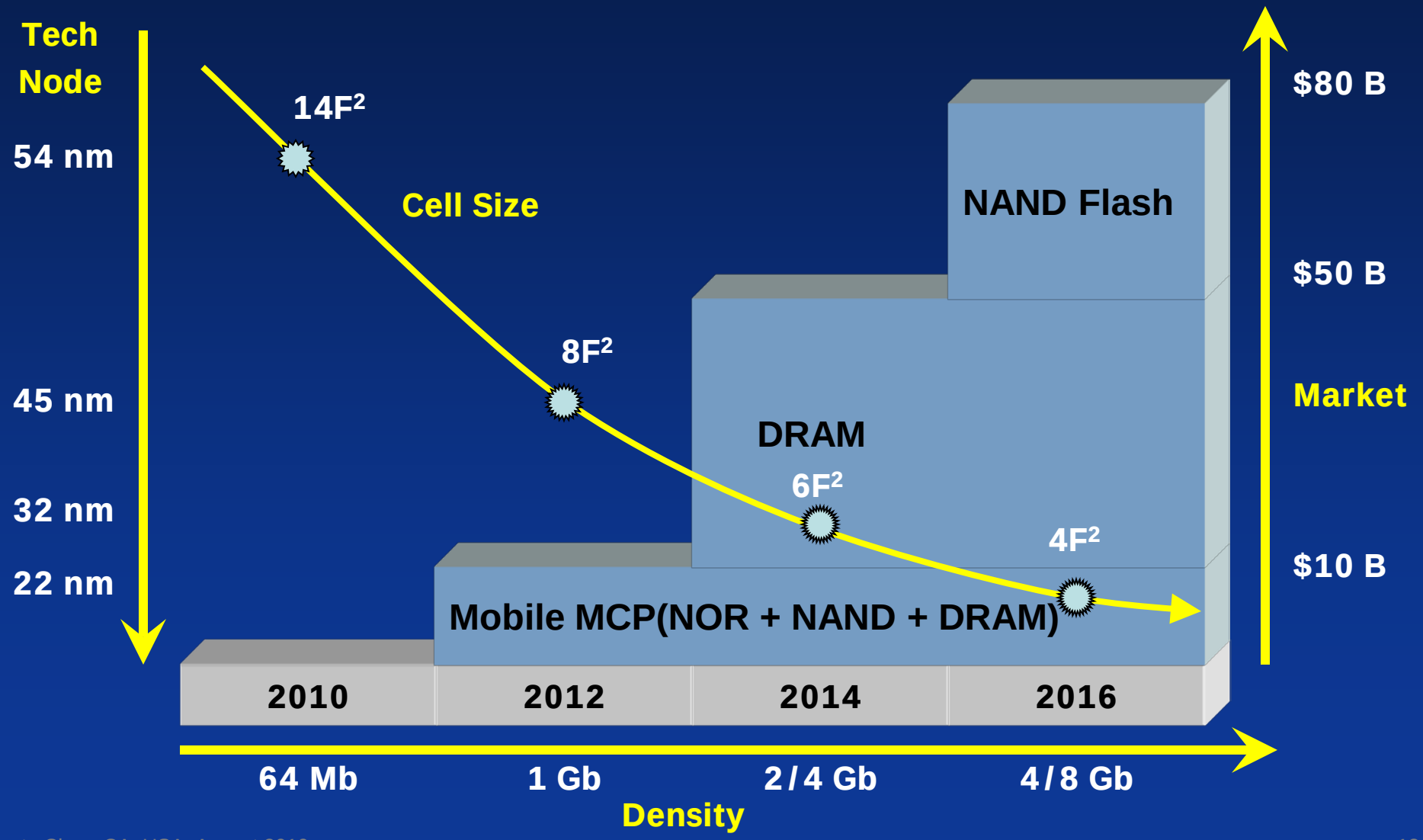


Embedded STT-RAM Roadmap

- Initial applications: replace embedded non-volatile memory in industrial, medical, consumer and military MCU units



Standalone STT-RAM Roadmap



Challenges for STT-RAM

- Grandis is working with its partners to address key challenges for STT-RAM
  - Proving technology reliability for large scale manufacturing
  - Tuning cell design for different application requirements

- To fully exploit STT-RAM's characteristics, a fundamental rethink of computing system architecture will be required
  - STT-RAM can enable revolutionary advances in latency, bandwidth, reliability and power-efficiency for data-intensive applications

The return on investment towards reducing overall system cost and added system functionality well justifies the effort to meet the above challenges

Flash Memory SUMMIT

GRANDIS
Pioneer in STT-RAM Technology

Summary

- STT-RAM accepted as the leading next-generation memory
  - Enables new era of instant-on computers, high-speed portable devices with extended battery life, and enterprise servers & storage
- Worldwide STT-RAM development has reached critical mass
  - Government programs in US (DARPA), Japan, Korea, France, Singapore
  - Hynix, Samsung, Renesas, Toshiba, Hitachi, Fujitsu, TSMC, Qualcomm, Intel, IBM, Everspin, …

With its partnerships with key semiconductor memory players and key fundamental and blocking patents in STT-RAM, Grandis is focused on commercializing STT-RAM in 1–2 years

Please visit

www.GrandisInc.com

for more information