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Power Design Issues in Enterprise SSD

Problem Statement

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    - Need Short Power Design Cycle

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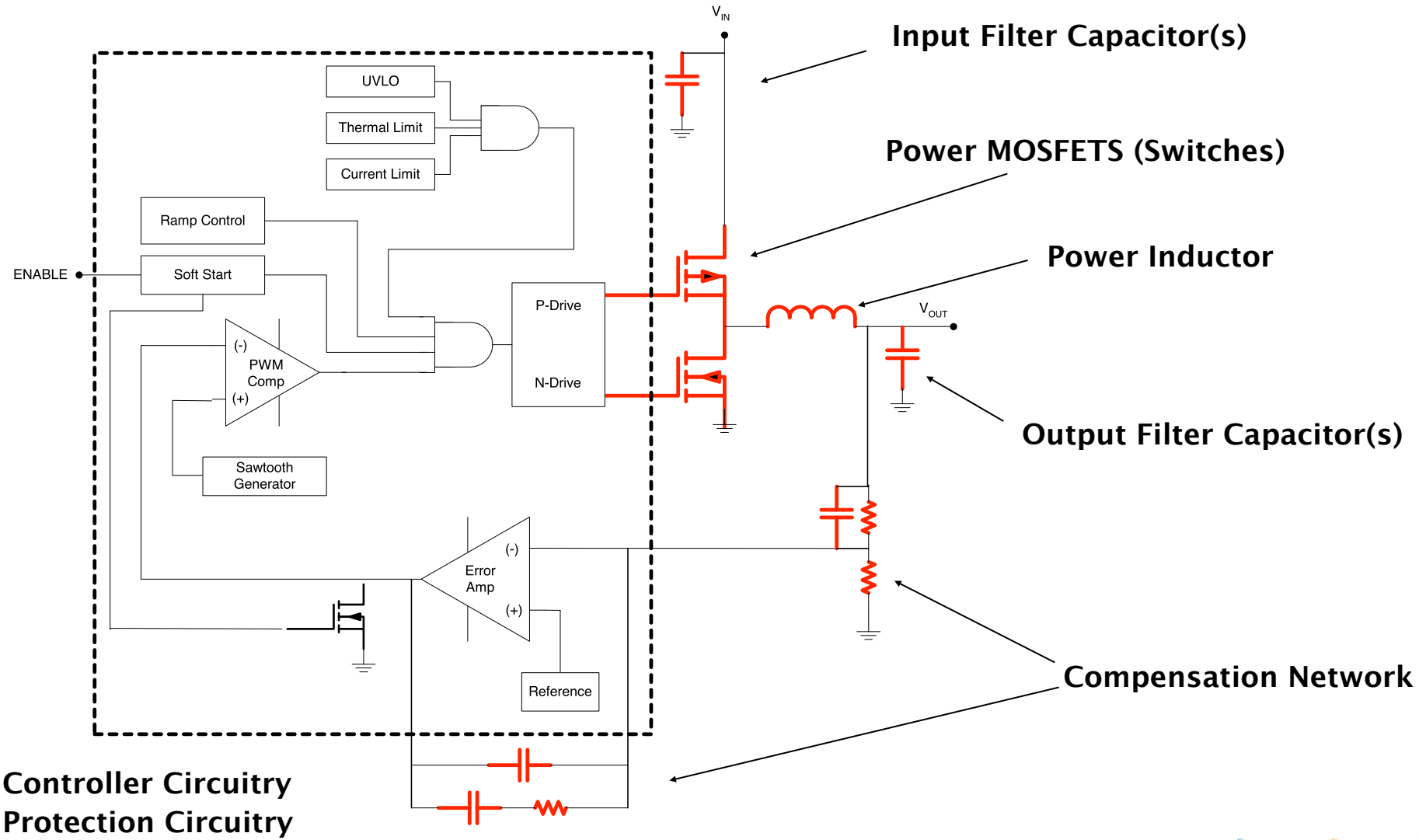
Converter and Components

Synchronous Buck Switch-Mode DC-DC



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A Little About Inductors

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  - Each supplier has own proprietary design/materials
    - Core material formulation
    - Winding technique and conductor type
    - Electrode material
    - Baking method

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  - Frequency dependencies/Small signal
- Temperature dependencies
  - DC Losses: resistivity
  - AC Losses: skin effect, proximity effect,…
  - Saturation Flux Density

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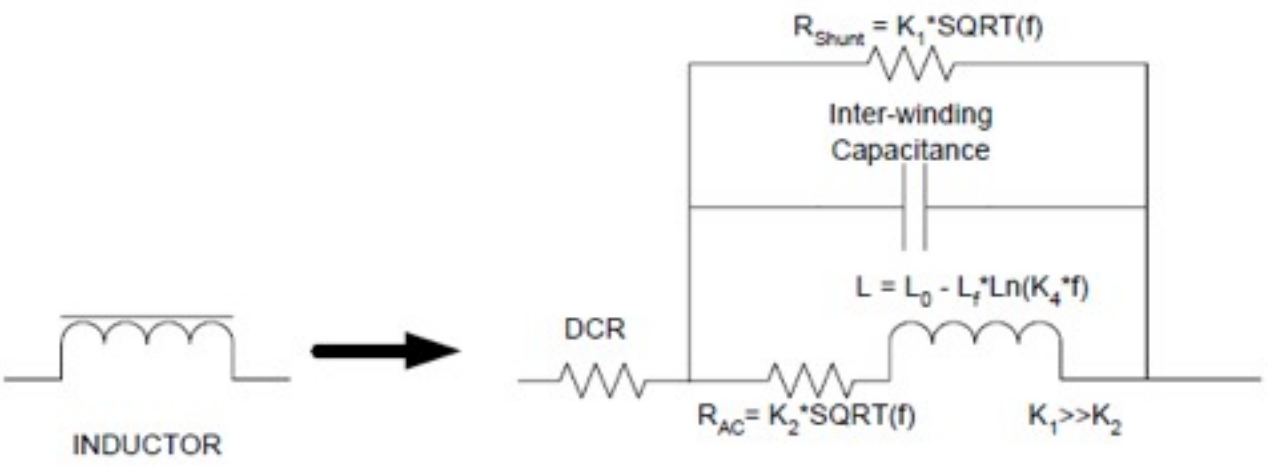
Inductor Characterization

Inductor Characterization

- Small Signal Parameters
- DC
- DC
- AC
- AC
- Ser
- Ser
- Impedance Magnitude and Phase vs Frequency
- Inductor Physical Dimension Analysis
- RoHS: Core, Conductor, Electrode Material Composition
- All of this is Different for Every Manufacturer



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Inductor Characterization

- Small Signal Parameters
- DC Resistance; Variation over Temp, Bias, Load
- DC Power Loss vs Load Current
- AC Power Loss vs Volt Seconds Stress and Temp
- AC Power Loss vs Frequency and Temp
- Series Inductance vs Load Current
- Series Inductance vs Temp
- Impedance Magnitude and Phase vs Frequency
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A Few Words on Capacitors

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- Industry Standards do Exist
- Capacitor Ratings exist at: “0V” bias; “25°C”; “0” Hz frequency
- Lose Capacitance with Frequency
- Lose Capacitance with Temperature
- Lose Capacitance with Bias Voltage

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$$\Delta V_{out} = \frac{\Delta I_{load}}{8 . BW . C_{out}}$$

Voltage Transient for a given load step, Loop BW, and Capacitor

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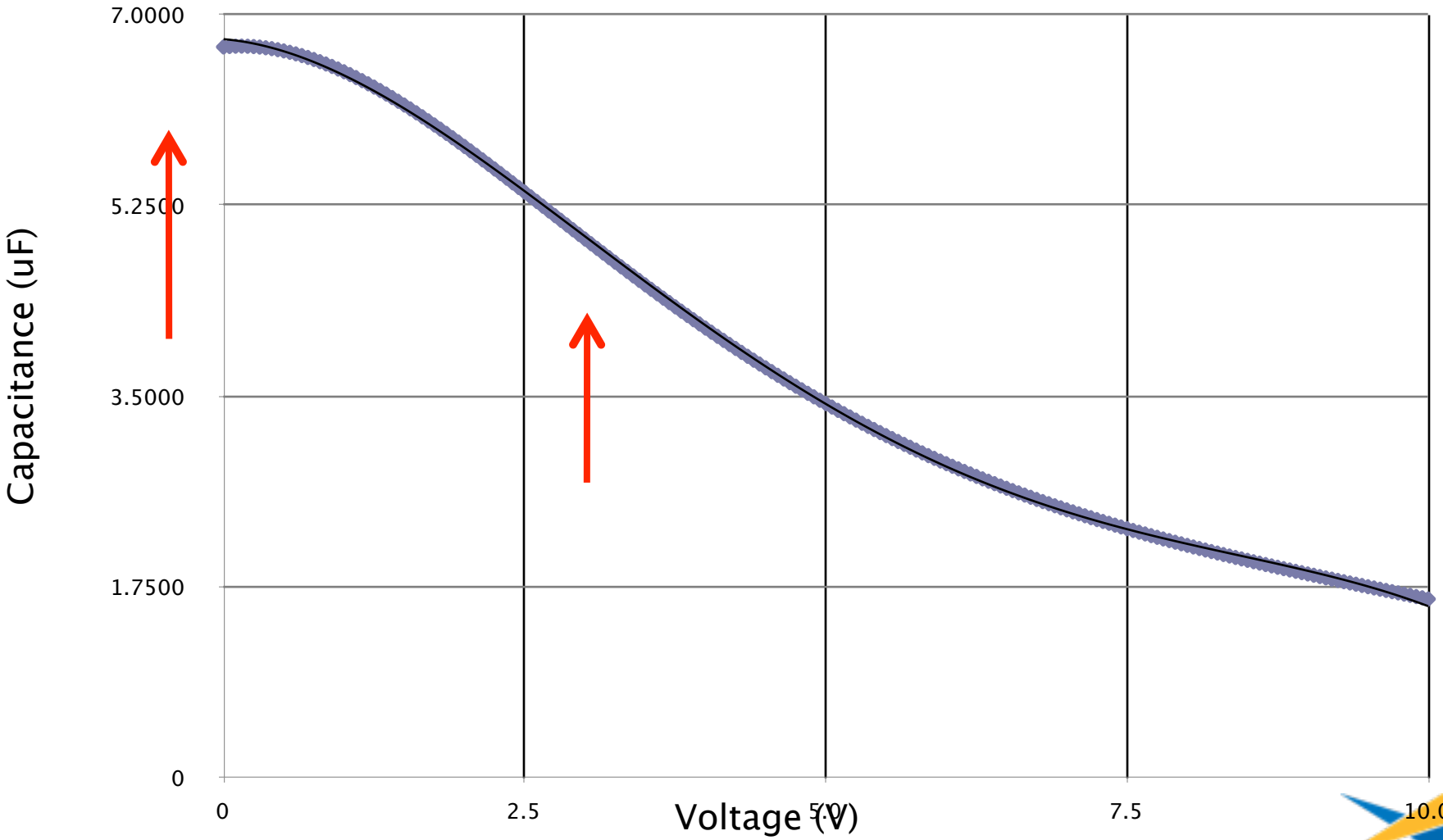
Capacitance vs Bias Example: 10uF 0805, X5R, 10V



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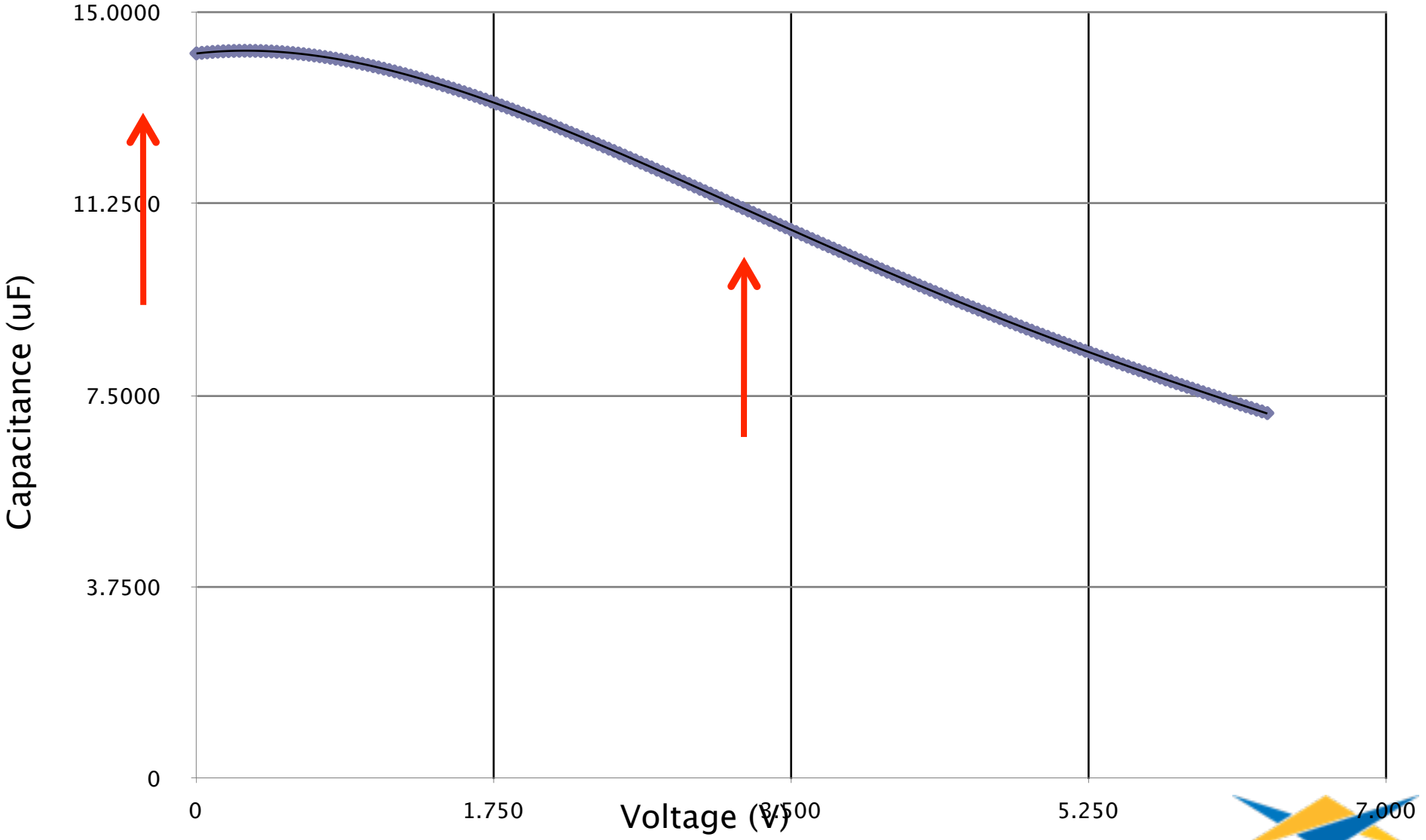
Capacitance vs Bias Example: 22uF 1206 X5R 6.3V



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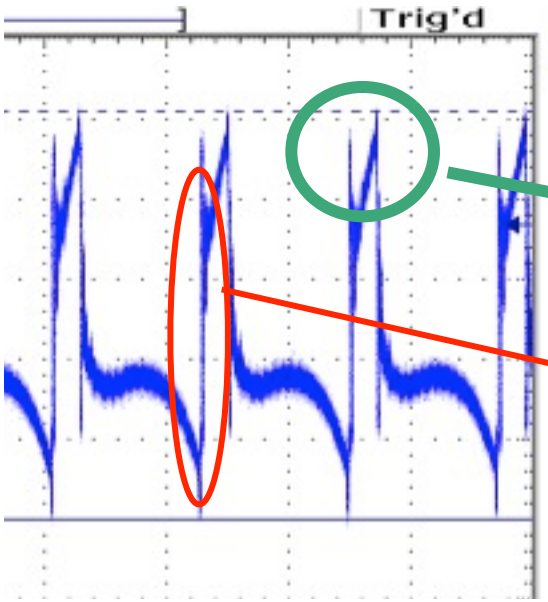
DCDC Converter Noise

- Output Ripple
- Radiated EMI
- Conducted EMI

Output Voltage Ripple

- Results from the output AC ripple current passing through the ESR and ESL of the output filter capacitor and the ESR and ESL of the PCB traces.



Output Ripple Waveform

Capacitor Equivalent Circuit

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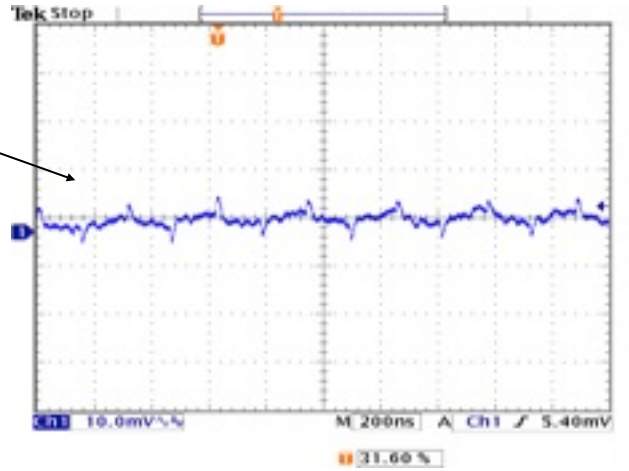
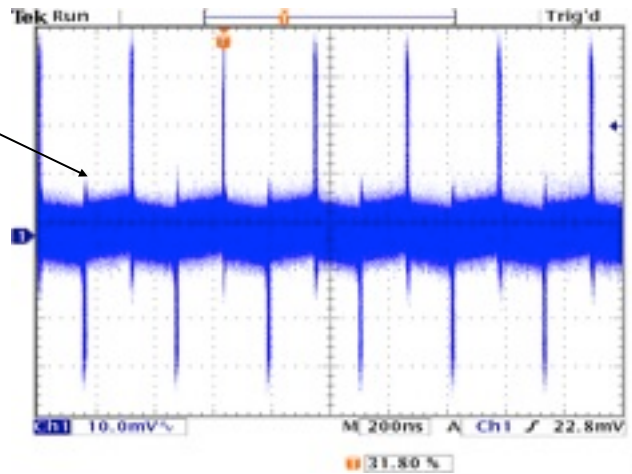
DCDC Datasheets Obfuscate the Truth About Ripple

Datasheets show band limited waveforms



20MHz Scope BW

Here is the actual ripple for this part



500MHz Scope BW

This is the noise the load "sees"

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Radiated Noise Considerations

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- Radiated noise results from high di/dt AC currents flowing in the input current loop path

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$$P_{RAD} = \eta \frac{\pi \left(\frac{2\pi r^2}{\lambda} \right)^4}{12} \left| I_0 \right|^2$$

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Radiated Noise Considerations

- Radiated noise results from high di/dt AC currents flowing in the input current loop path
- Solution is to minimize the radius of the current loop
  - Radiated power decreases by r^8

$$P_{RAD} = \eta \frac{\pi \left(\frac{2\pi r^2}{\lambda} \right)^4}{12} \left| I_0 \right|^2$$

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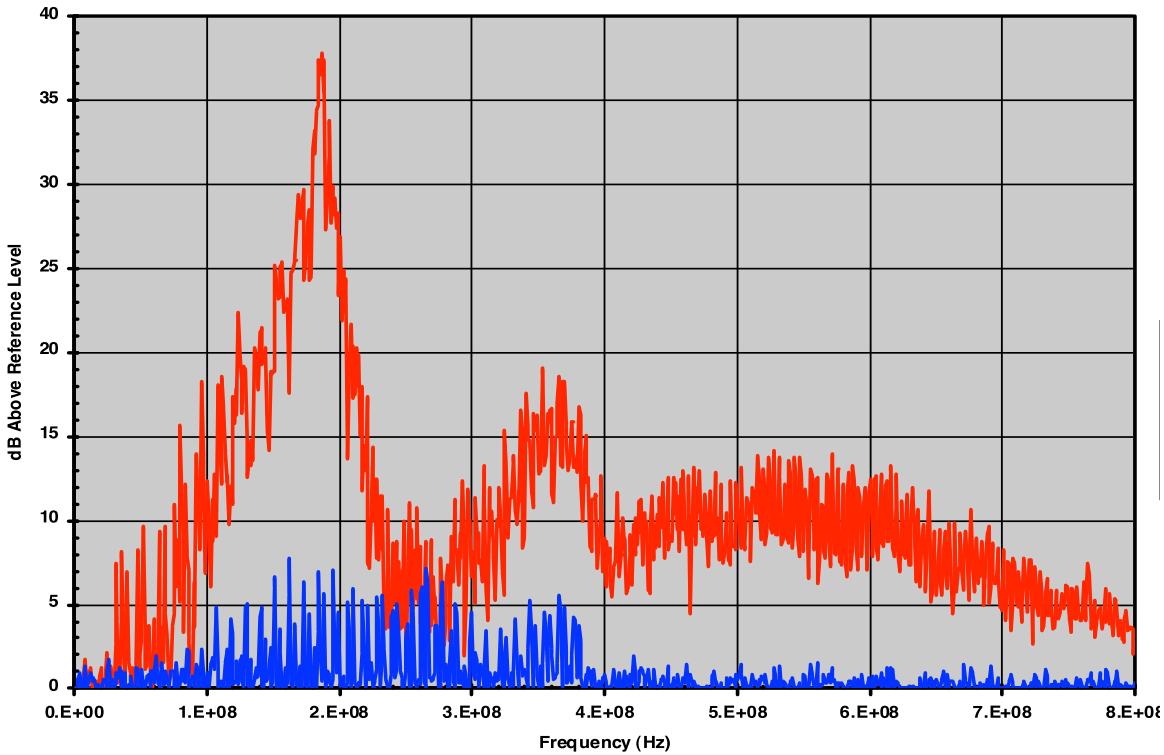
Conducted Noise Considerations

- Results from AC currents flowing through the parasitic inductances in the input ground plane.



Common mode voltage measured on input ground terminal

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Memory Termination

Many Enterprise Class SSDs Require DDRx

- High performance DDR DRAM requires termination
- Common approach is to use Linear Termination
  - Linear termination is only 50% efficient
  - Fine if you don't have power and thermal limitations
- Switch mode DCDC can be up to 95% efficient
  - However, DCDC can be complex, expensive, and have large footprint

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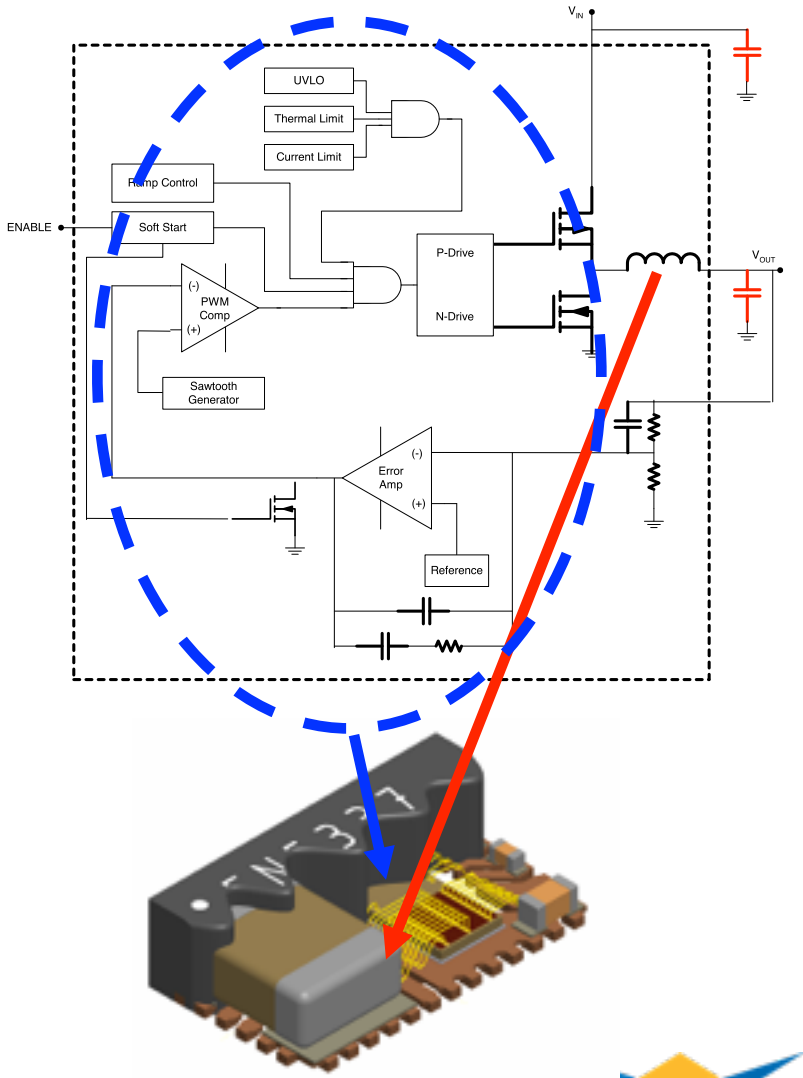
PowerSoC: a Possible Solution

- There are multiple vendors of PowerSoC
- Examples herein are Enpirion

What is a PowerSoC

- PowerSoC is defined by PSMA
- Integrates:
  - MOSFET Switches
  - Gate Drive Circuitry
  - Controller, and Protection
  - Most Compensation Circuitry
  - AND, the Magnetics



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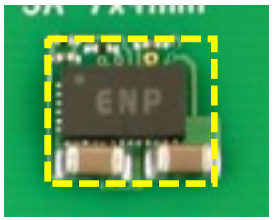
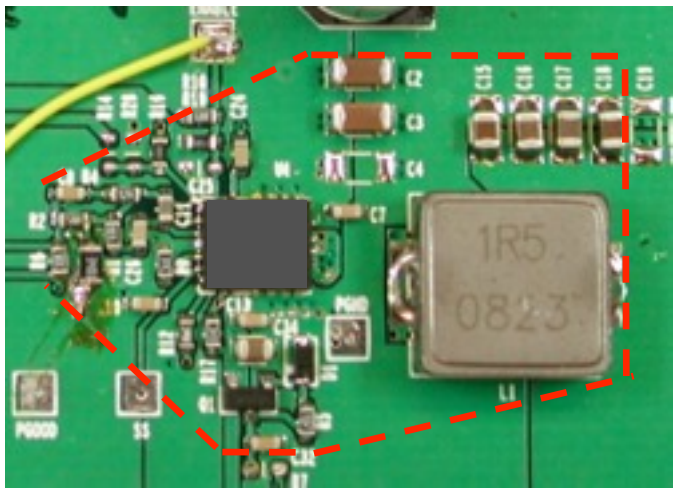
PowerSoC vs Discrete: Footprint Comparison

PowerSoC



Equivalent Discrete DCDC



Typically 1/4th to 1/8th the Discrete Footprint

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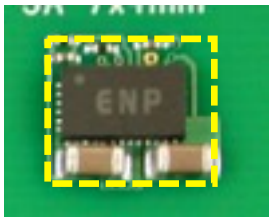

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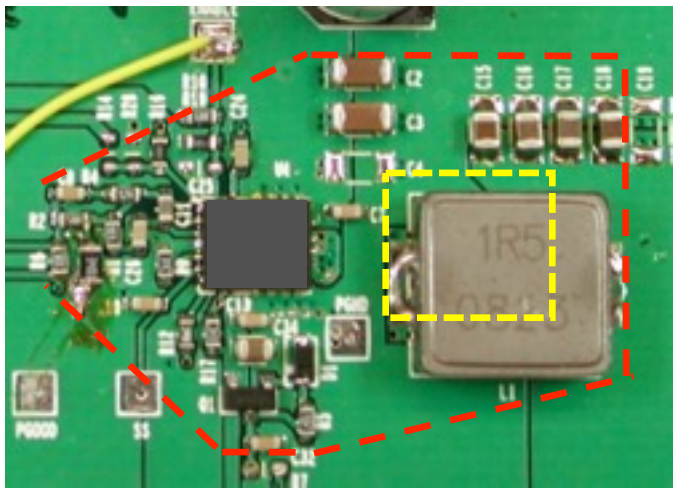

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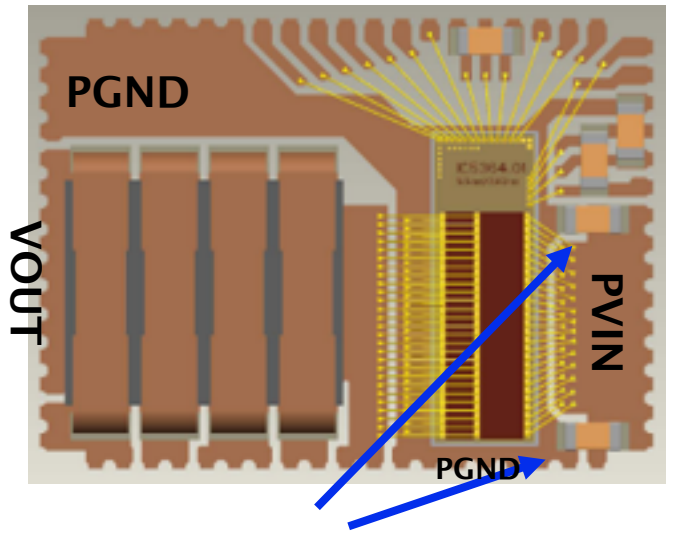
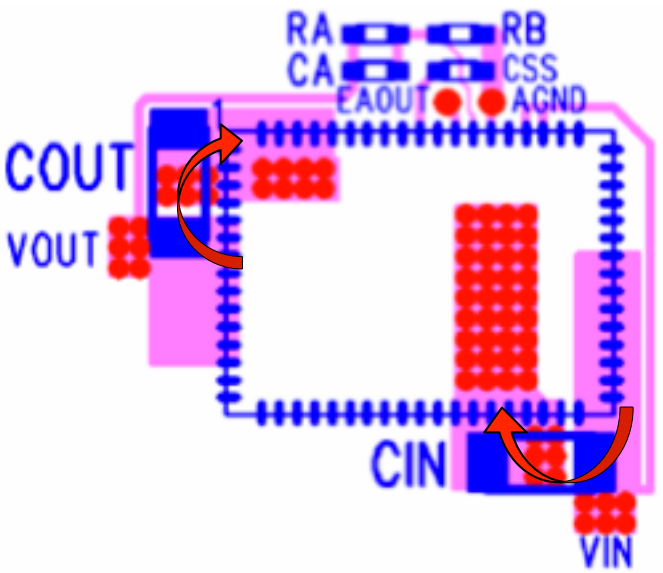
PowerSoC Addresses Noise Issues

- Package layout optimized for noise containment
- Input AC current loop very tight
- Output AC current loop very tight
- Package designed to minimize in-package parasitic impedances.



On board decoupling on input loop



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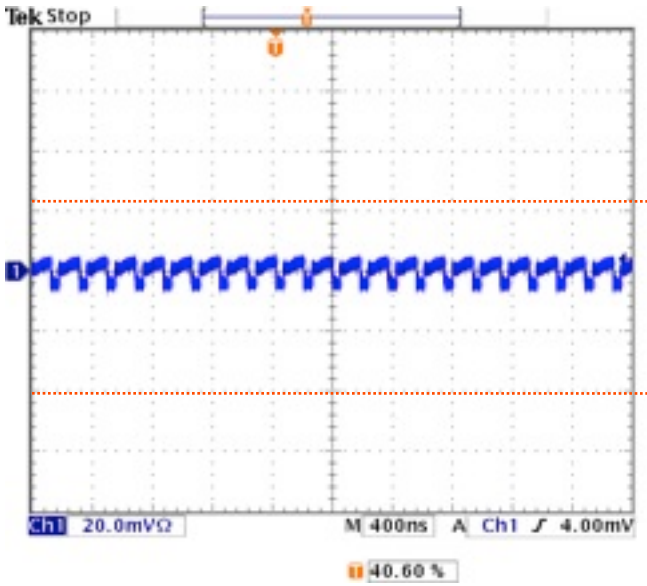
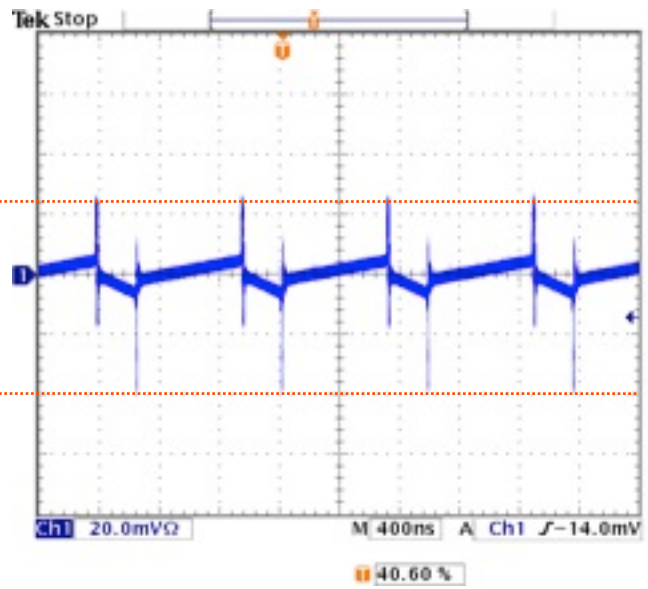
PowerSoC vs Discrete Buck: Ripple Comparison



PowerSoC
5Vin / 3.3Vout
3A Load

500MHz Bandwidth



Discrete Buck
5Vin / 3.3Vout
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500MHz Bandwidth

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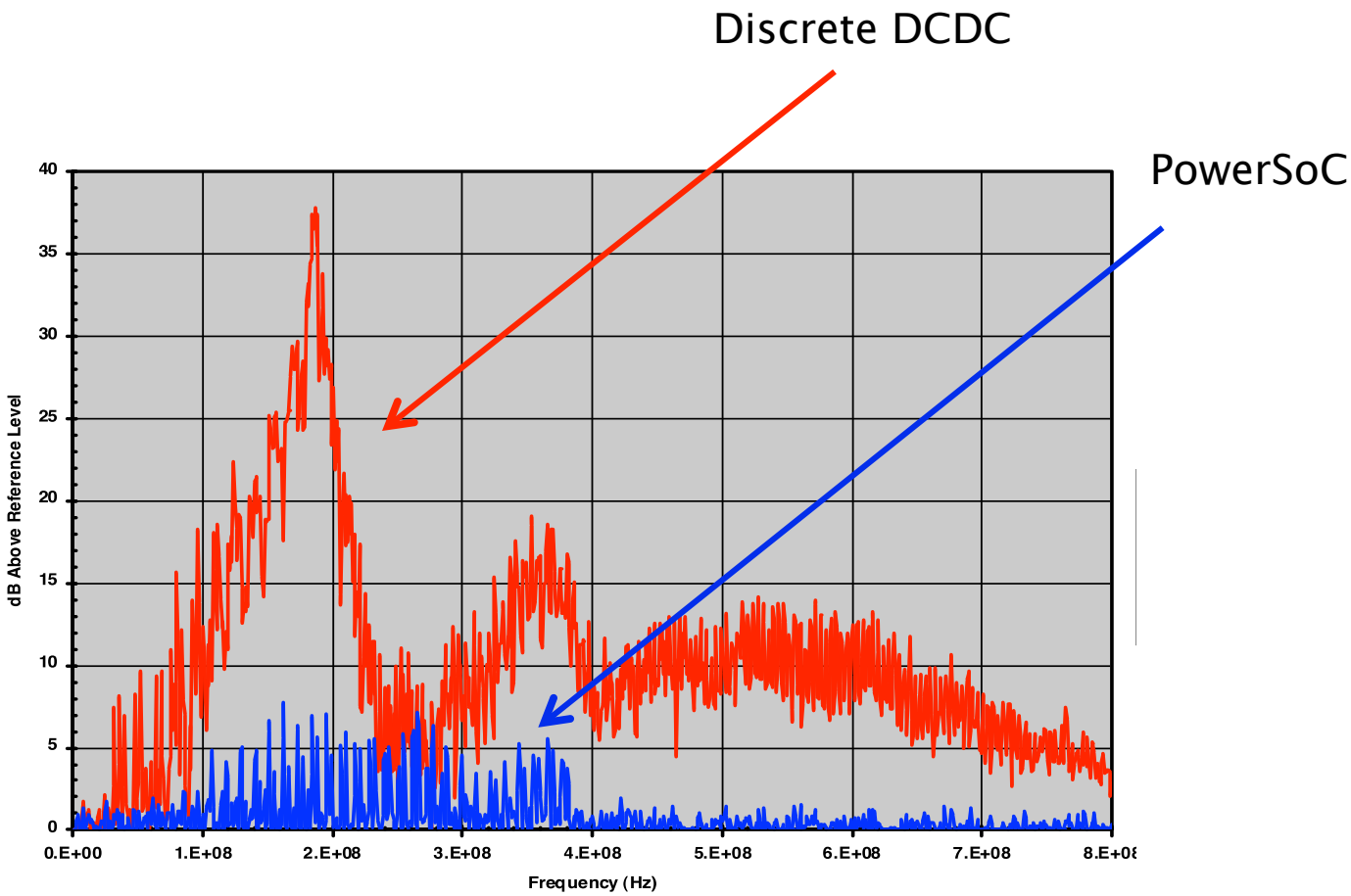
PowerSoC CISPR 22 Class B Charts

3A PowerSoC

4A PowerSoC

Conducted Noise Revisited

- PowerSoC vs Discrete DCDC



Common mode voltage measured on input ground terminal

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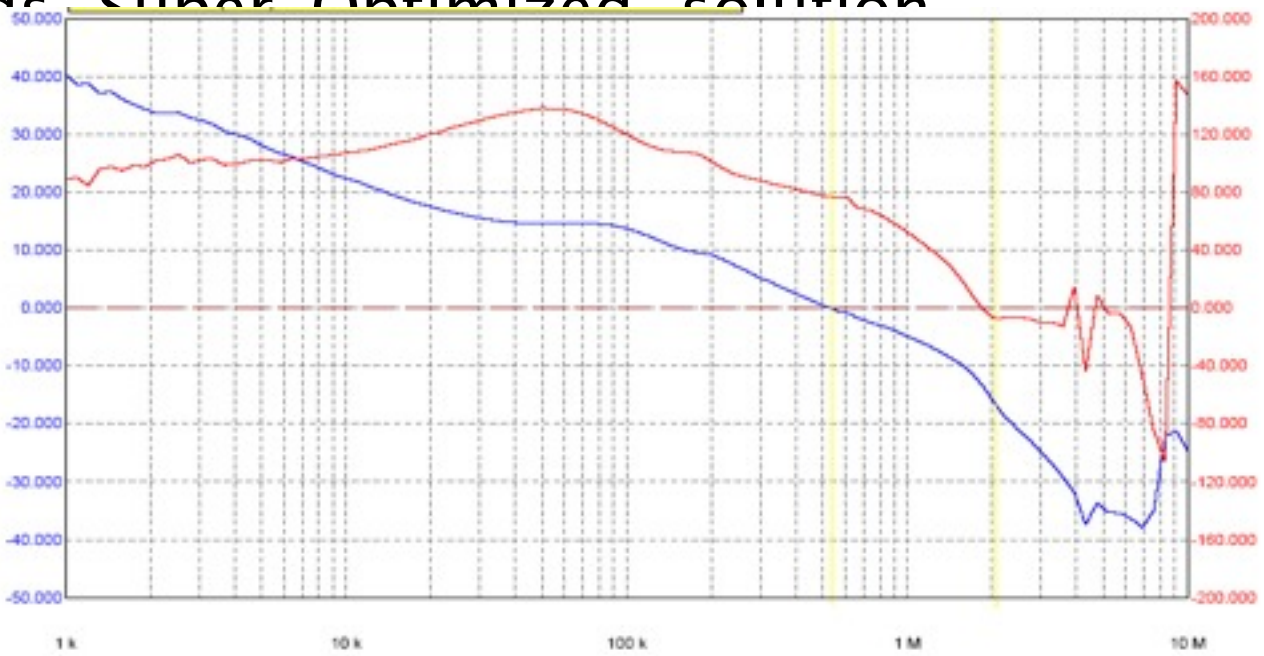
PowerSoC: Stable, Optimized Performance

- Inductor is fully characterized over entire operating range
- Compensation network is matched to the inductor
- Yields "Super Optimized" solution



	M1	M2	M2 - M1
Frequency	539.31 kHz	2.08 MHz	1.54 MHz
Magnitude	-0.149 dB	-16.846 dB	-16.696 dB
Phase	76.833 deg	-7.000 deg	-83.834 deg
Ref (Mag)	0.000 dB	0.000 dB	0.000 dB
Ref (Phase)	0.000 deg	0.000 deg	0.000 deg
Delta (Mag)	-0.149 dB	-16.846 dB	
Delta (Phase)	76.833 deg	-7.000 deg	

- **BW = 540 KHz**
- **Phase Margin = 76.8 Deg**
- **Gain Margin = 16.8 dB**

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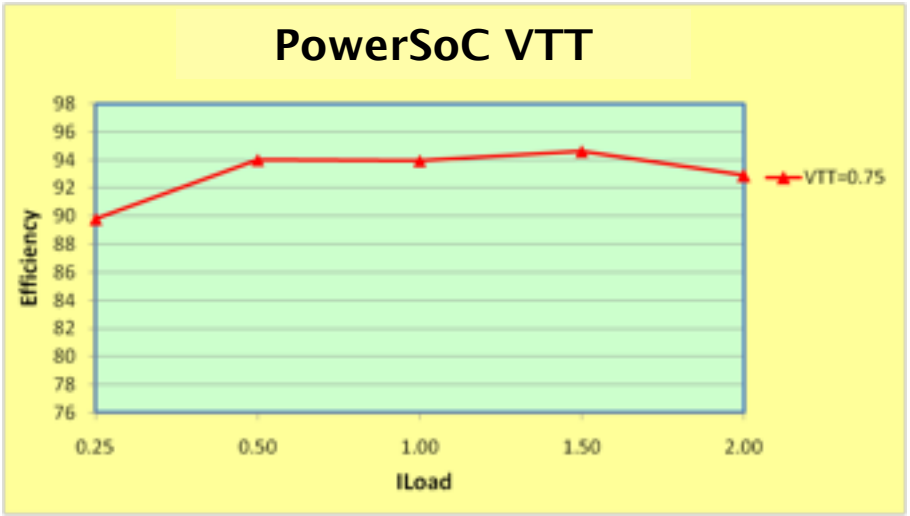
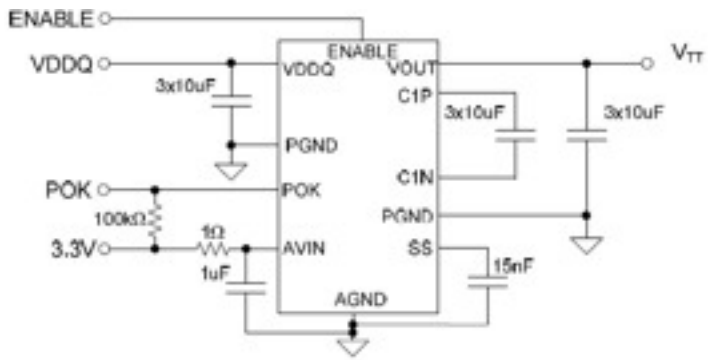
- Enpirion Layout Files available for easy CAD integration

Memory Termination: PowerSoC





	EV1330	Linear VTT
Total Solution Size (mm²)	80	88
Efficiency at TDC	95%	50%
Power Loss	0.06W	0.9W
	0.84W	

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PowerSoC Solves Many SSD DCDC Issues

- Very small footprint
- Low part count/fewer placemer
- Low ripple, low EMI
- High efficiency
- Fast transient response
- Up to 10x higher reliability
- Ease of design for fast TTM