Session 102: SSD Benchmark Testing

Tuesday, August 09, 2011
8:30 am - 9:50 am

FMS Program Organization

Eden Kim, Organizer

July 14, 2011

Rev 0.3

Logistics

- FMS – August 9 – 11, 2011
- Venue – Santa Clara Convention Center
- Day – Tuesday, August 09, 2011
- Time – S102 8:30 am – 9:50 am
- Topic – S102 Benchmark Testing Panel
- Participant Slots – (6) Panelists
- Presentation Time – Panelists 10 min ea followed by panel Q&A
- Organizer – Eden Kim, edenkim@calypsotesters.com

Panelists - Session 102

S102 8:30 am – 9:50 am

8:30 – 8:40: Introduction - Eden Kim

8:40 – 9:40: Speakers (5 – 10 minutes, try for 7 to leave more Q&A time)

- **8:40 – 8:50: Doug Rollins, Micron**
- **8:50 – 9:00: Harry Pon, Intel**
- **9:00 – 9:10: Andrew Ku, Tom's Hardware**
- **9:10 – 9:20: Shirish Jamthe, Virident**
- **9:20 – 9:30: Chuck Paridon, HP**
- **9:30 – 9:40: Easen Ho, Calypso**

9:40 – 9:50: Audience Questions

Panelist Information

Speaker Name	Company Title	Introductory Bio
Doug Rollins	**Snr Applications Eng Enterprise SSDs**	Doug Rollins joined Micron in 2009 as an applications engineer with the Enterprise SSD Products group. Prior to joining Micron, Mr. Rollins spent 13 years working in server system, network appliance, and storage platform/data protection design and manufacture. Mr. Rollins is the named inventor in 13 U.S. patents and has been recognized by both the Storage Networking Industry Association (SNIA) and Intel Corporation for outstanding technical achievement. Mr. Rollins is an active member of several technical groups within SNIA including: The Solid State Storage Initiative and its Technical Working Group; Data Protection and Capacity Optimization; Marketing and Technical Development; Total Cost of Ownership; and the IO and Trace Tools Analysis. As co-chair of SNIA's Solid State Storage Initiative's Technical Working Group, Mr. Rollins was instrumental in the early development and validation of SNIA's SSD Performance Test Specification. Mr. Rollins earned his BA degree in mathematics from Humboldt State University.
Harry Pon	**Intel Corp.**	rry Pon is a Senior Staff Development Engineer in the NVM Solutions Group at Intel Corporation where he has been involved with flash product design, product development, and integrating NAND flash into the Intel Architecture PC platform in the form of SSDs and NVM Caches for the past 24 years. He served on the "VLSI Symposium" technical program committee for 7 years, authored and co-authored several journal papers, has been awarded seven patents with additional patents pending. Harry received a BSEE degree in semiconductor processing and device physics from the University of California, Davis and MSEE degree in integrated circuit design from San Jose State University. He continues his post graduate education with the Summer Education Program at the Massachusetts Institute of Technology, MIT, Cambridge, MA. He is a *Senior* Member of IEEE in the "IEEE Solid-State Circuits Society", "IEEE Electron Devices Society", and the "IEEE Nanotechnology Society".
Andrew Ku	**Tom's Hardware** **Senior Editor** **xxx@bestofmedia.com**	Andrew is a technology journalist for Tom's Hardware. In addition to product evaluations, he is responsible for sheparding the development of performance benchmarks and testing protocols. Andrew earned his BA in Economics and BS in Evolutionary Biology at the University of Texas. He research focuses on computational models of predictive behavior.

Panelist Information

Speaker Name	Company Title Email Tel	Introductory Bio
Shirish Jamthe	**Virident** **Global Director of Sales Engineering**	
Chuck Paridon	**HP** **Storage Performance Architect** chuck.paridon@hp.com **916-785-5155**	Chuck is 24 year veteran in computer system and storage subsystem benchmark development and performance analysis. He is currently responsible for the development and delivery of Hewlett-Packard Storage Performance collateral in the form of field performance troubleshooting training, efficient storage technology deployment and pre-sales consulting. He is a member of the SNIA Solid State Storage Technical Workgroup, the SNIA Green Storage Technical Workgroup and the Storage Performance Council. Chuck has earned a BS in Mechanical Engineering from the the University of Akron, Oh. as well as an MS in Computer Science from California State University, Chico.
Easen Ho	**Calypso** **CTO** **eho@calypsotesters.com**	Dr. Ho is the CTO of Calypso Systems, Inc. and has been a principal architect of the recently released SNIA Solid State Storage Performance Test Specification. Dr. Ho has been intimately involved in the development of performance benchmarking for NAND Flash based solid state storage devices. Dr. Ho received his doctorate in laser physics from MIT and his BSEE from the Tokyo Institute of Technology. Dr. Ho previously was founder, CEO and CTO of digital papyrus, inc. a laser optical mass storage technology firm.

Panelists - Session 102

Summary of Session

- **Each Speaker will have a 5-10 minute oral presentation**
  - **Introduction by Organizer (please submit BIO and requested intro)**
  - **PPTX slides are allowed**
- **Subject matter: SSD Performance Testing**
  - **Can focus on either Enterprise of Client testing**
  - **Will coordinate blurbs among presenters**
- **Panel Discussion follows – 10 – 20 Minute Q&A led by Moderator – prepared questions and questions from audience. See Next Slide for Questions**

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Questions for Q & A

Introductory Statement by Chair:

SSD Performance Benchmarking is being conducted at different levels: Synthetic Device Level tests, Application/File System tests, IO Trace based workload tests.

This Panel will discuss the advantages / disadvantages and the pros / cons of these approaches and what the future may hold for SSD Performance Benchmarking.

Sample Questions:

1. *What role does performance testing have in the development, mfg and sale of SSDs?*
2. *What is your preferred performance benchmark methodology, why do you use it, what are its advantages?*
3. *What are some of the critical issues facing SSD performance testing going forward?*
4. *Who is your audience for performance testing and what are their key issues?*
5. *What is the difference, advantages & disadvantages between using synthetic device level tests (such as the SNIA PTS), application based tests (such as SPC and PCMark), and IO Trace based methodologies (such as Intel and Tom's Hardware)?*

- Thank You for your Participation!
- Presenter Slides are attached.

- Questions? – contact Eden Kim edenkim@calypsotesters.com or Lance Leavanthal lanclev@pacbell.net