
# HLNAND2 DDR800 Arrives

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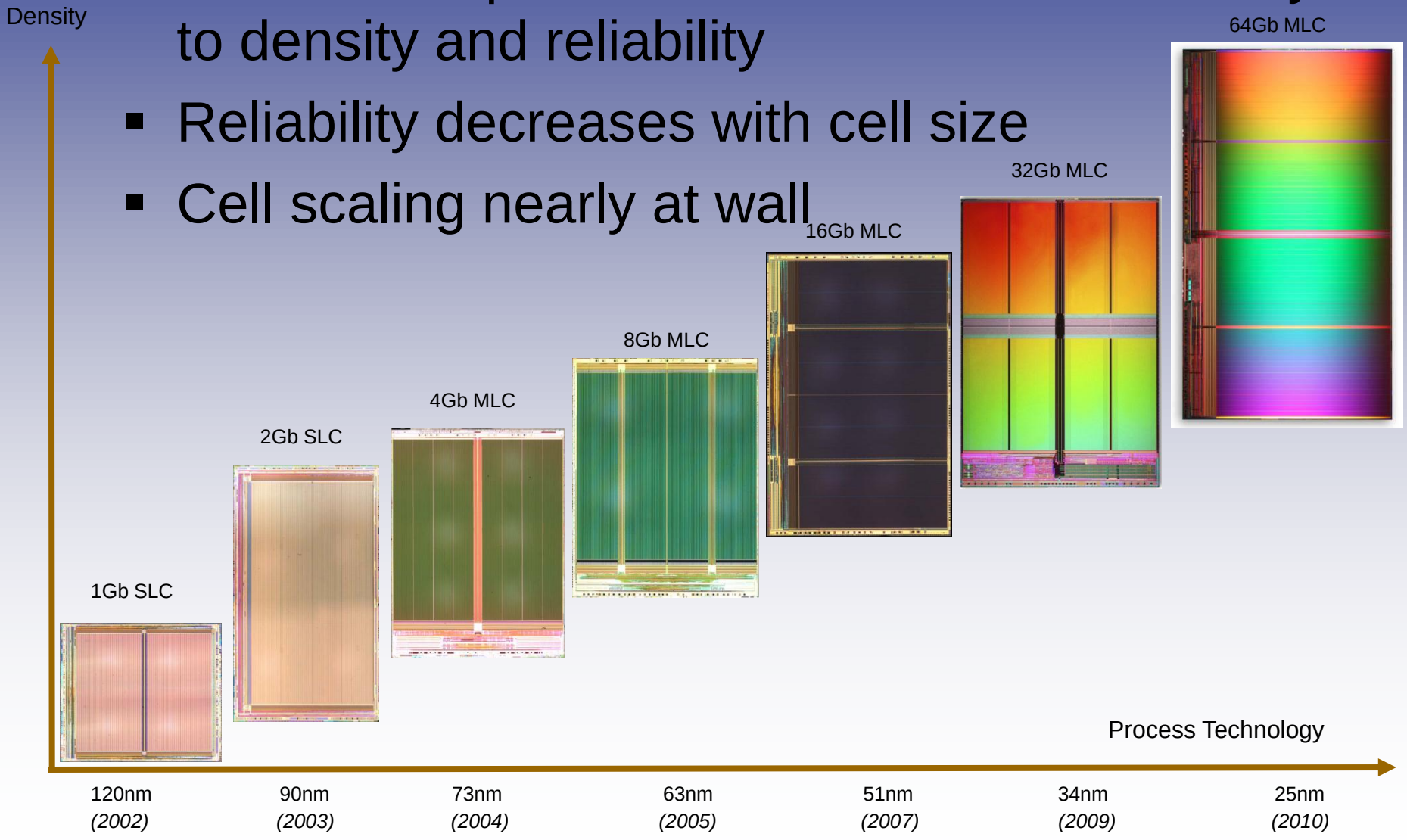
Flash Memory Summit 2011
Santa Clara, CA

# Scaling History

- Vendor and product differentiation tied mainly to density and reliability
- Reliability decreases with cell size
- Cell scaling nearly at wall



# Nearly at Scaling Wall, What Next?

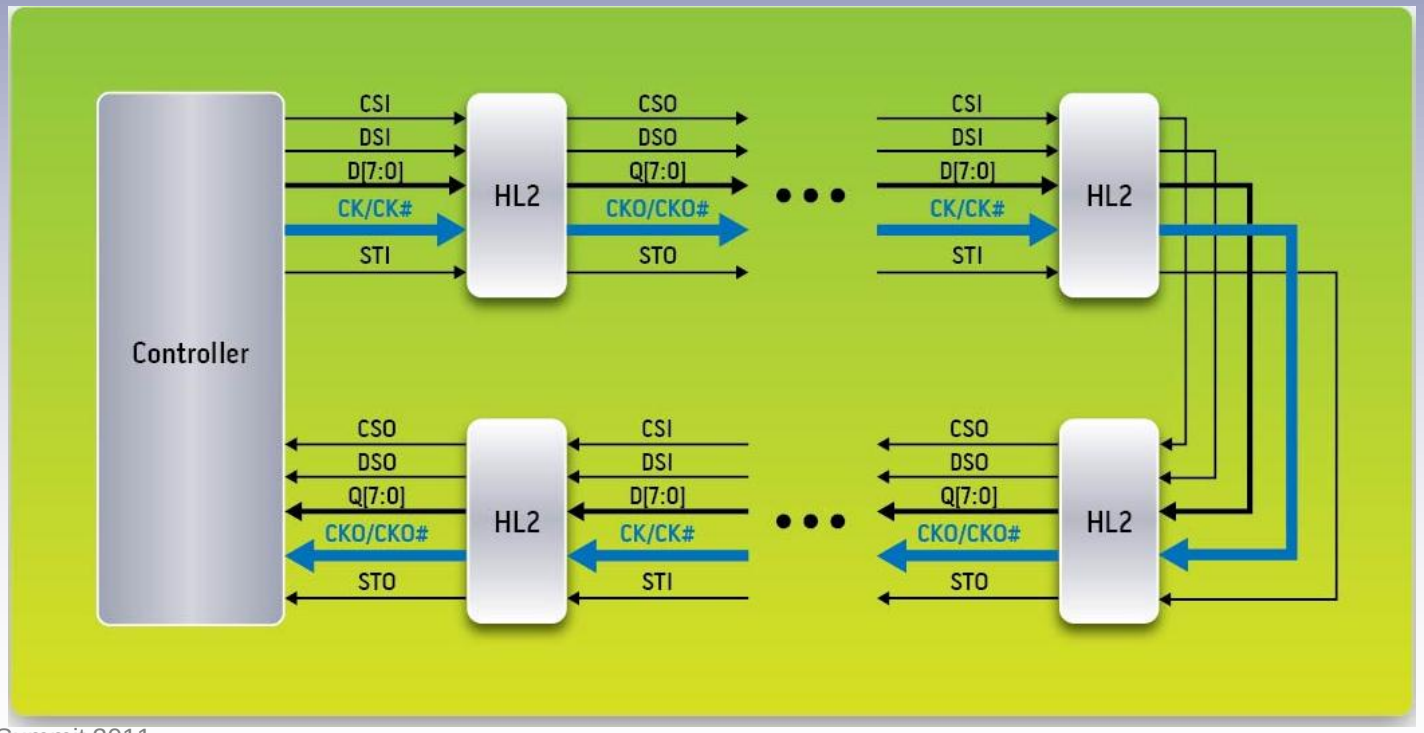
- How will Flash producers make a compelling story at the wall?
- Reliability will still play a differentiating role
- Feature enrichment and performance improvements will also help distinguish products and serve product niches

# Feature Rich Interface Chip Lights the Way

- Load buffering
- Higher transfer rates
- Higher capacity per channel
- Built-in ECC
- Localized page copy
- Relieves IO congestion in mobile platforms
- Consolidated mixed memory types

# HLNAND2: First DDR800 NAND Flash Device Arrives

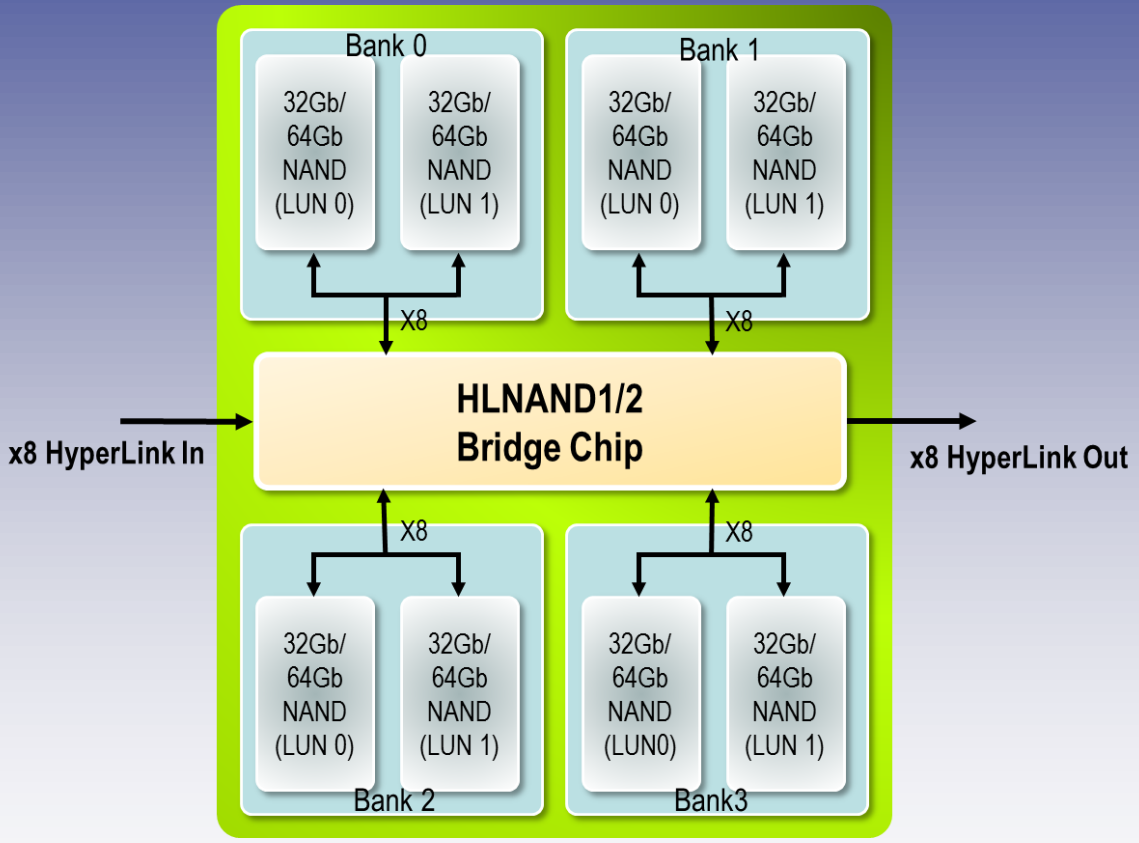
- 1.2V interface achieves up to DDR800
- Source synchronous clocking
- DuplexRW™ doubles throughput, upto 1.6 GB/s

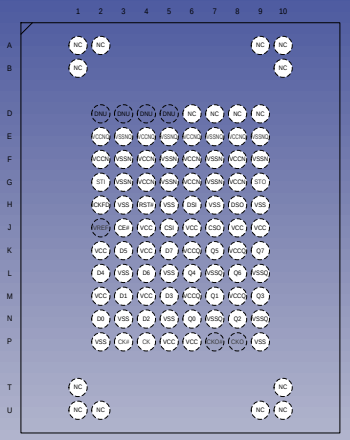


# HLNAND2 Features

- DDR533 / DDR667 / DDR800
- JEDEC 1.2V HSUL_12 Interface Signaling
- Source Synchronous differential clock
- No On-Die Termination (ODT)
- Four bank architecture
- Fully independent 8 die operation
- Built-in EDC (Error Detection Code)
- DuplexRW™: Simultaneous DDR800 read & write, effectively 1600MB/s data throughput
- Independent, automatic status bus

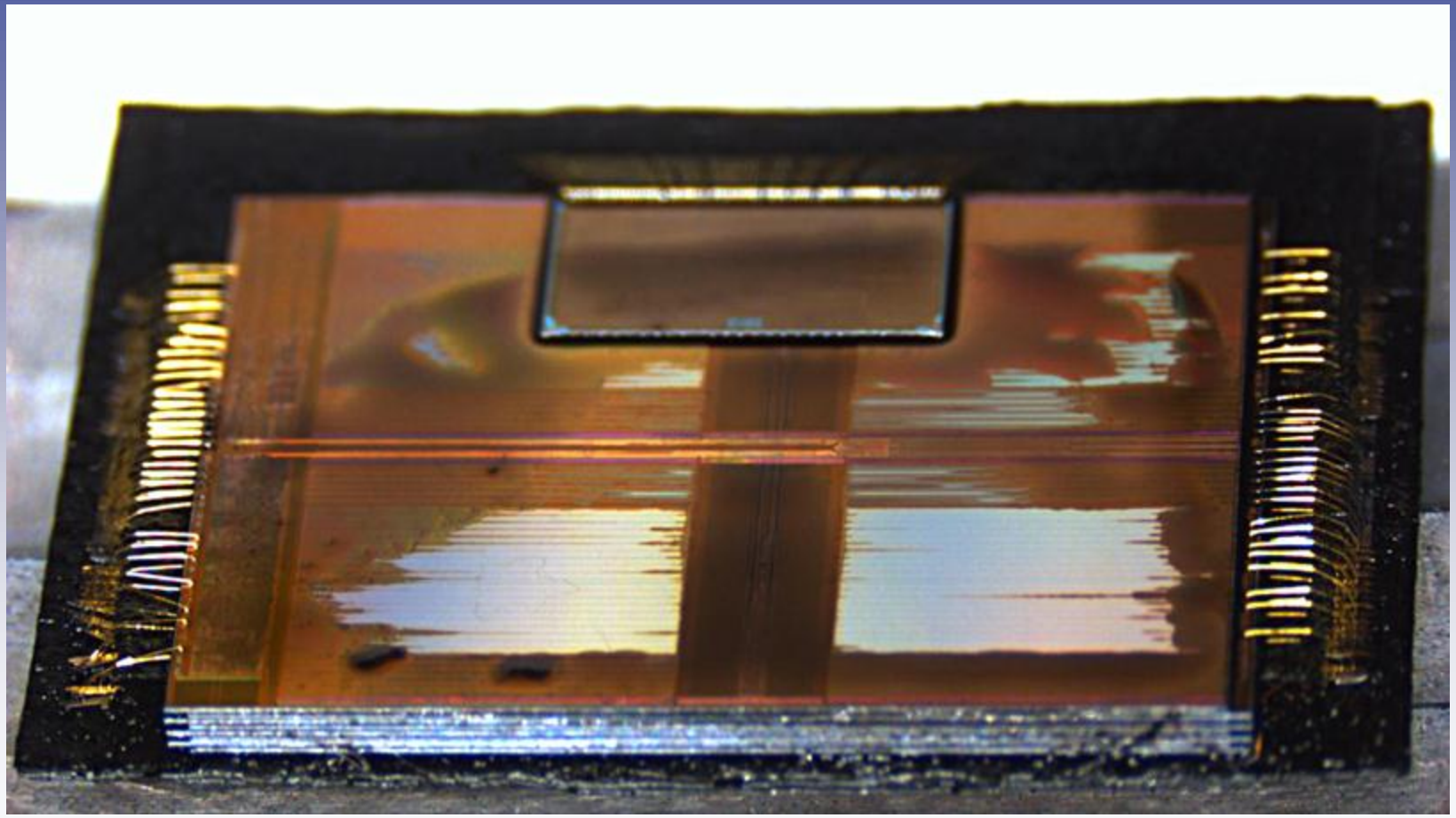
# 256Gb MLC HLNAND2 MCP



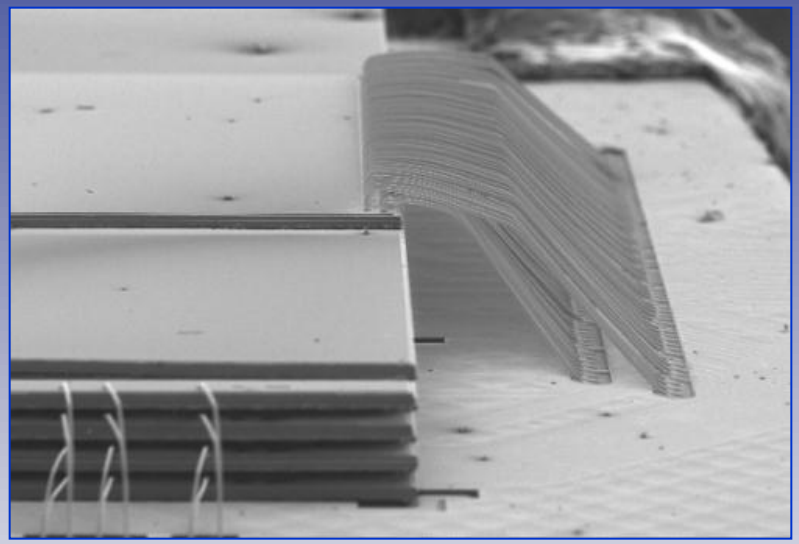



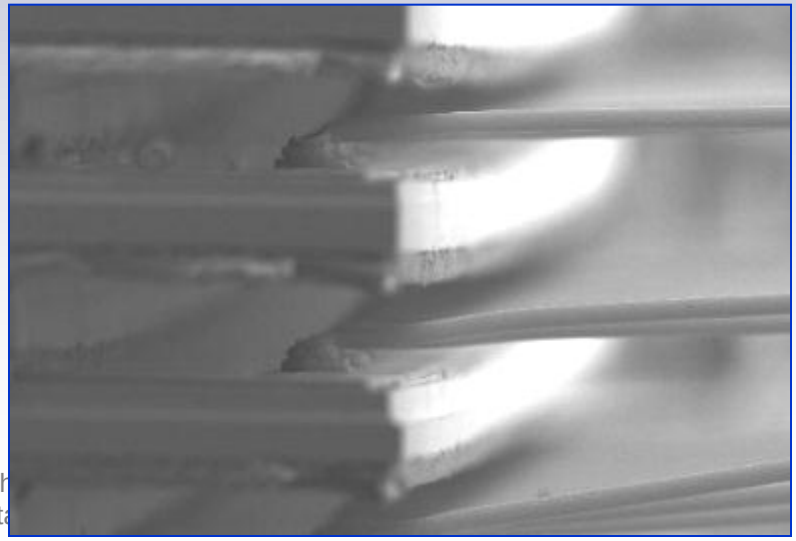
100-Ball BGA (18mm x 14mm)

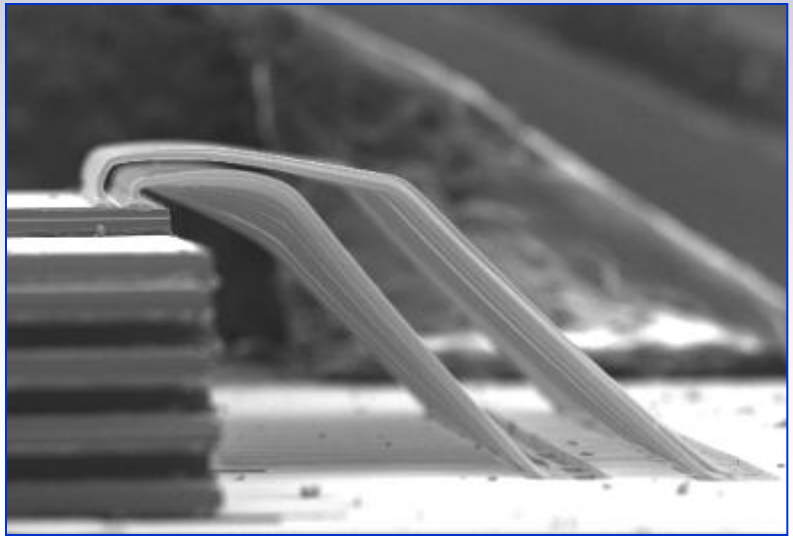
# Inside the MCP lies a 9-Die Stack



# SEM of 9-Die Stack

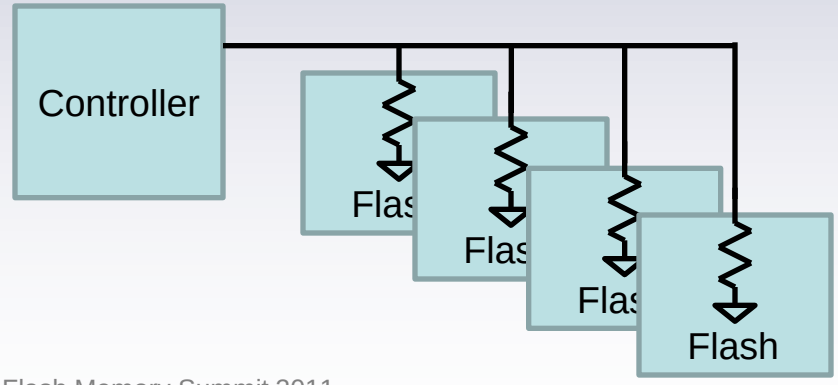


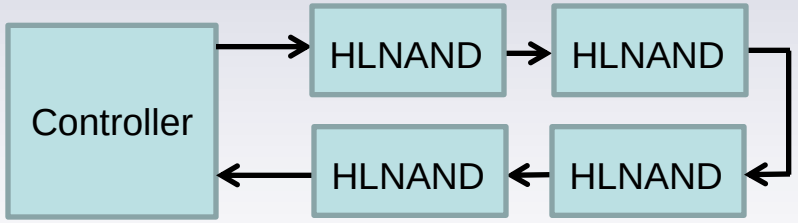




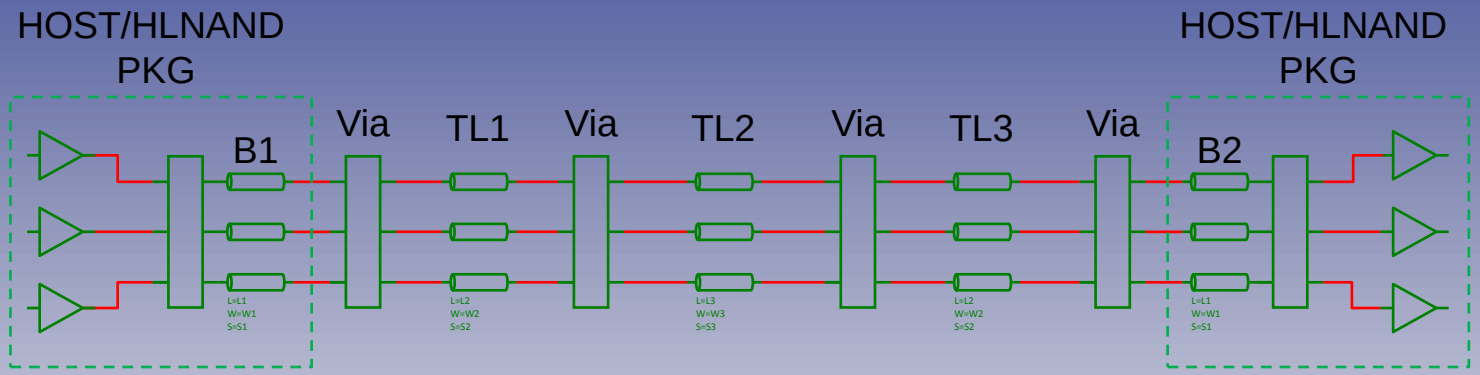
# HLNAND2: High Speed, no ODT

- Parallel-bus flash requires power hungry ODT beyond 200MT/s
- HLNAND2 needs no termination, even at 800MT/s
- Point-to-point topology is logical choice at higher transfer rates



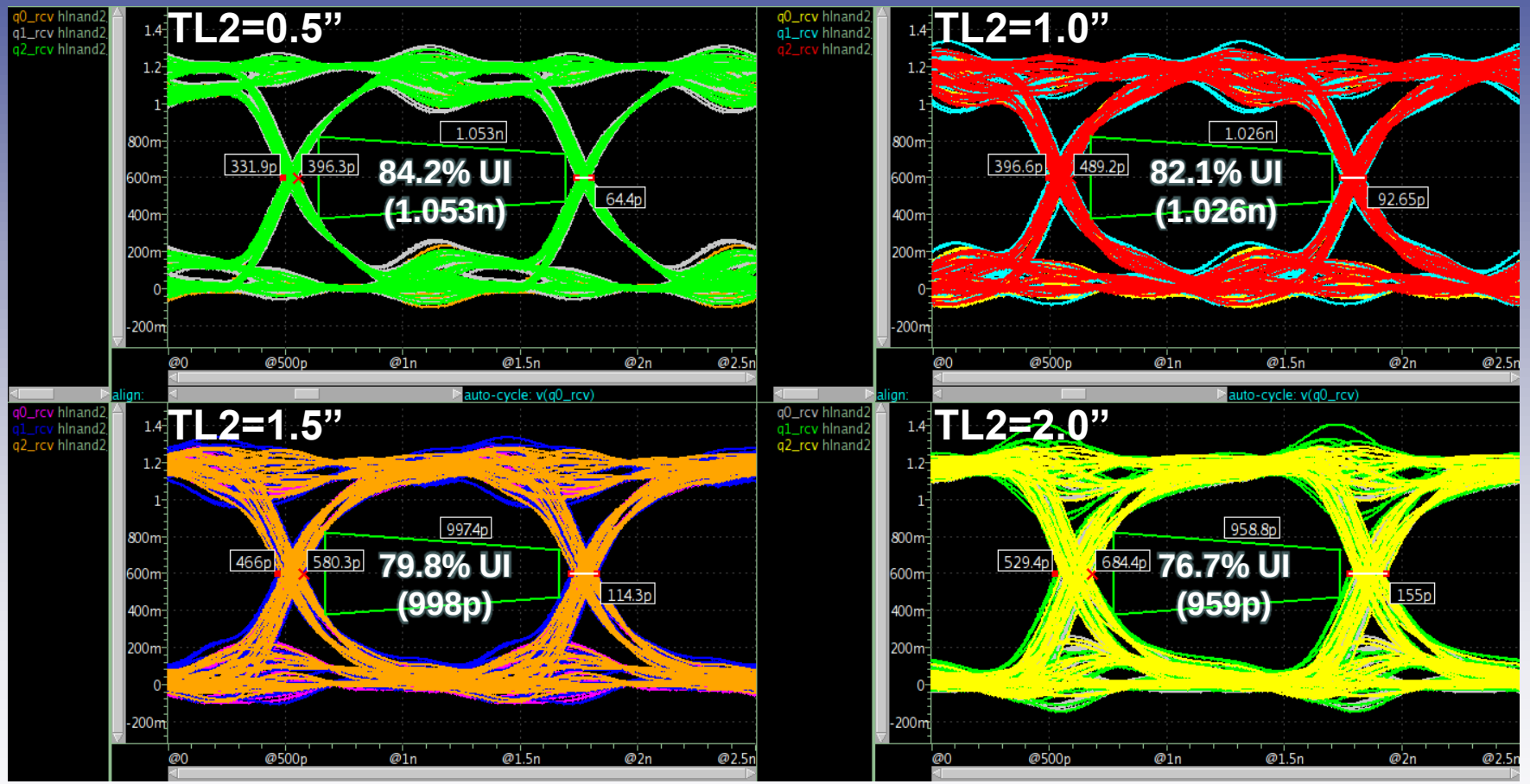



# DDR800 HLNAND2 Signal Integrity (General Topology Model)

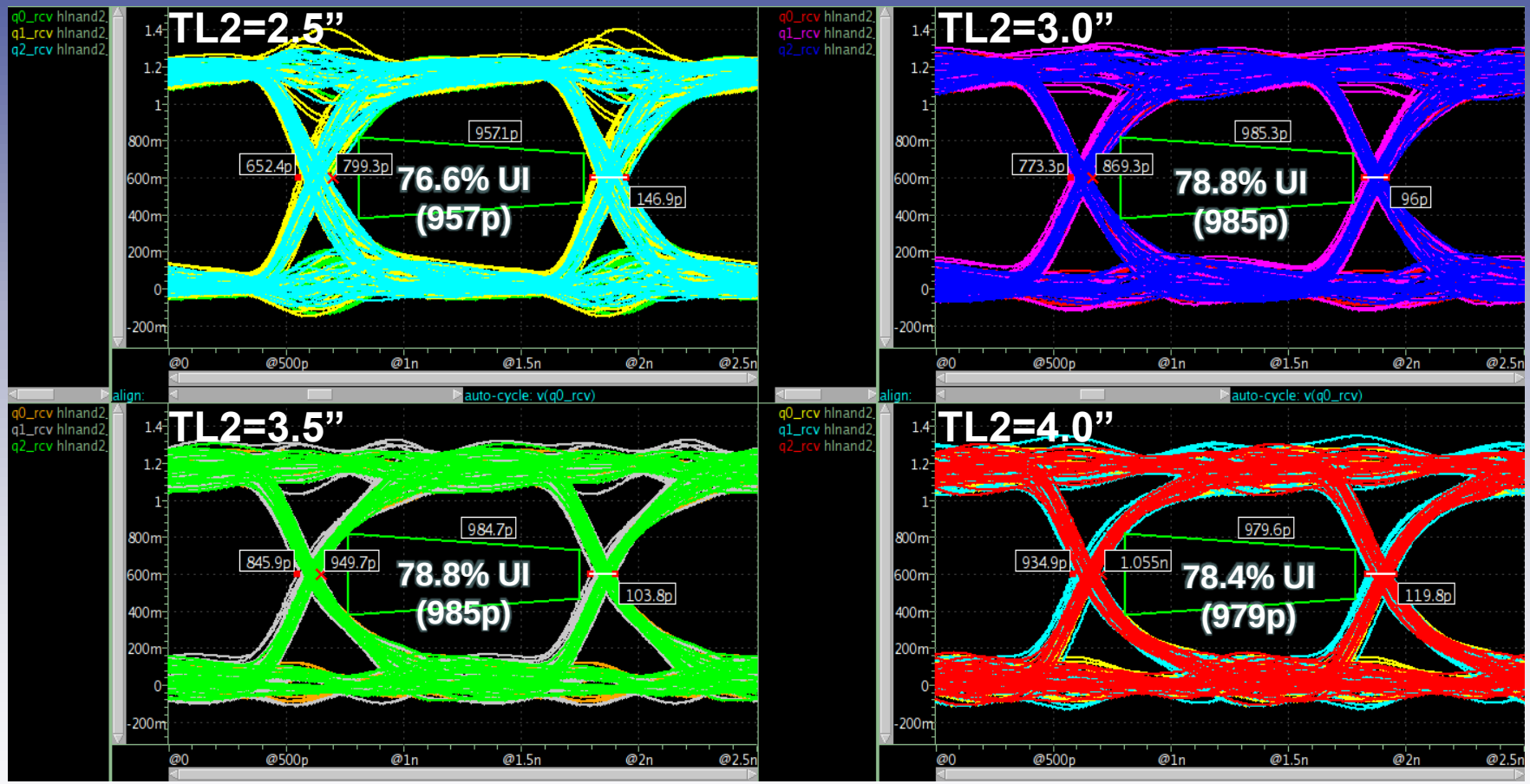



- PCB Impedance = 50 Ω ± 7.5 Ω
- Space of Lines = 4/8 mil = 101.6/203.2 μm
- X-talk = 3 Line Model
- Min. time width of RCV eye window = 0.66UI
- Driver Strength = 50 Ω / 33 Ω
- ODT = Not Required

# DDR800 HLNAND2 Signal Integrity (Eye Diagram, 0.5” - 2.0” trace length)

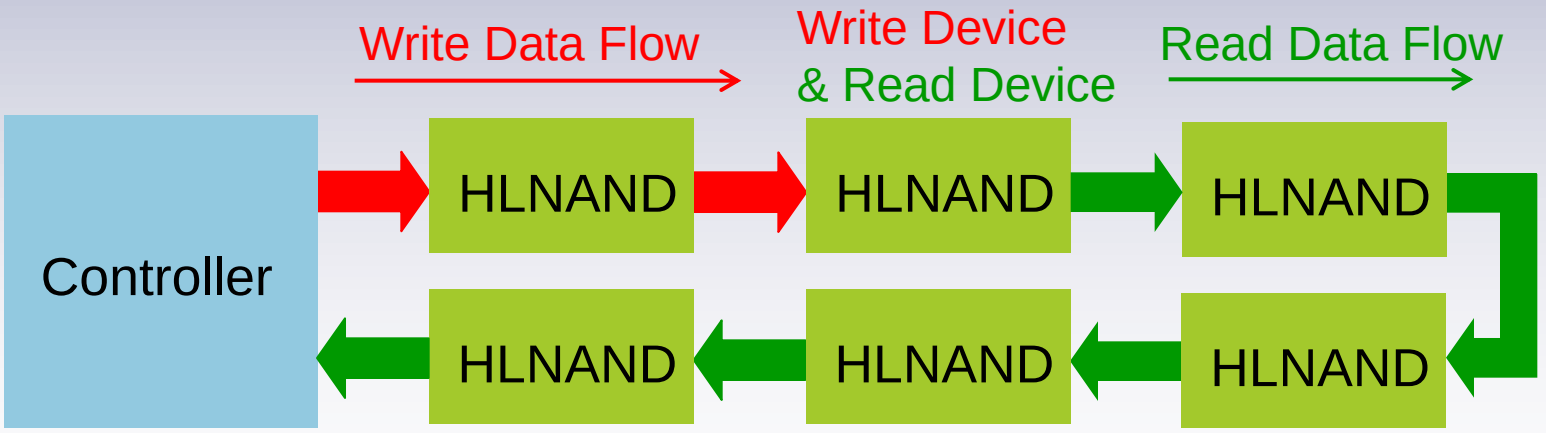


# DDR800 HLNAND2 Signal Integrity (Eye Diagram, 2.5” – 4.0” trace length)



# Enabling DuplexRW

- DuplexRW doubles throughput to 1600MB/s
- Write and read on ring simultaneously
- Write & Read same device on ring



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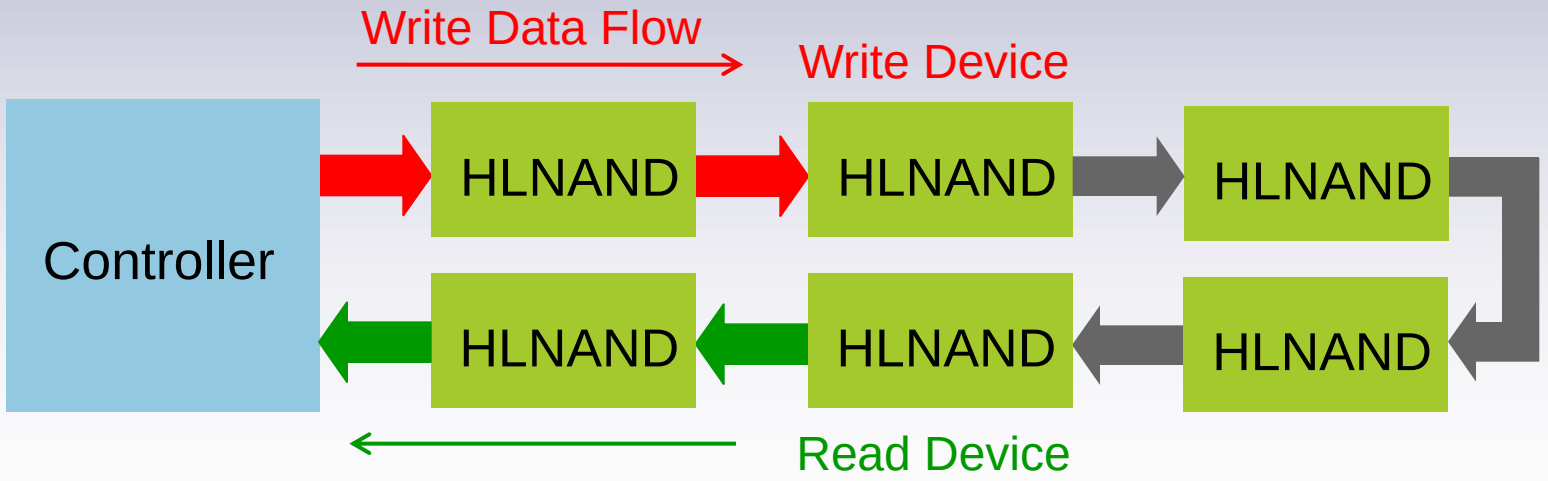
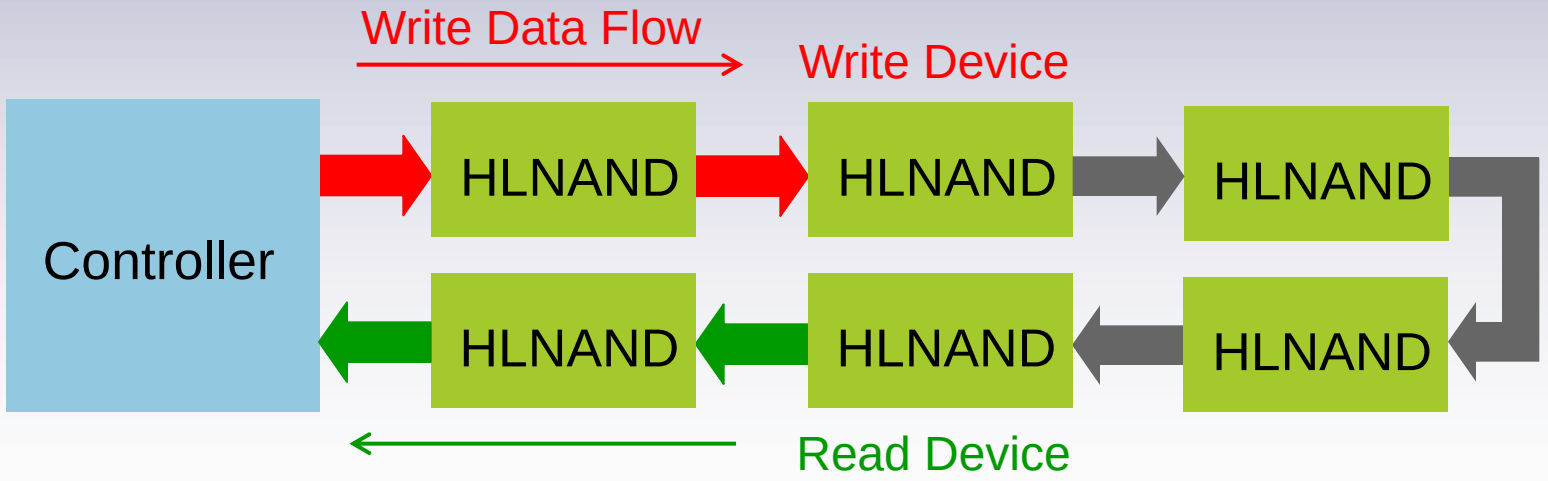
- Write & Read same device on ring
- Read device downstream from write device



# Enabling DuplexRW

- DuplexRW doubles throughput to 1600MB/s
- Write and read on ring simultaneously
- Write & Read same device on ring
- Read device downstream from write device
- Can use DuplexRW 50% of the time

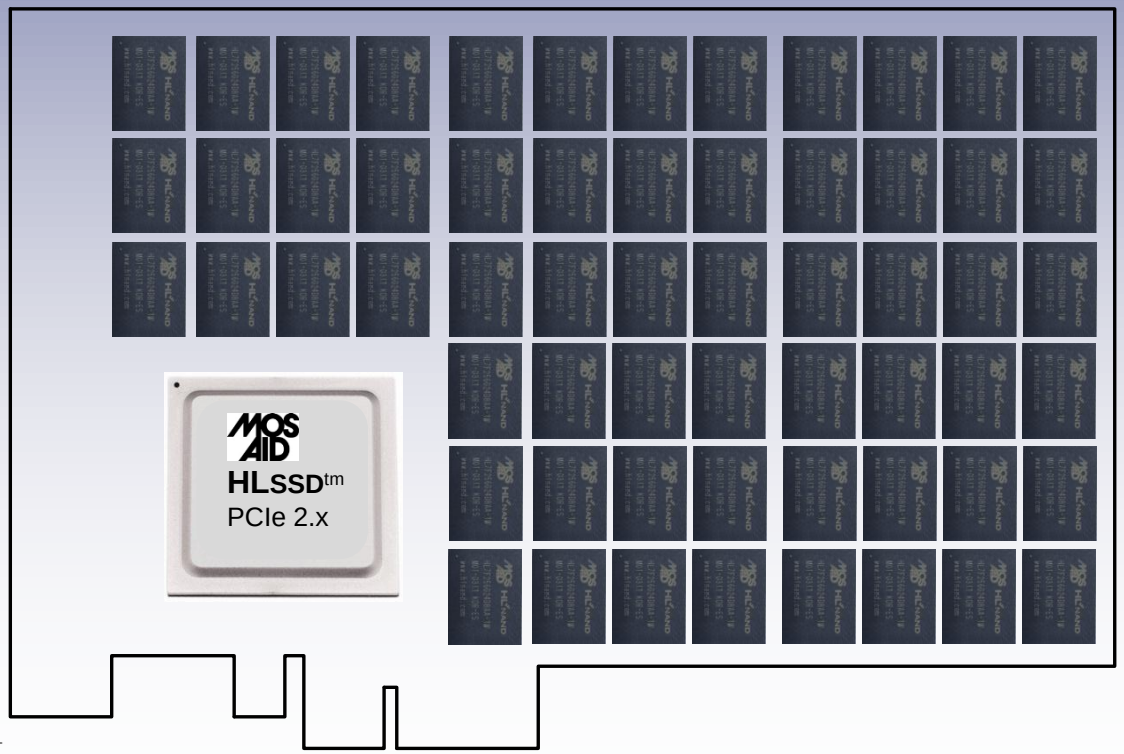


# High-Speed NAND Comparisons

| | HLNAND2 | HLNAND | ONFI 3.0 | Toggle Mode 2.0 |
|---|---|---|---|---|
| Synchronous I/O | Yes | Yes | Yes | No (Pseudo Sync) |
| Clock Speed | 400MHz | 133MHz | 200MHz | 200MHz (DQS) |
| Transfer Rate (Duplex RW) | 800MT/s 1600MT/s | 266MT/s 533MT/s | 400MT/s N/A | 400MT/s N/A |
| I/O Voltage | 1.2V | 1.8V | 1.8V | 1.8V |
| # of Chips before Roll-off | 255 | 255 | 8 | 8 |
| Termination | No | No | Yes | Yes |

# PCIe HLSSD™ Prototype

- Native PCIe SSD Controller (ASIC/FPGA)
- X4 or x8 PCIe V2.0
- TB Capacity & GB/s-Class Performance



# Summary

- Flash vendors offering faster flash IO as they approach the scaling wall
- Interface chip enables product differentiation through feature enrichment and faster interface
- HLNAND2 provides 800MB/s/ch. transfer rate with no ODT
- HLNAND provides high capacity at any performance level

**HLNAND2 with Interface chip lights the way…**

# Resource for HLNAND Flash

## www.HLNAND.com