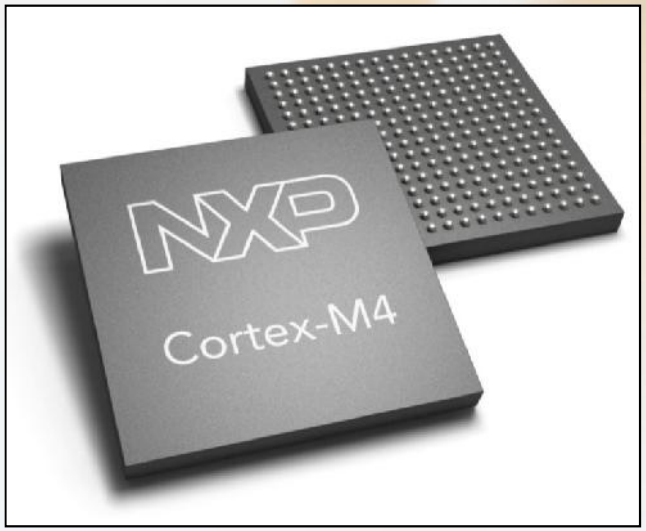
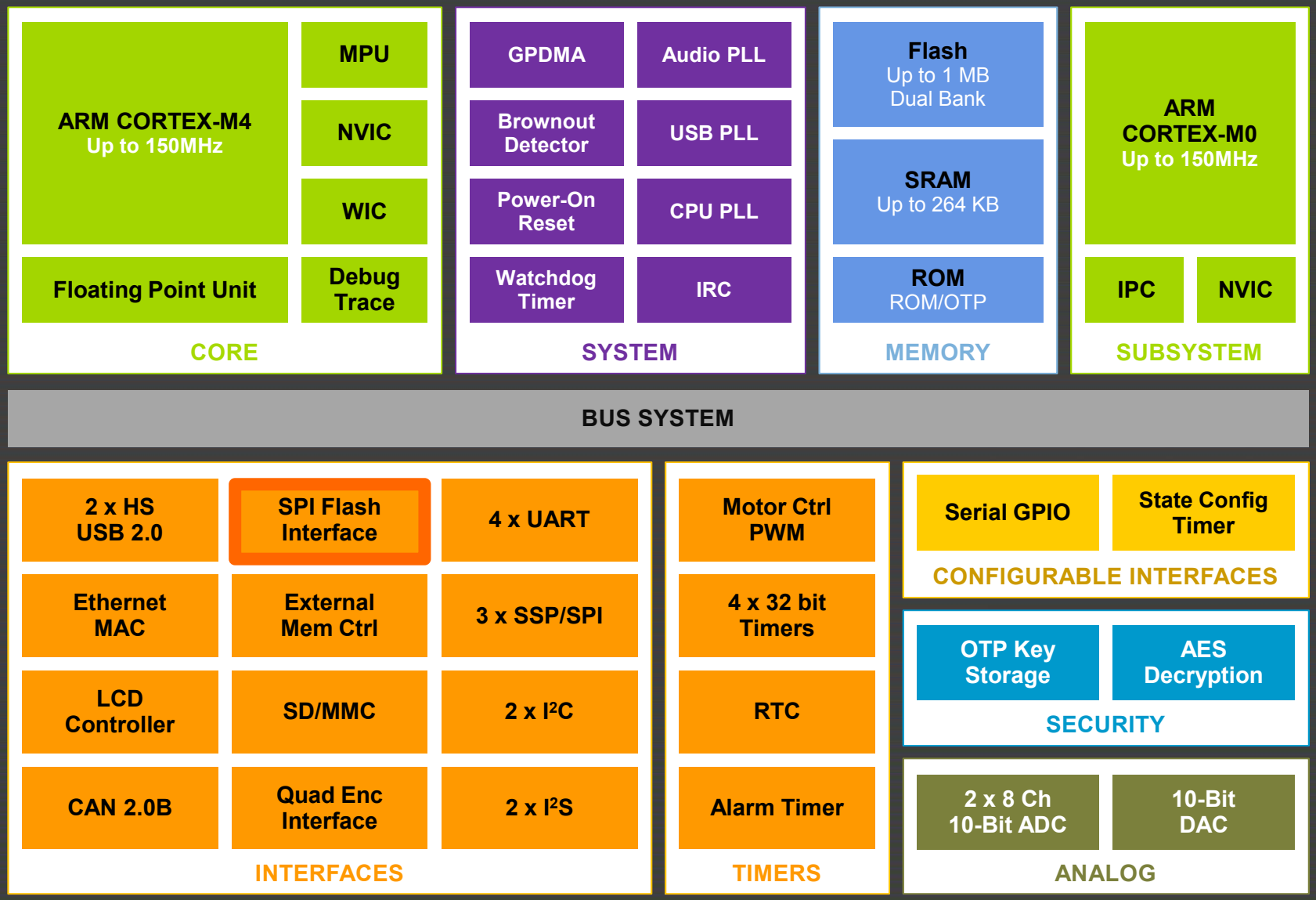


Quad SPI Flash: Benefits and Uses in General Purpose Microcontrollers

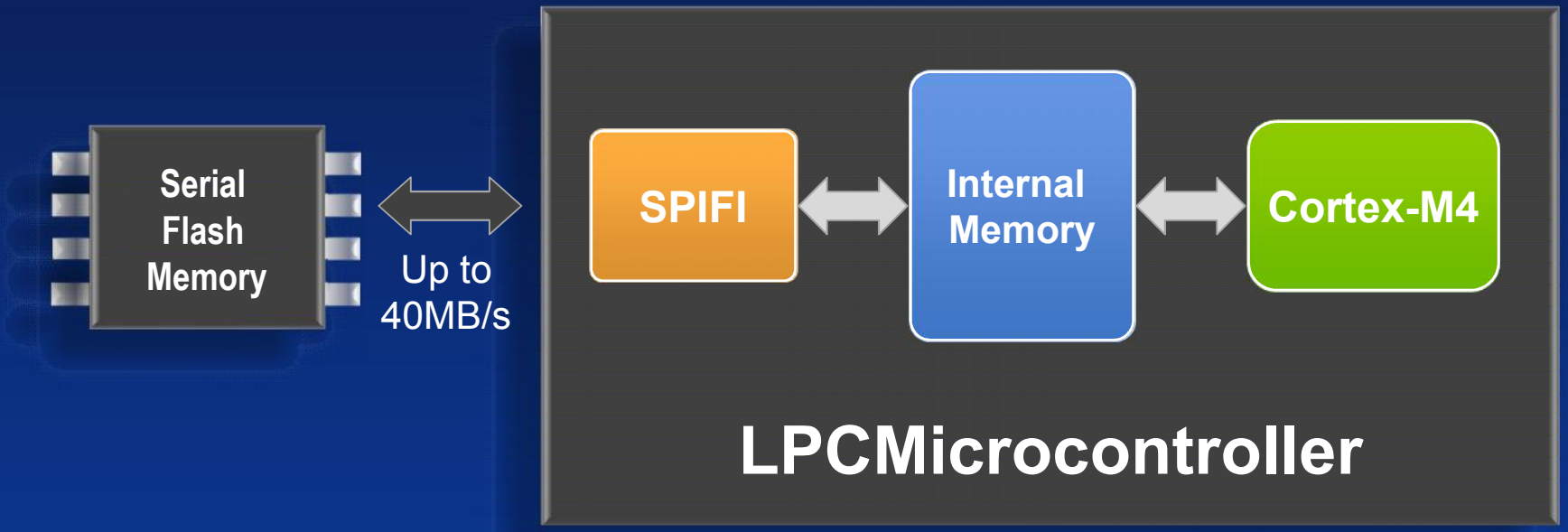
NXP Semiconductors
BL Microcontrollers
San Jose CA
October 2010

LPC4300: SPI Flash Interface



SPIFI – Overview

SPI Flash Interface



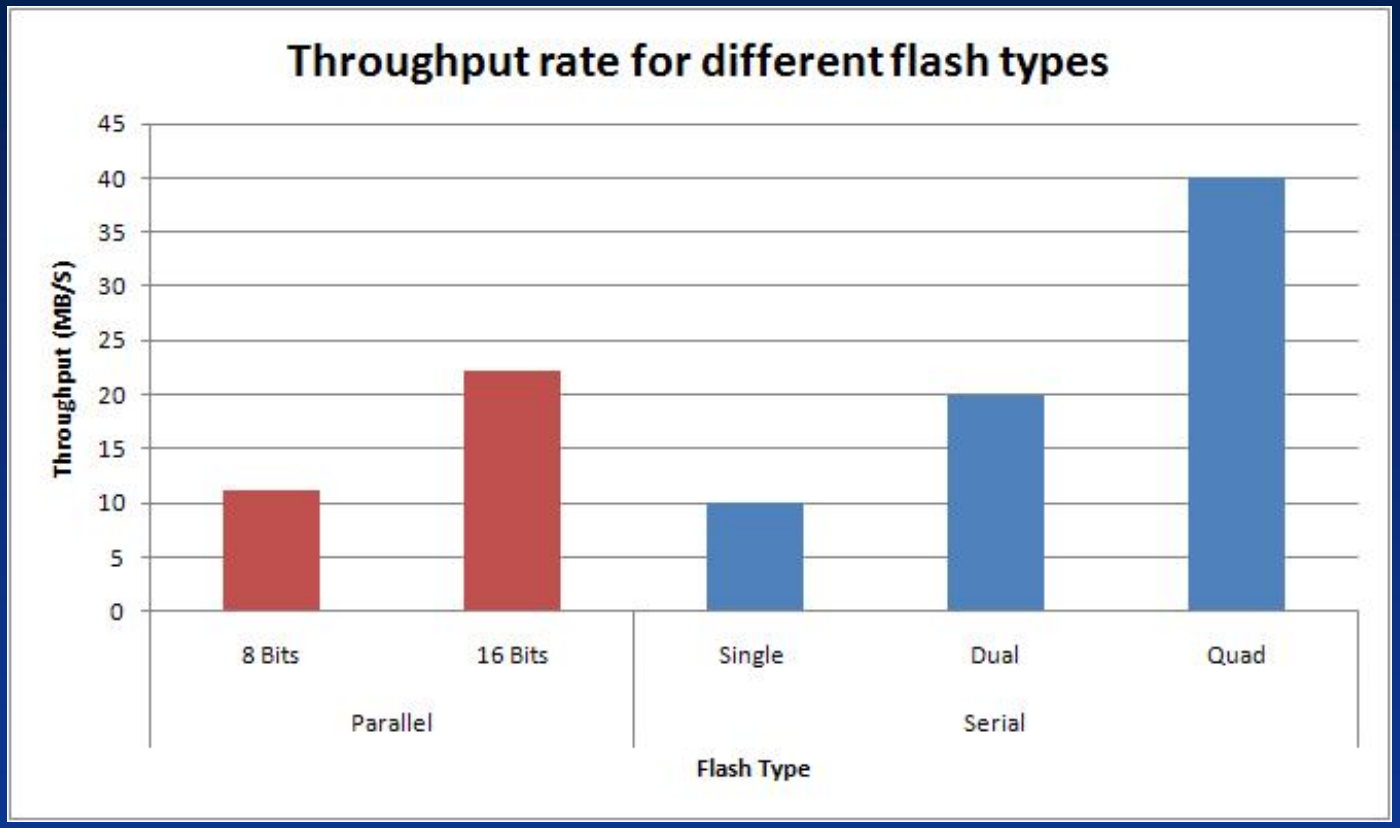
Unique NXP feature that maps low-cost serial flash memories into the internal memory system.

SPIFI – Quad SPI Flash Interface

- What is Quad SPI?
  - A couple of years ago, PCs started using Quad-SPI Flash for loading BIOS. The high PC volumes forced prices down to low levels
  - Advantages: High speeds, small packages/few pins, low cost
  - Disadvantages: Not supported by standard MCUs – UNTIL NOW!

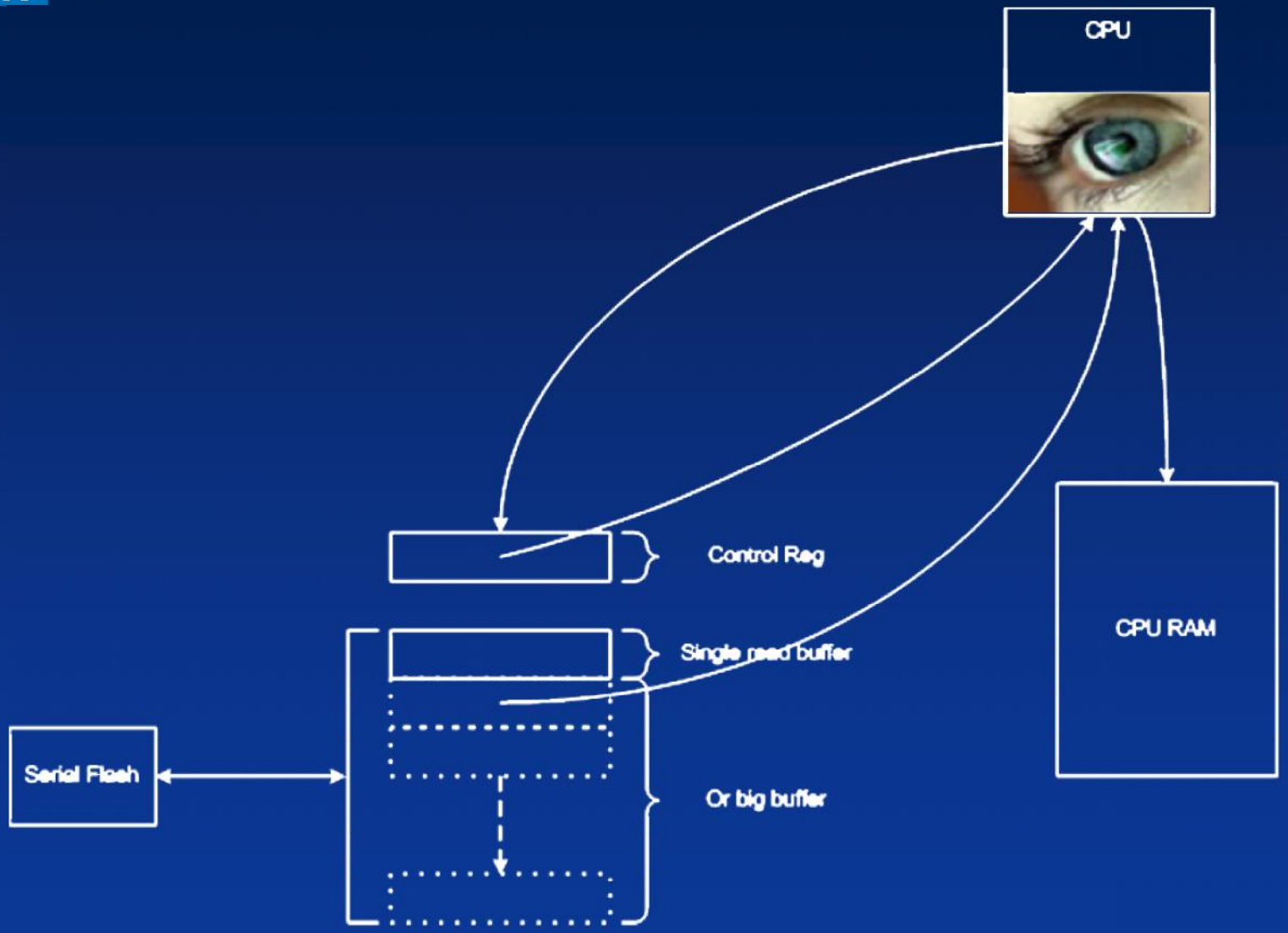
- SPI Flash Interface uses either 4 or 6 lines
  - Standard SPI flash uses CLK, CS, MISO and MOSI
  - Quad SPI flash uses CLK, CS IO0, IO1, IO2 and IO3

External Flash Performance Comparison

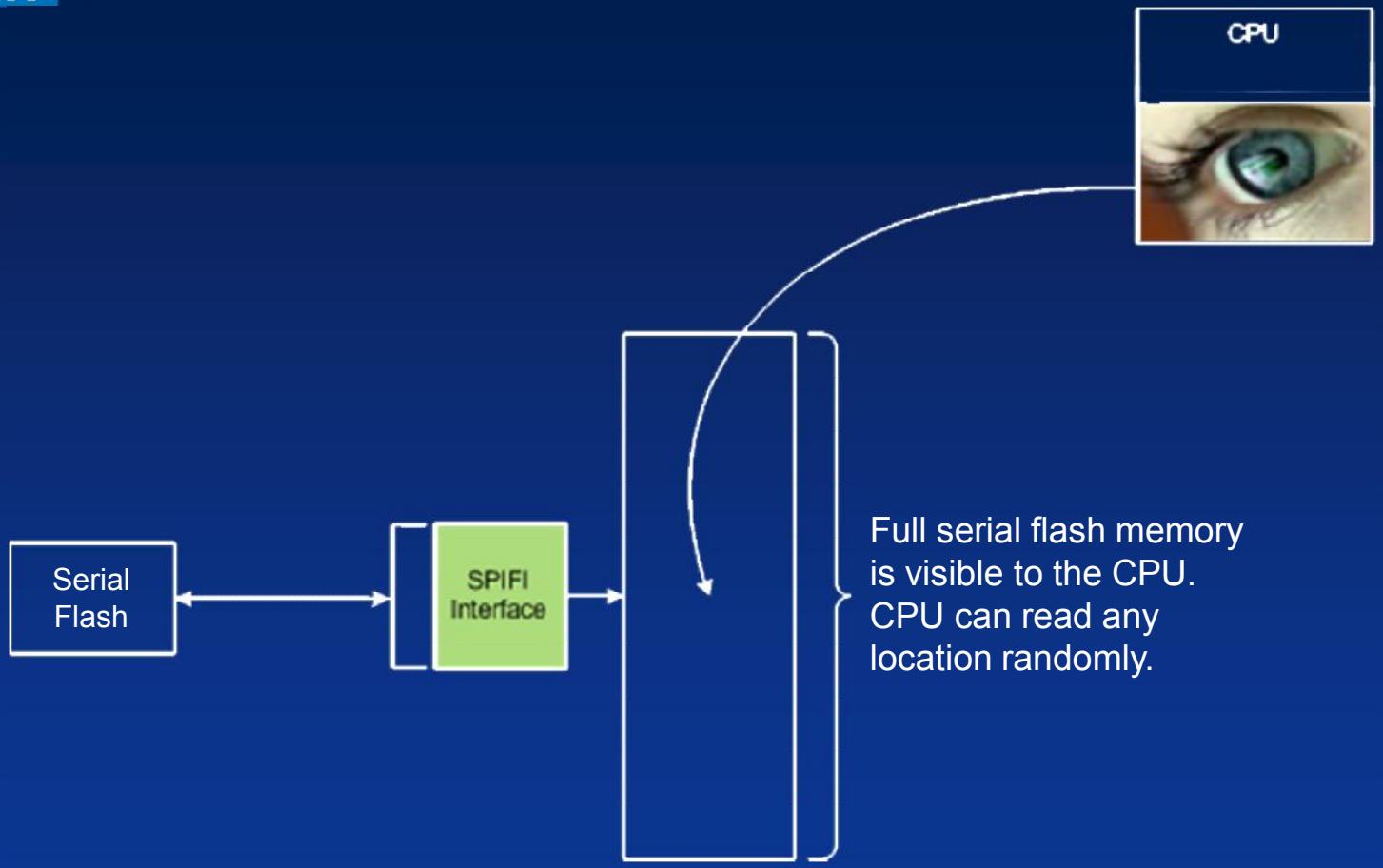


Interface	Mode	Access Time (nS)	Effective Throughput(MB/S)
Parallel	8 Bits	90	11
	16 Bits	90	22
Serial	Single	12.5	10
	Dual	12.5	20
	Quad	12.5	40

Traditional View

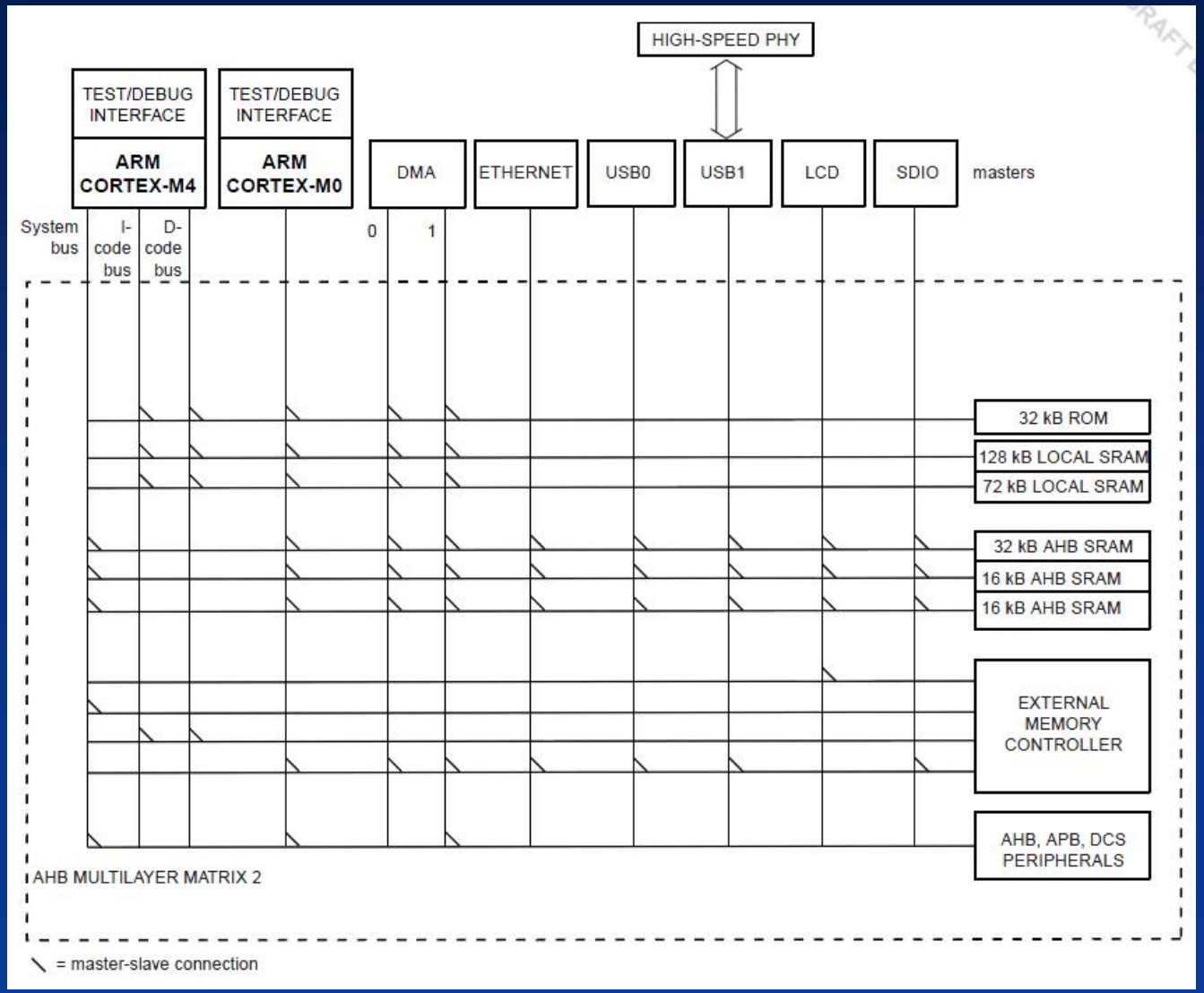


SPIFI View



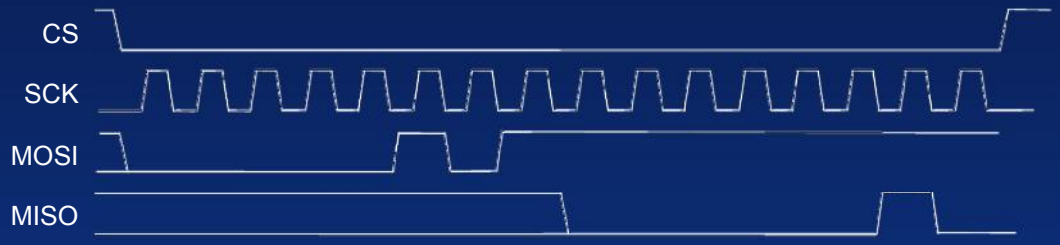
Full serial flash memory is visible to the CPU. CPU can read any location randomly.

Bus Matrix


HIGH-SPEED PHY
TEST/DEBUG INTERFACE
TEST/DEBUG INTERFACE
ARM CORTEX-M4
ARM CORTEX-M0
DMA
ETHERNET
USB0
USB1
LCD
SDIO
masters
System bus
I-code bus
D-code bus
0
1
32 kB ROM
128 kB LOCAL SRAM
72 kB LOCAL SRAM
32 kB AHB SRAM
16 kB AHB SRAM
16 kB AHB SRAM
EXTERNAL MEMORY CONTROLLER
AHB, APB, DCS PERIPHERALS
AHB MULTILAYER MATRIX 2
= master-slave connection

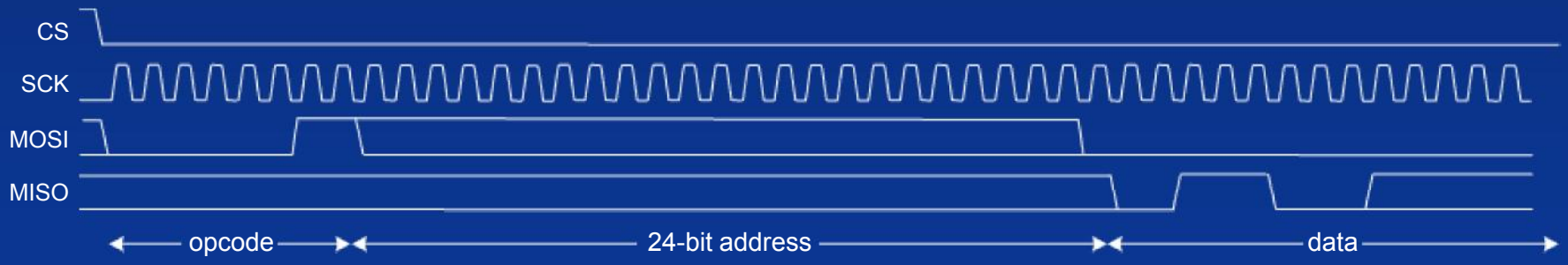
Pin Level Interface

- Most of the 157 serial flashes noted above are SPI-only:



Read Status (opcode 05), input data 02, SPI mode

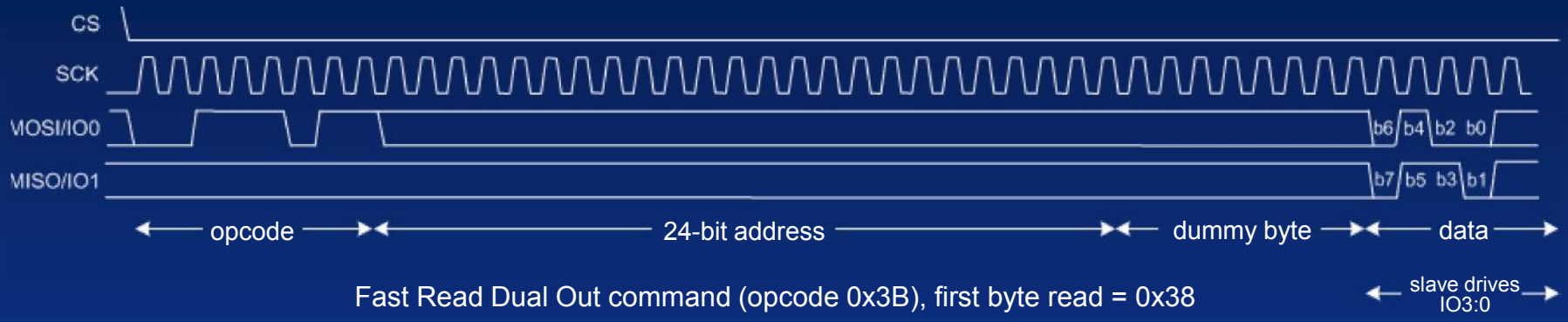
- Most Basic SPI Read command:



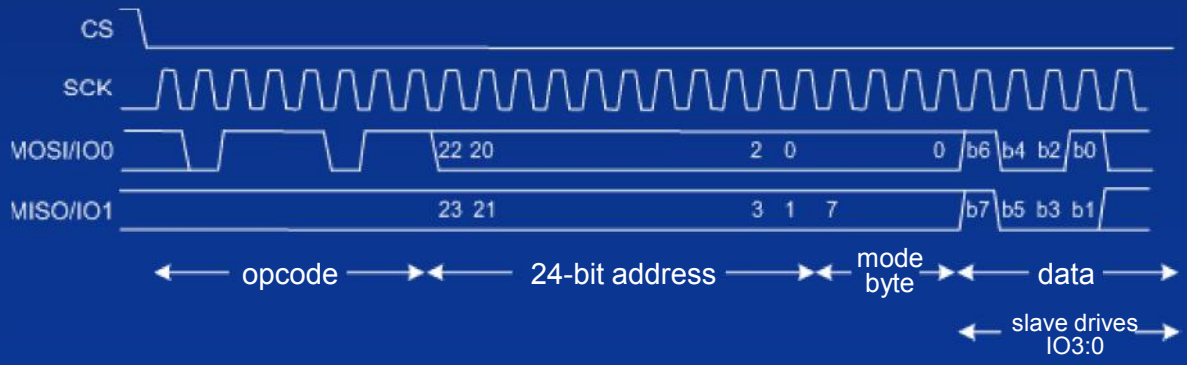
Read Command (opcode 0x03), SPI mode, first byte read = 0x38

Pin Level Interface 3

- Next faster mode is for slave to send read data in dual format

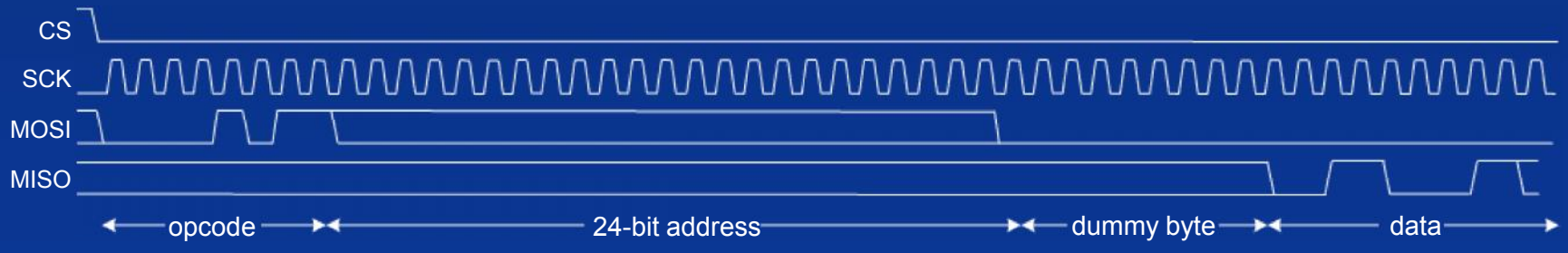


- Next faster mode: master sends the address & mode in dual format



Pin Level Interface 2

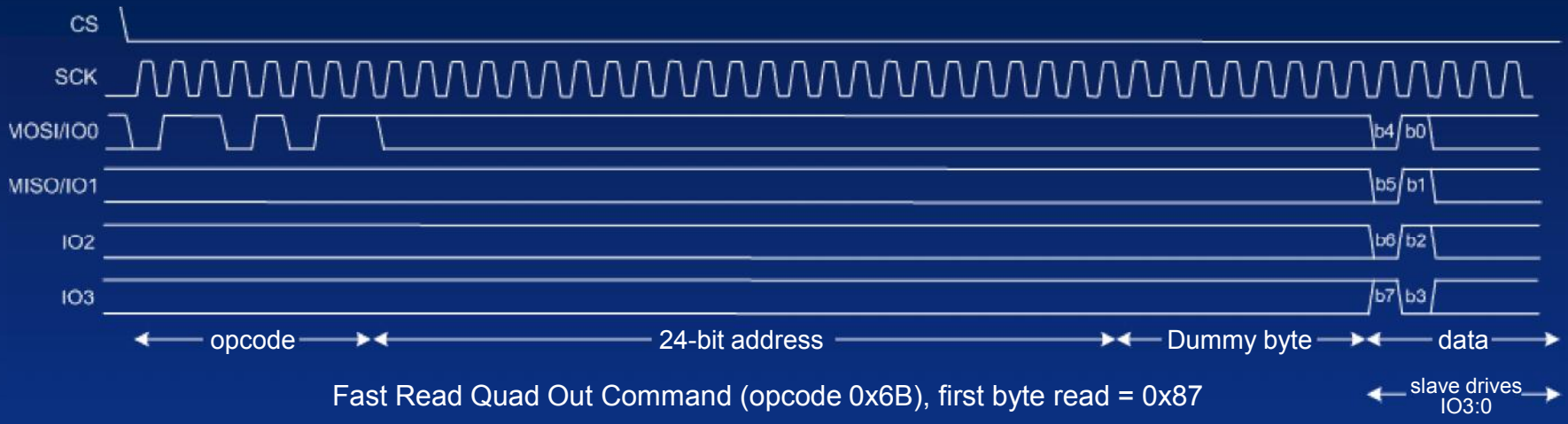
- Note that Read command requires the serial flash to provide data in the clock period after it samples the last bit of the address.
- This is a difficult requirement, and constrains the serial clock rate at which the Read command can be used.
  - Most devices limit Read to 20–50 MHz.
- Fast Read command adds dummy byte between address and data.
  - Allows time for device to get its data pipeline filled and ready.
  - Can be used up to max serial clock frequency of device (50–133 MHz).



Fast Read command (opcode 0x0B), SPI mode, first byte read = 0x31

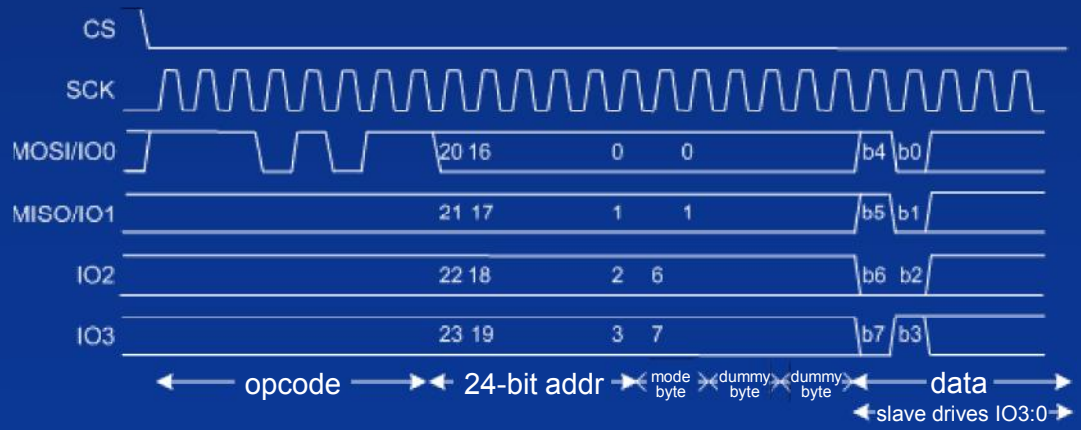
Pin Level Interface 4

- Quad mode adds signals IO3:2; here slave sends data in quad format



Fast Read Quad Out Command (opcode 0x6B), first byte read = 0x87

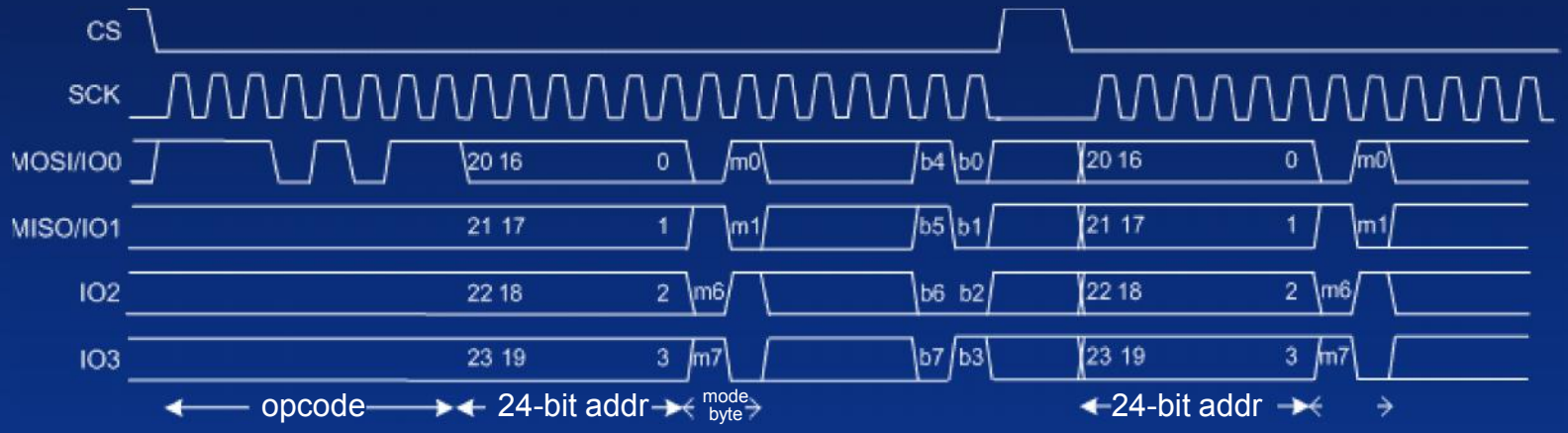
- Here master sends the address, mode, 2 dummy bytes in quad format



Fast Read Quad Out Command (opcode 0xEB), first byte read = 0x38

Mode Byte and No Opcode Mode

- If the mode byte in the Read Dual/Quad I/O command is 0xA5, most serial flashes will not expect the next command to have an opcode.



Fast Read Quad I/O command (opcode 0xEB), mode byte 0xAF sets No Opcode mode for next command

- Next mode byte(s) can be 0xA5, or 0xFF to end No Opcode mode.
- Driver automatically uses no-opcode mode for devices that can do it.
- “No opcode mode” is our term, flash vendors use “continuous read mode”, “XIP mode”

ROM-based Drivers

Advance Information

- **Boot from Quad SPI Flash using SPIFI**
  - Faster than single lane serial flash
  - Boot source selected by pin or NV location
- **Initialization API**
  - Checks what kind of device
  - Writes to control registers for optimal read performance
- **Write API**
  - Block writes
  - Erase
  - Write protection.

SPIFI – Supported Devices

- All NXP's devices with the unique SPI Flash Interface (SPIFI) support all major suppliers of QSPI flash

Supported/Unsupported Devices

- **Three requirements for serial flash include most existing devices:**
  - Read JEDEC ID command
  - Page programming command (byte programming not supported)
  - At least one erase command that is uniform across the whole device
- **Most (all?) of the 17 unsupported devices lack page programming:**
  - Elite F25L004, F25L008, F25L016
  - Eon 25B64
  - SST 25[VW]F512, 25[VW]F010, 25[LVW]F020, 25[VW]F040, 25[VW]F080, 25VF016, 25VF032.
- **157 serial flash devices from 11 vendors meet these requirements.**
- **95 have been successfully tested with the SPIFI driver API.**
- **Most of the untested 62 are old, small, more or less obsolete.**

Thank You