# Emerging Challenges in NAND Flash Technology


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August 10, 2011

# Presentation Agenda

- NAND Flash Market Overview
- Technology Scaling Trend & Forecast
- Technology Scaling Limitation & Hurdle
- Future Technology Development Direction

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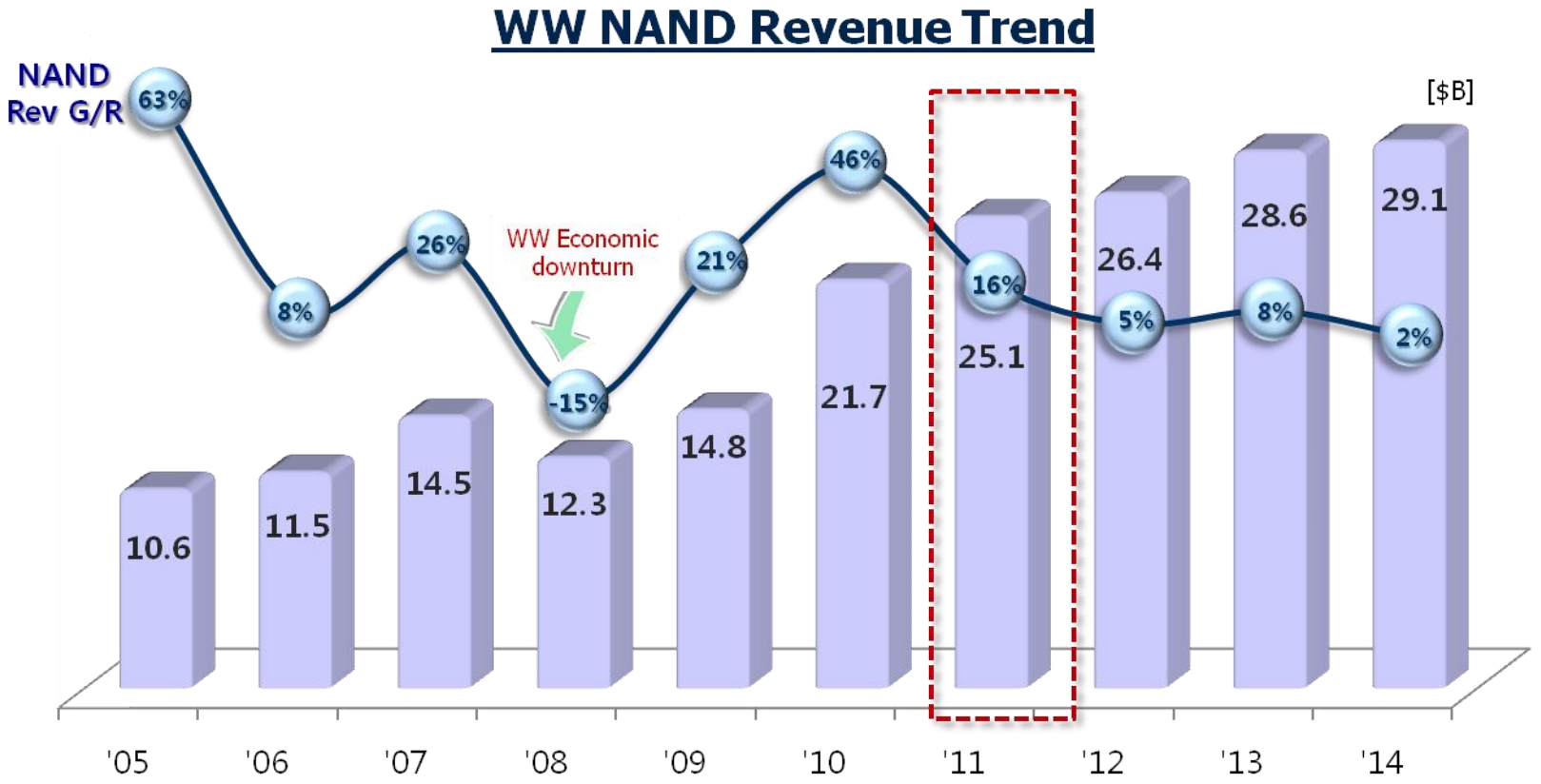
# Market Revenue Forecasting

## Expect continuous NAND market growth; $29.1B in 2014



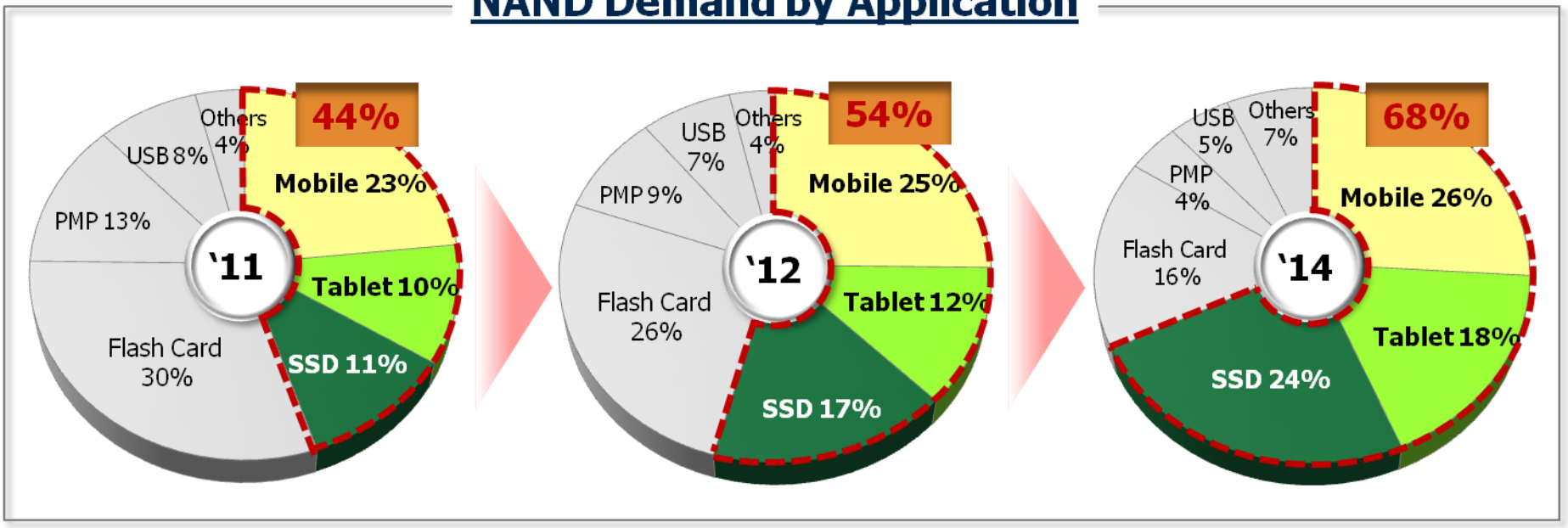

[Source; WSTS2011]



Good memory Great company hynix

# Prospective Application Trend

## Mobile, Tablet, SSD dominate NAND demand in 2011~2014

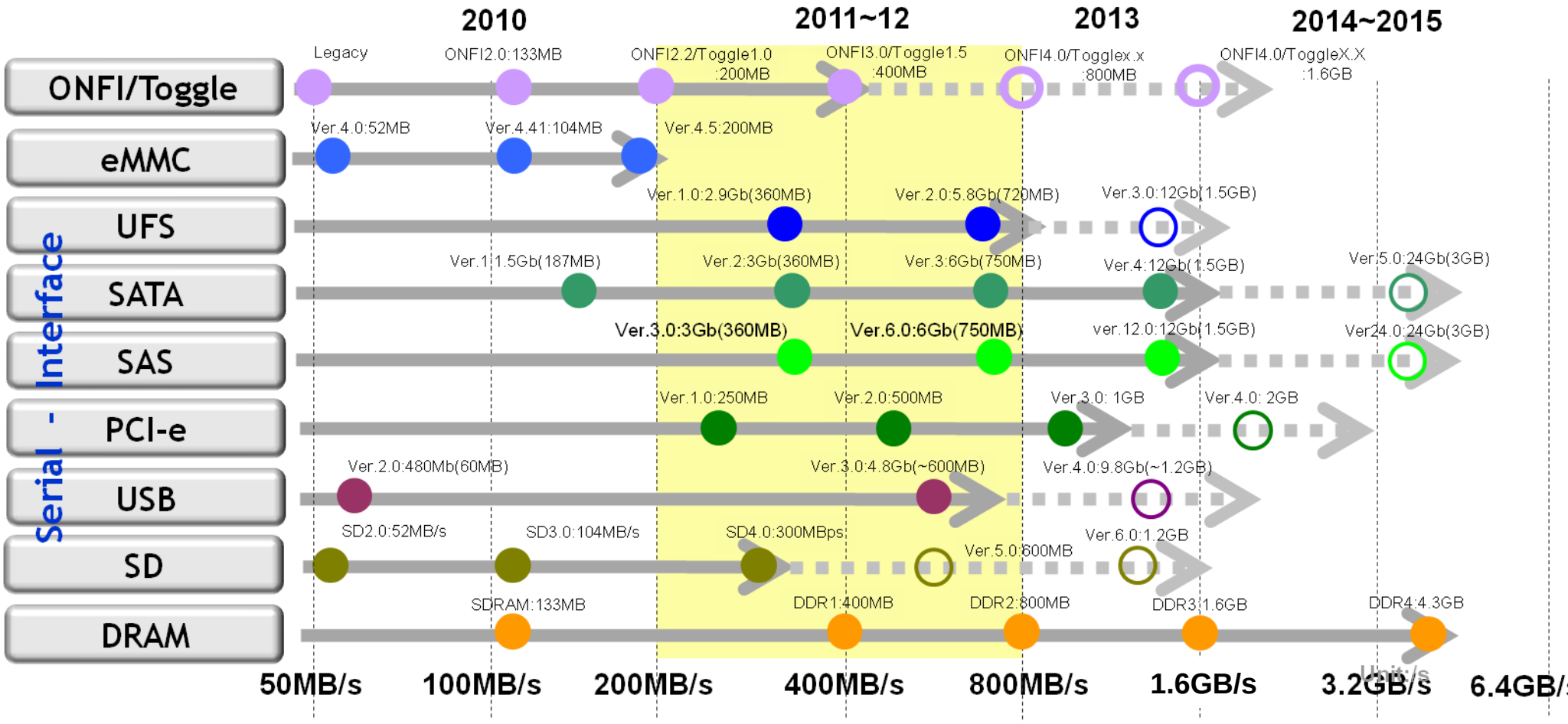



[Source; Hynix Marketing 2011]

# General Market Requirement

- **Low Cost**
  - ✓ *Bit growth*
- **High Performance**
  - ✓ *+ Controller SW solution*
- **High Reliability**
  - ✓ *+ Controller SW solution*

# Standard Interface Trend; *Performance*



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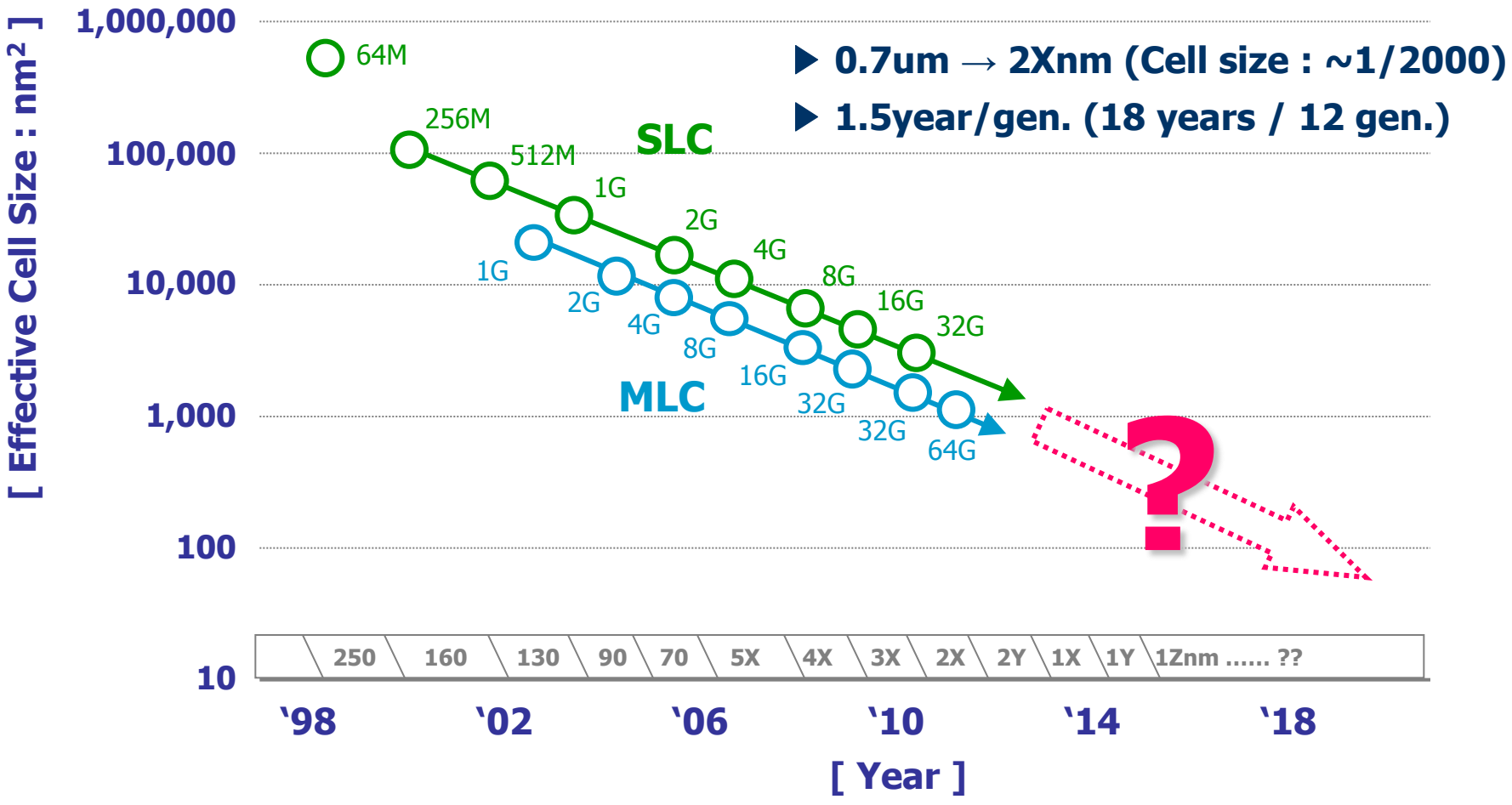
# Further Scaling Solution?

*Conventional FG NAND cell has been scaled down over 18 years.*



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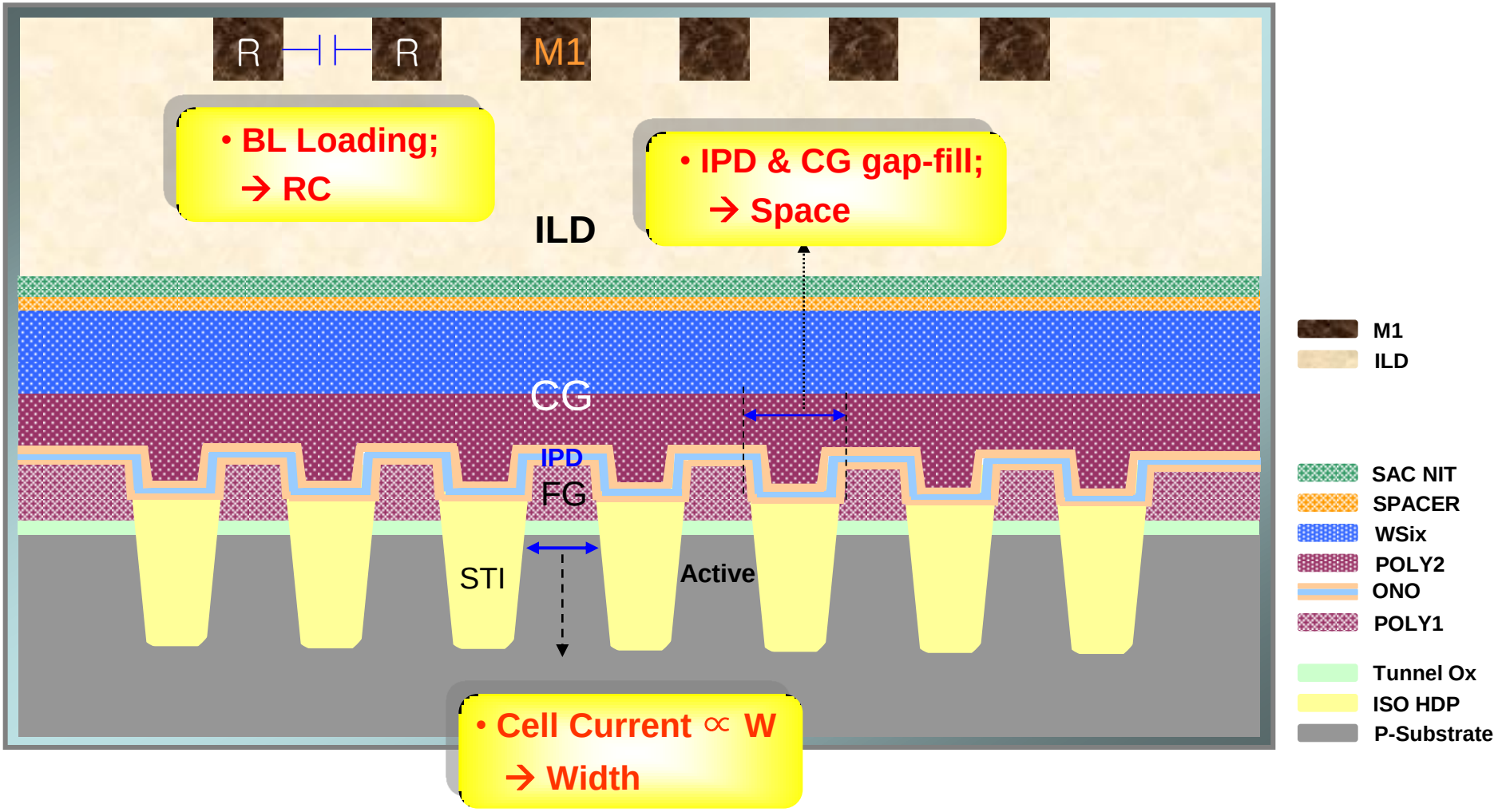
# Scaling Limitation of FG Cell

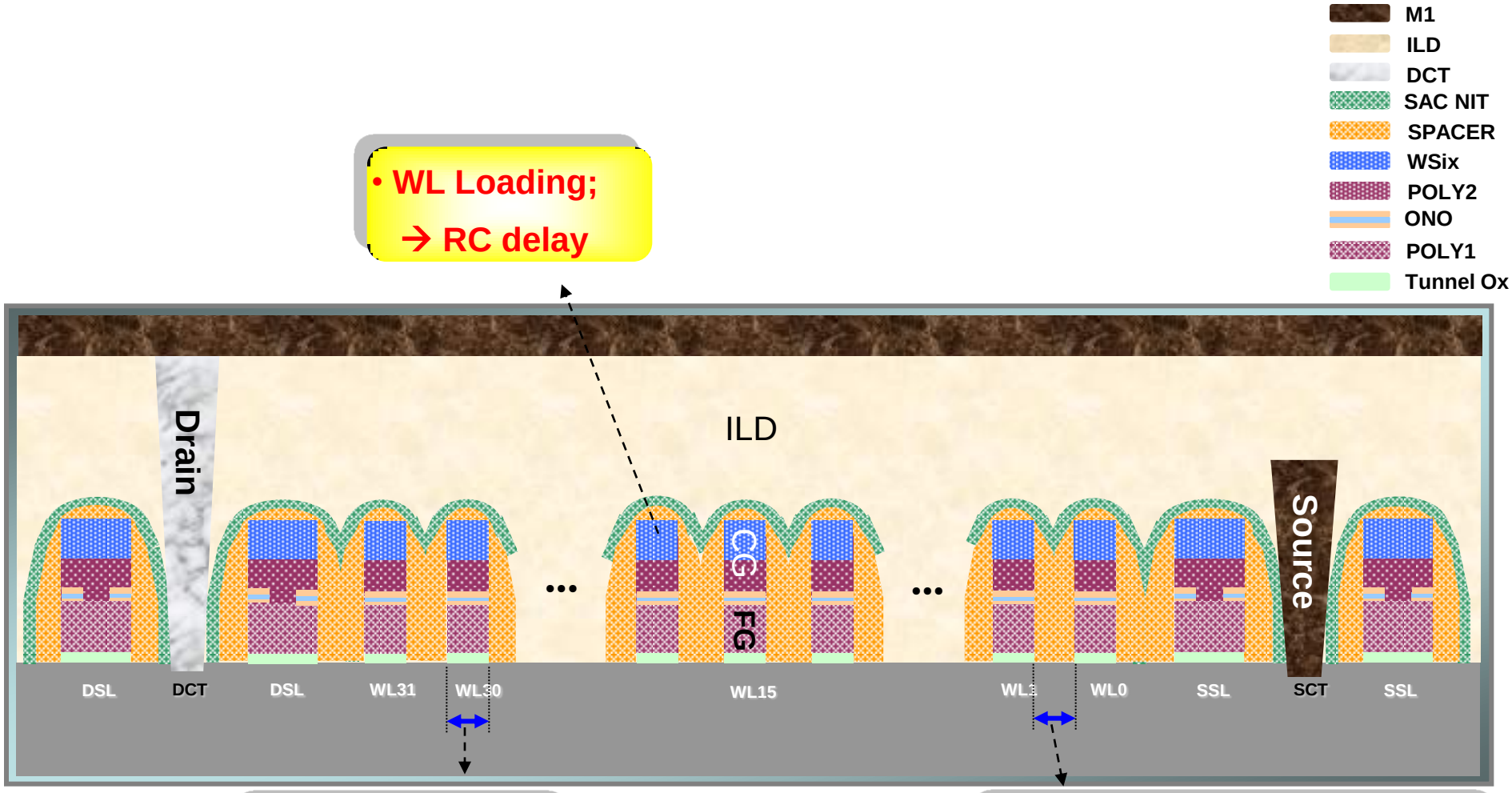
- **Physical Limitation;**
  - ✓ *Patterning*
  - ✓ *Structure formation : FG, CG, IPD …*
- **Electrical Limitation;**
  - ✓ *Interference*
  - ✓ *Capacitive coupling ratio*
  - ✓ *No. of electron in FG*
  - ✓ *Dielectric leakage*

# Cell Scaling Limitation; x-direction

✓ **ASA-FG** Advanced Self-Aligned Floating Gate

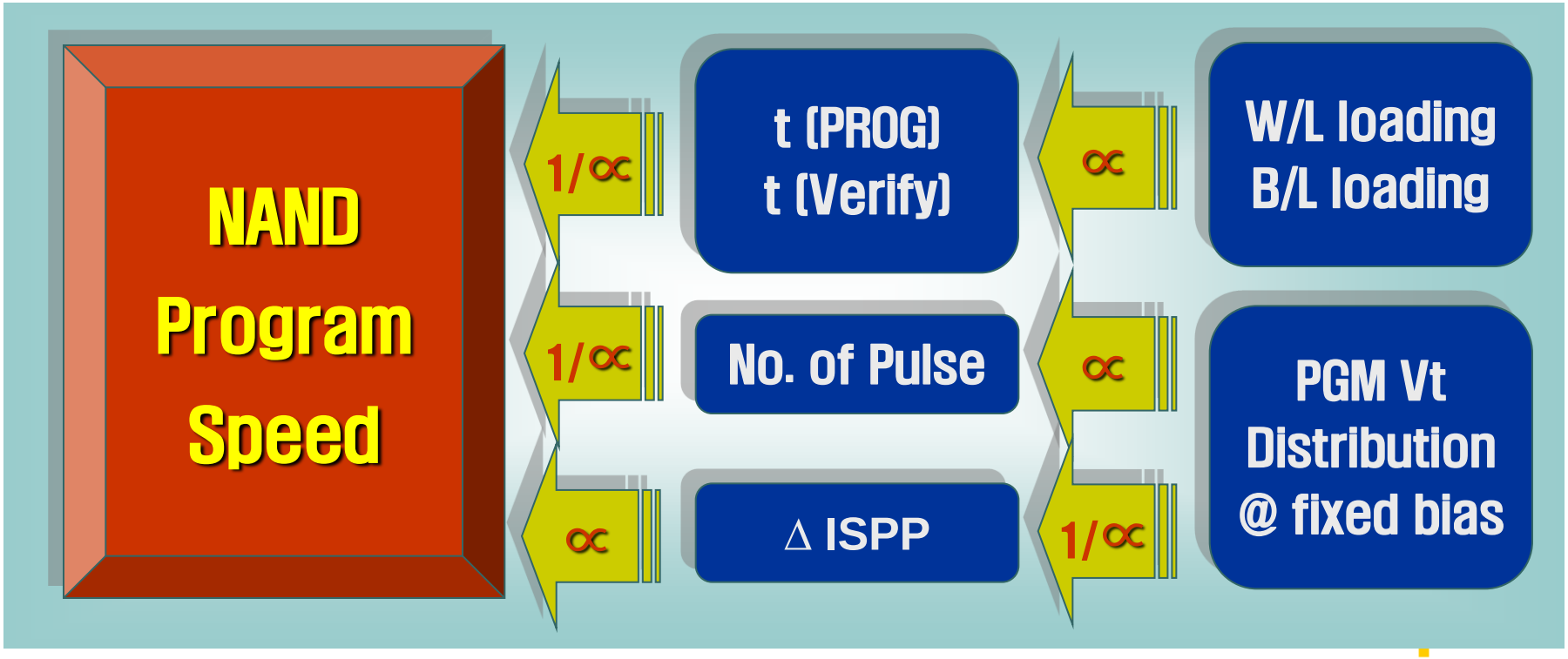


# Cell Scaling Limitation; y-direction



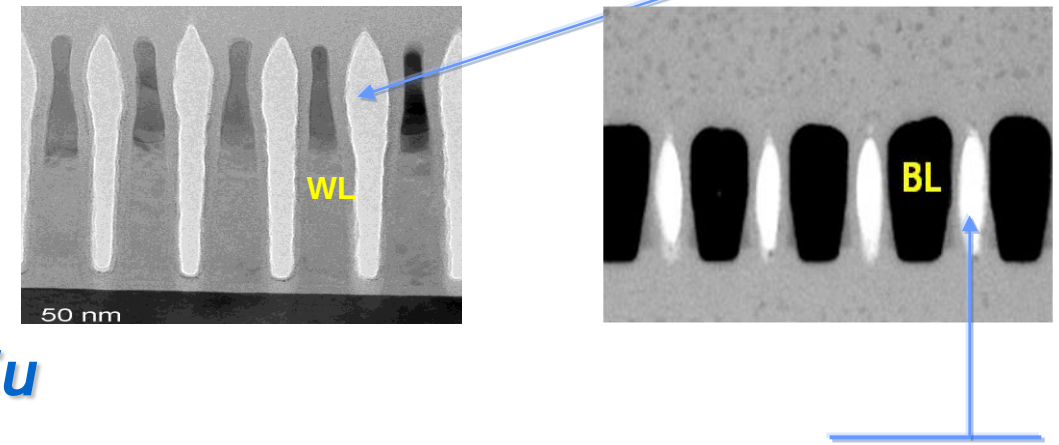
# NAND Program Speed

- **Program Speed = t (PROG + Verify) X N**
  - *tPROG ; unit program & verify time*
  - *N ; no. of ISPP*



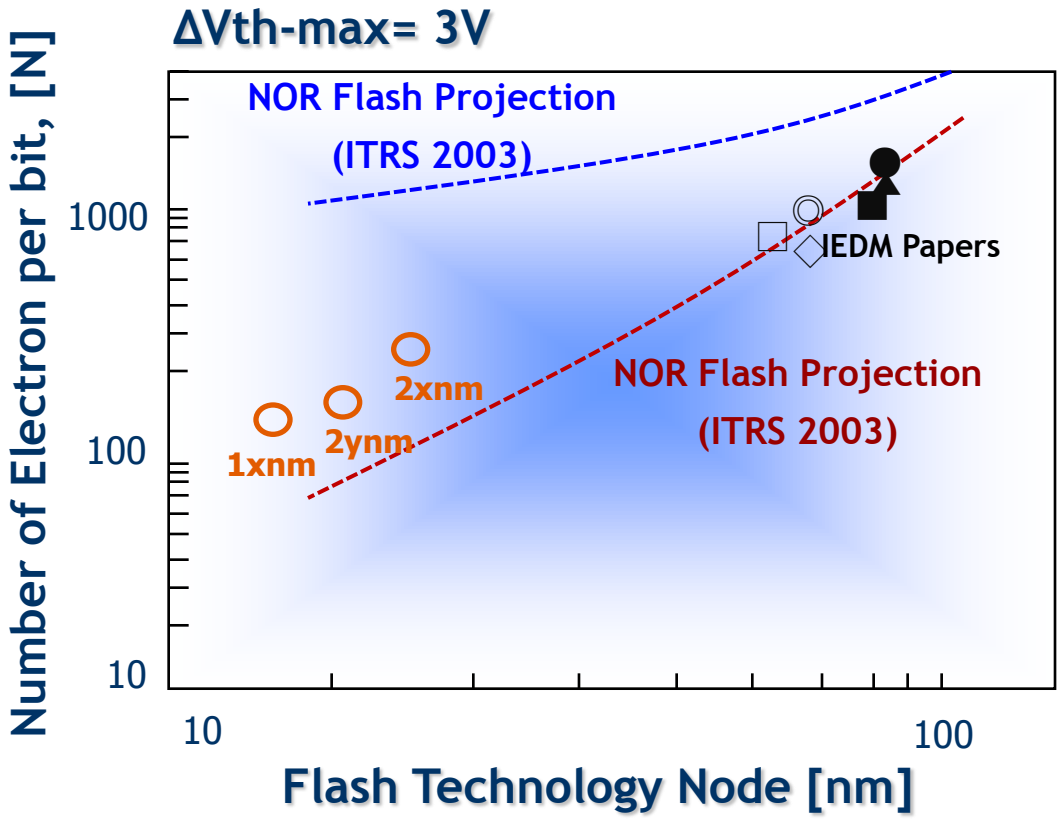
# WL & BL Loading Improvement

- **WL Loading**
  - *Material; Poly- Si → CoSix → W*
  - *WL Space; Vertical Profile → Low-k dielectric → Air Gap*

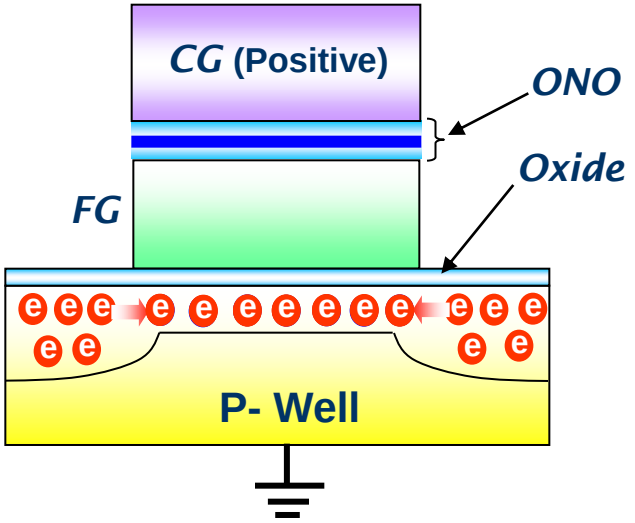



- **BL Loading**
  - *Material; W → Al → Cu*
  - *BL Space; Vertical Profile → Low-k dielectric → Air Gap*

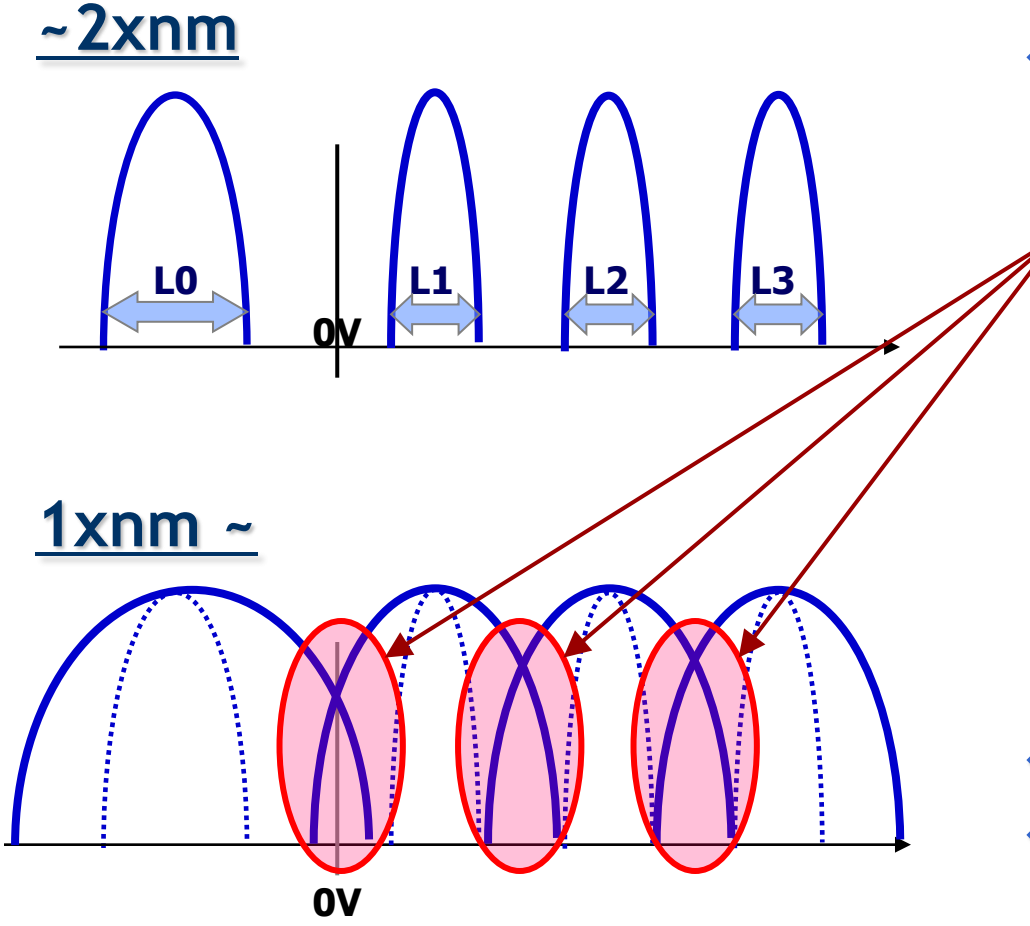
# No. of stored electrons in FG




## Program Operation



# Read Window Margin Solution



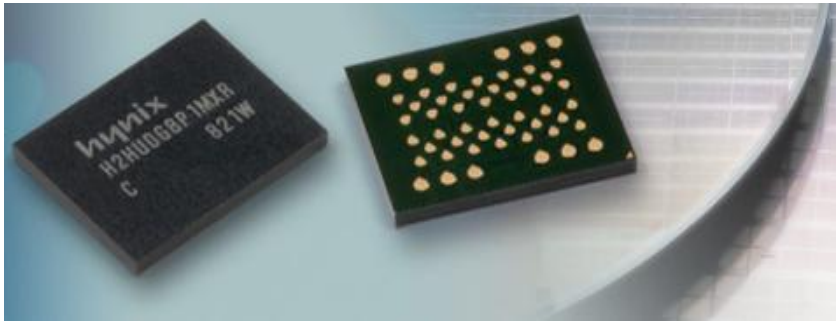

- **Vt Distribution Overlap due to;**
  - ✓ *Process Variation*
  - ✓ *Data Retention Shift*
  - ✓ *FG-FG Interference*

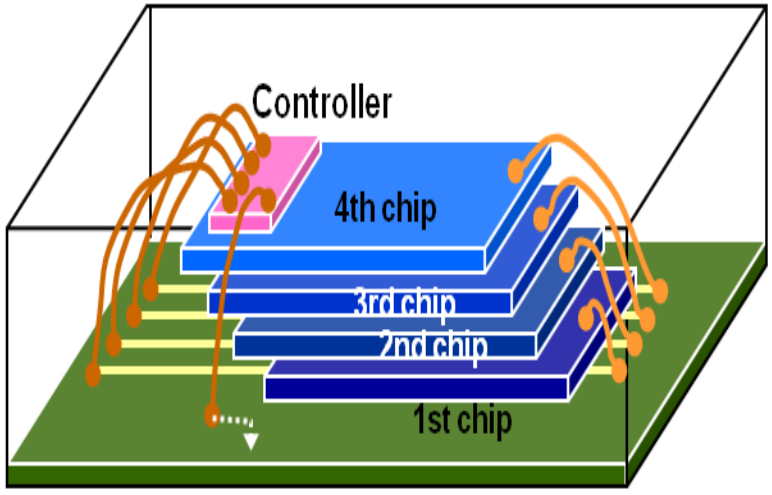
**Controller Solution**

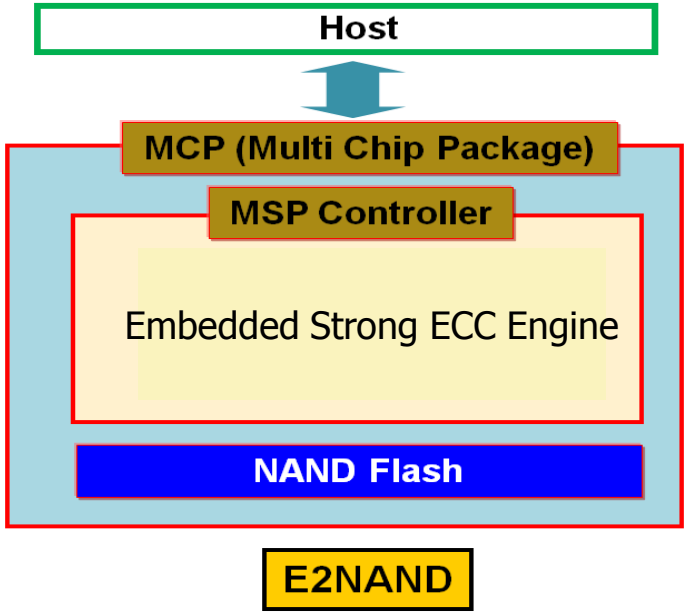
- **Smart Read Algorithm**
- **Strong ECC**

# Enhanced Solution Products

- **Hynix; *E2NAND***
  *[embedded-ECC]*





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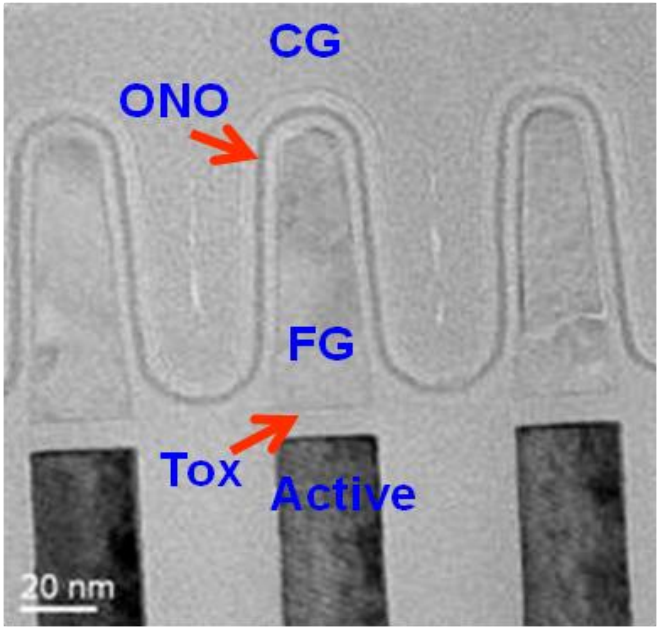
# Planar FG with High-k IPD

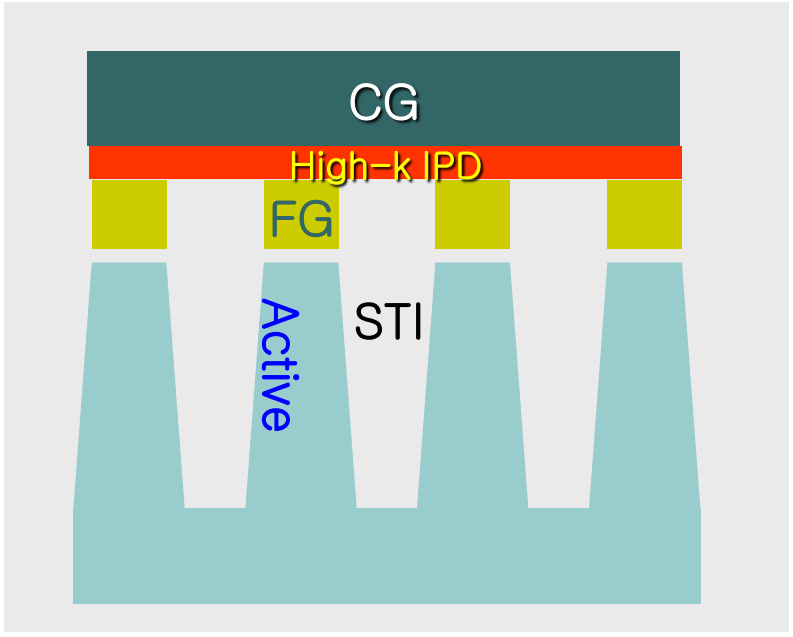
## ◆ CG Gap-filling & Interference

### ❖ Thin FG structure with High-k IPD

✓ *FG vertical scaling*




Conventional FG Structure

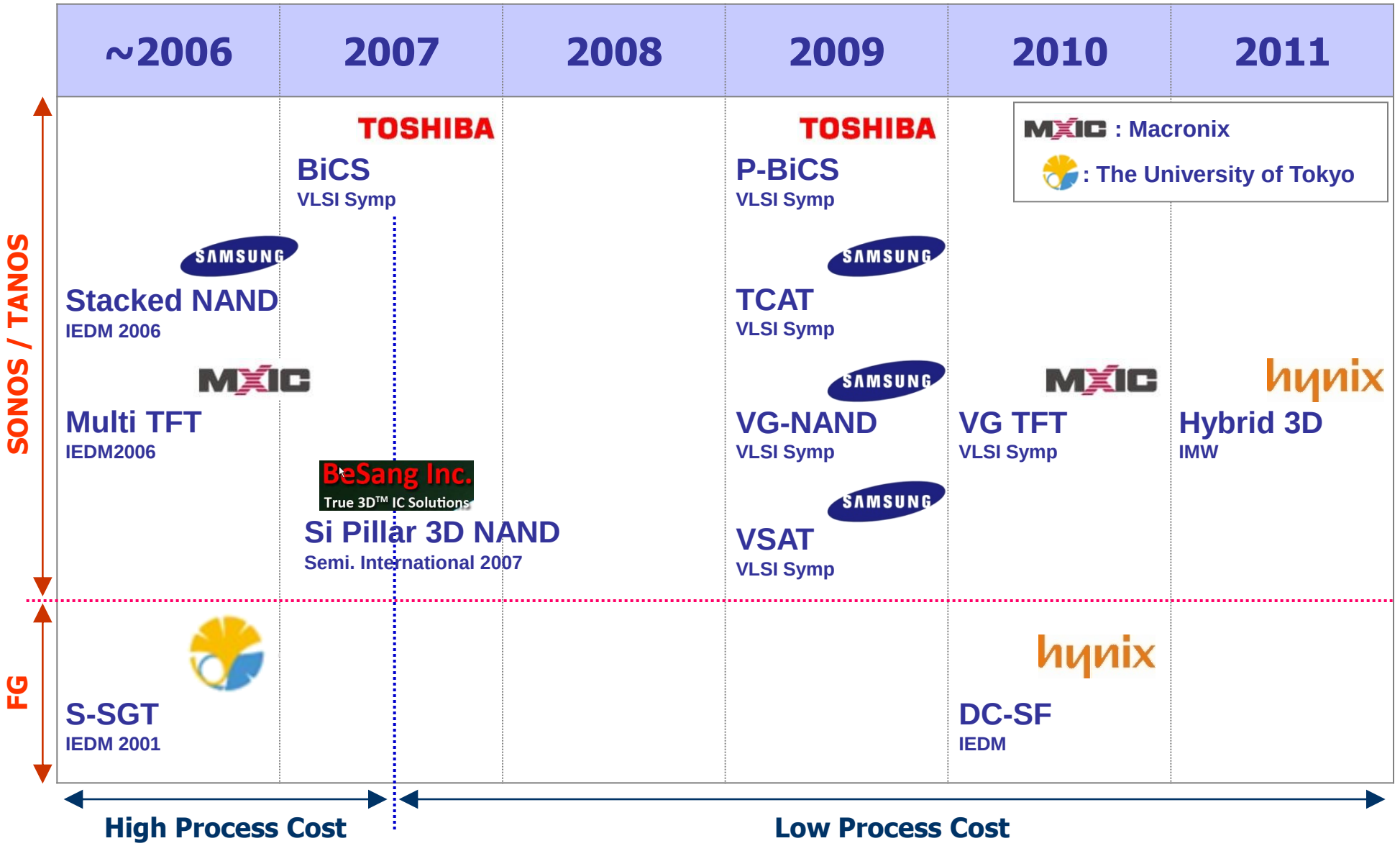



Planar FG Structure

# 3D Cell Structure Approach

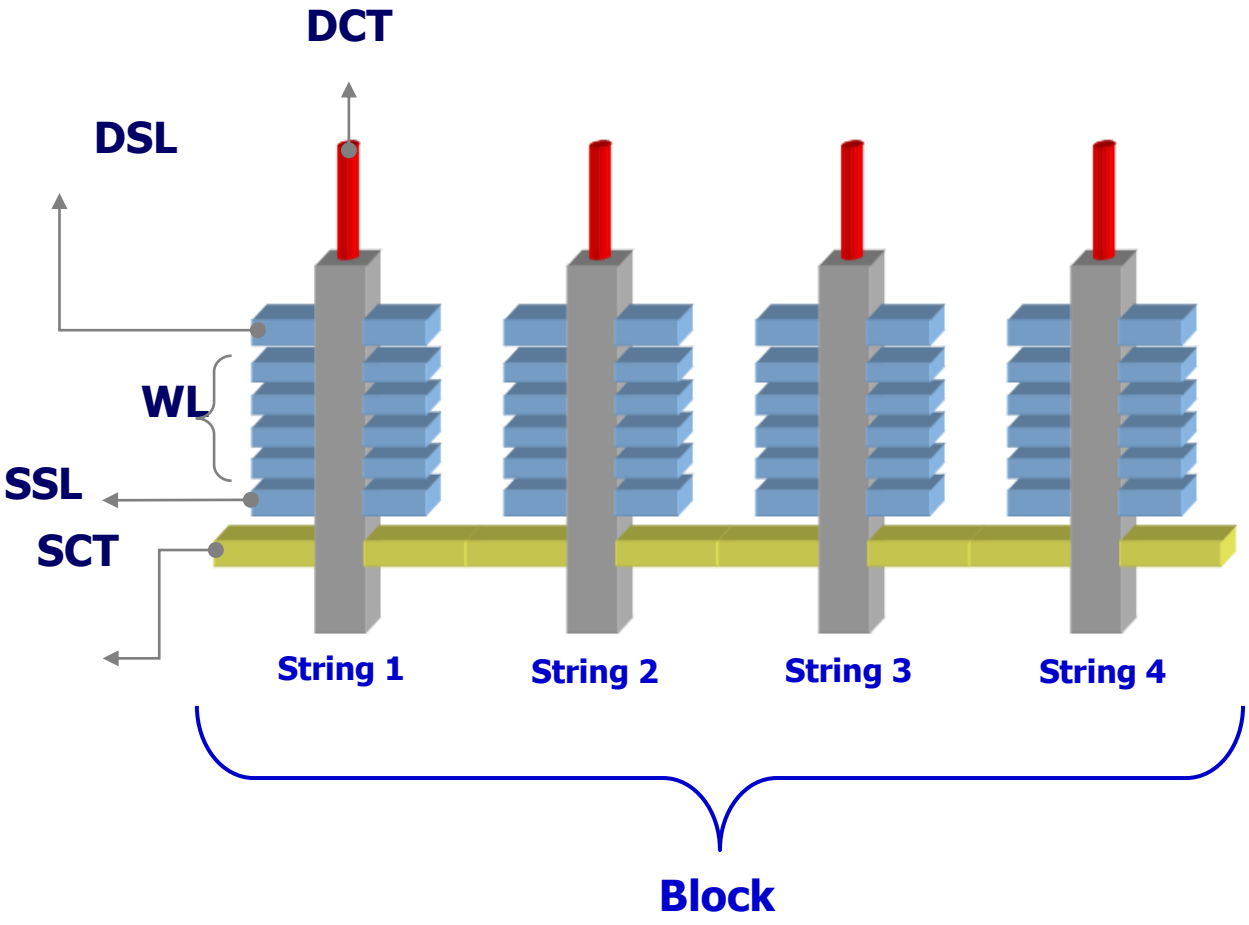
- Stacked 3D with SONOS structure
- Stacked 3D with FG structure
- Si Pillar 3D with wafer bonding technology

# History of 3D NAND Flash



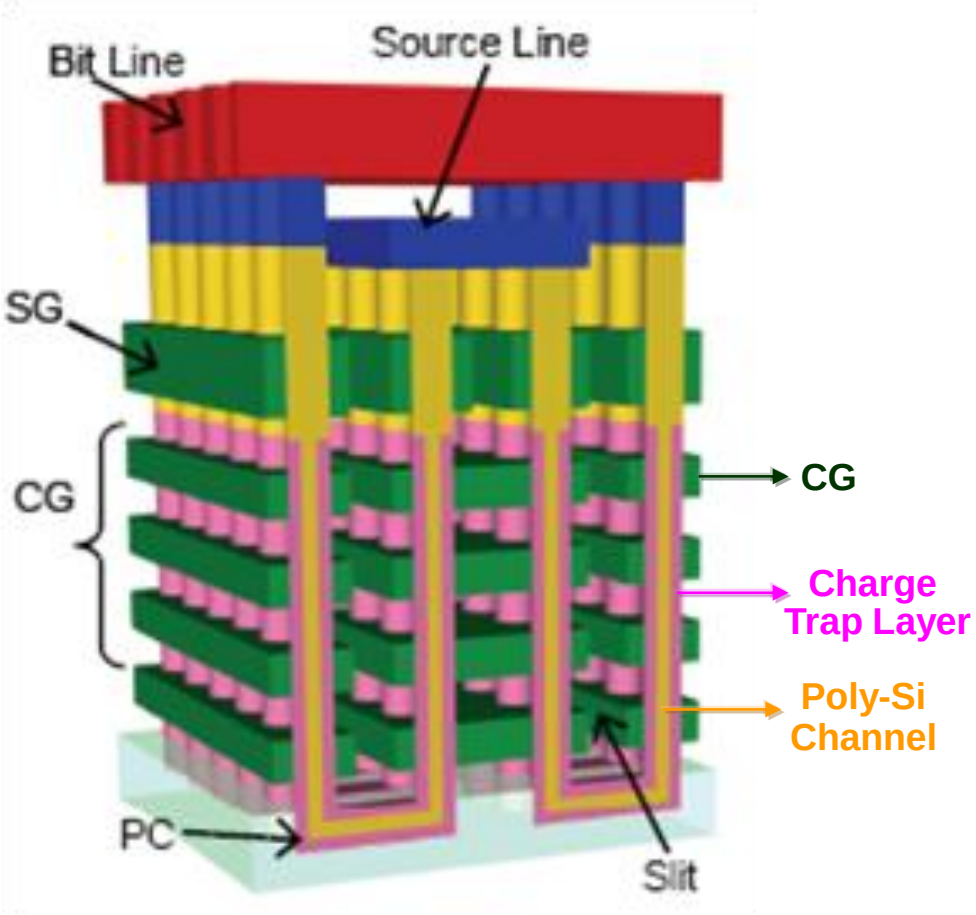
# Stacked 3D NAND Flash Concept

## 3D NAND Cell string



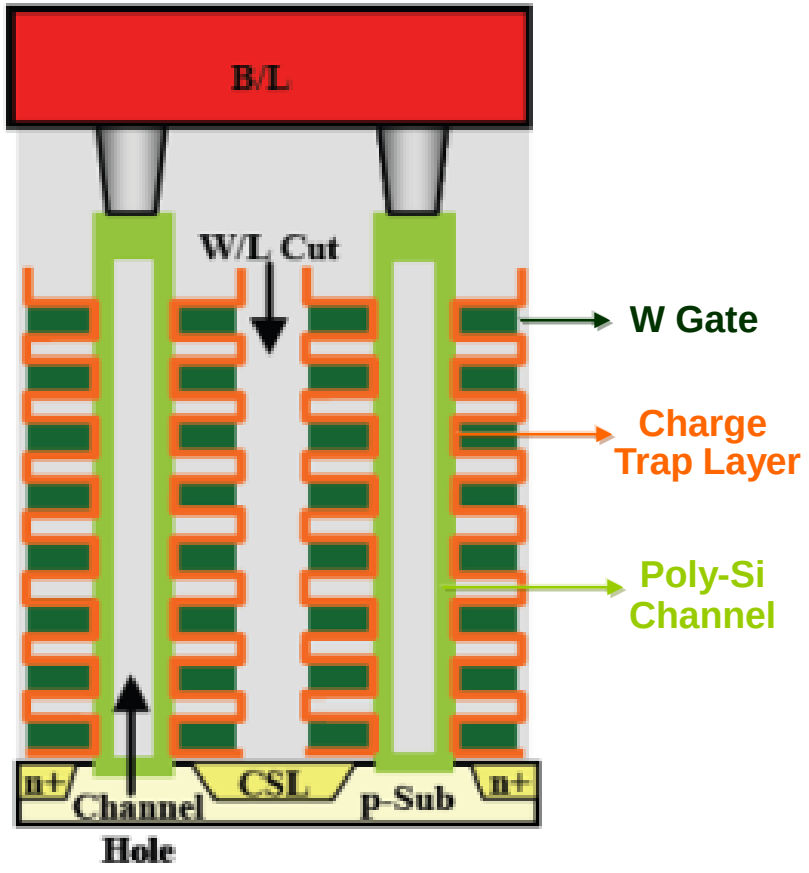
# Stacked 3D Cell Structures

## P-BiCS




[VLSI 2009 by Toshiba]

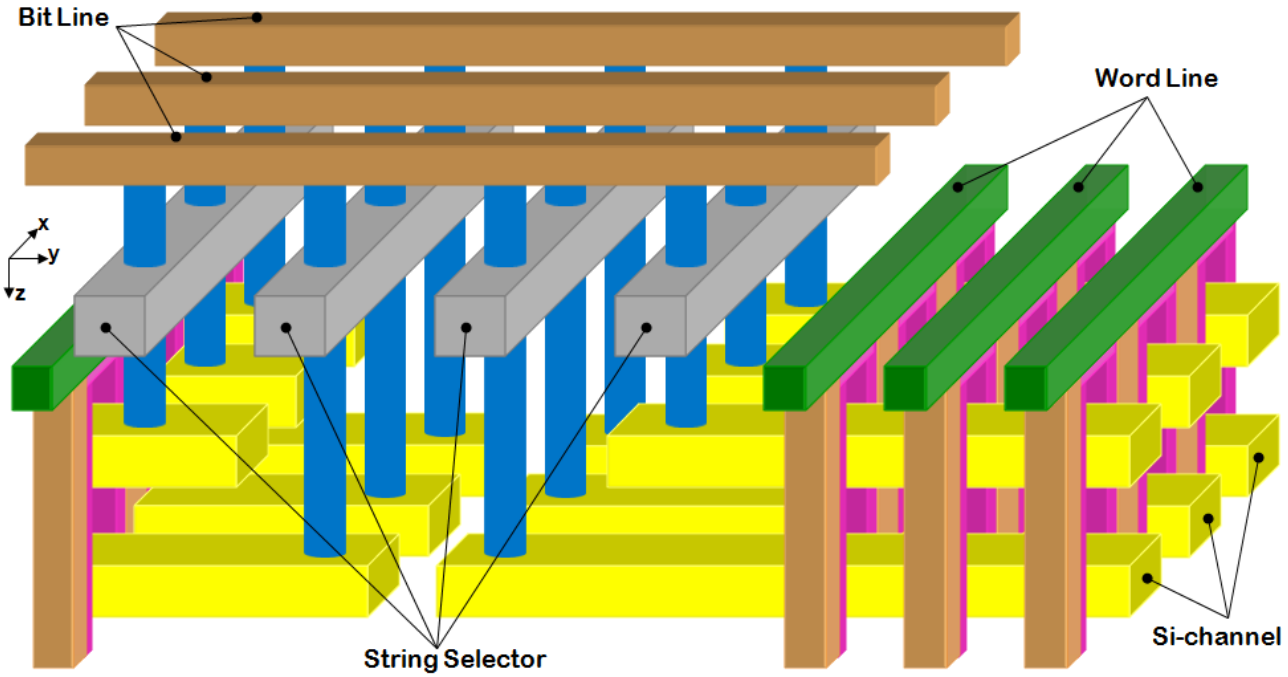
## TCAT




[VLSI 2009 by Samsung]

# Stacked 3D Cell Structures

## Hybrid Stacked 3D



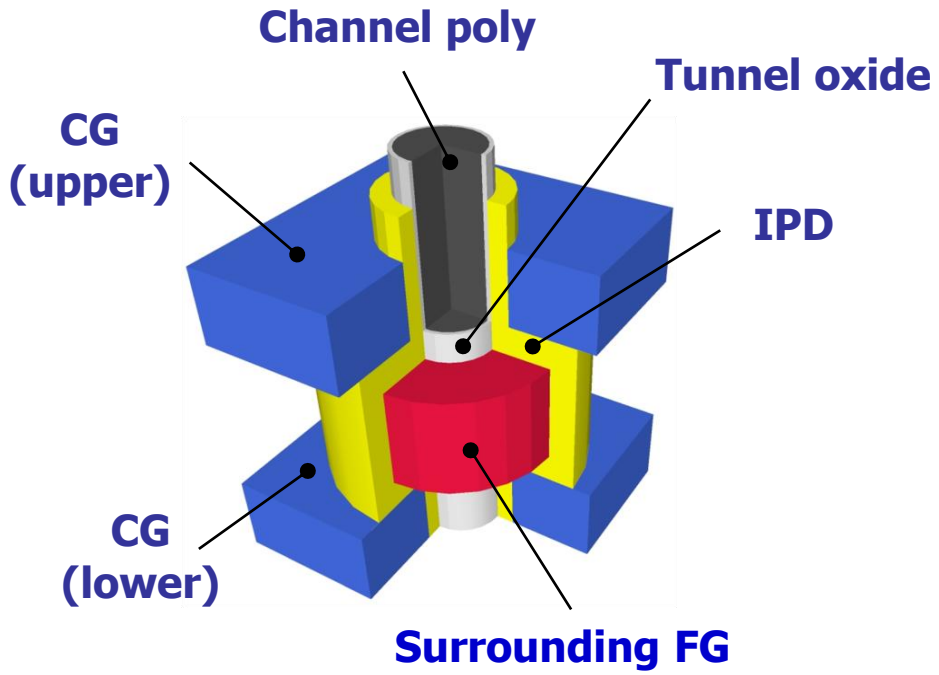

***3D Cell Structure with Horizontal Poly-Si Channel***

**[IMW 2011 by Hynix]**

# Dual CG - Surrounding 3D FG Cell

- New 3D Structure Concept with FG cell
- Surrounding FG is controlled by two control gates.

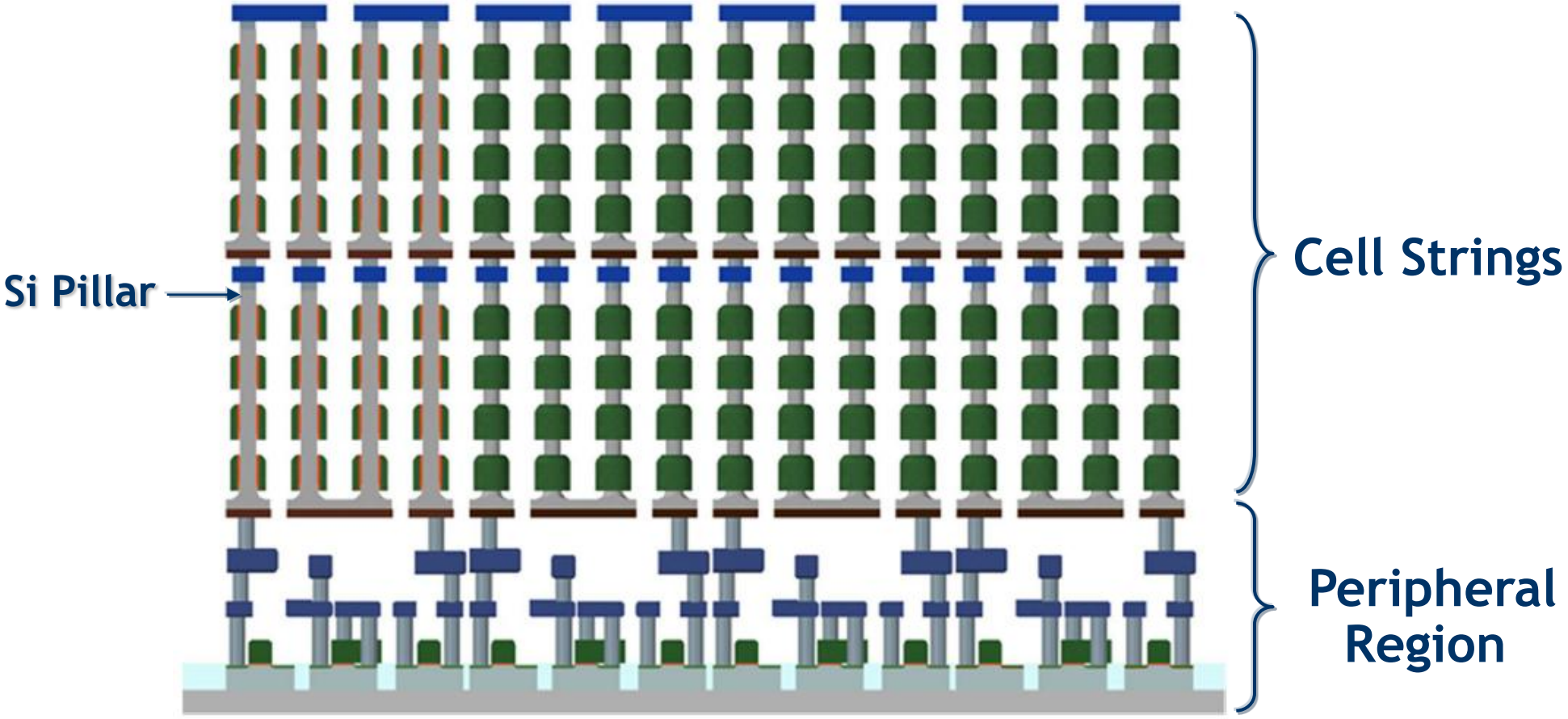
## Single cell




*) Sung Jin Whang, et al, IEDM. 2010, pp.668-671

[IEDM 2010 by Hynix]

# Si Pillar 3D Structure

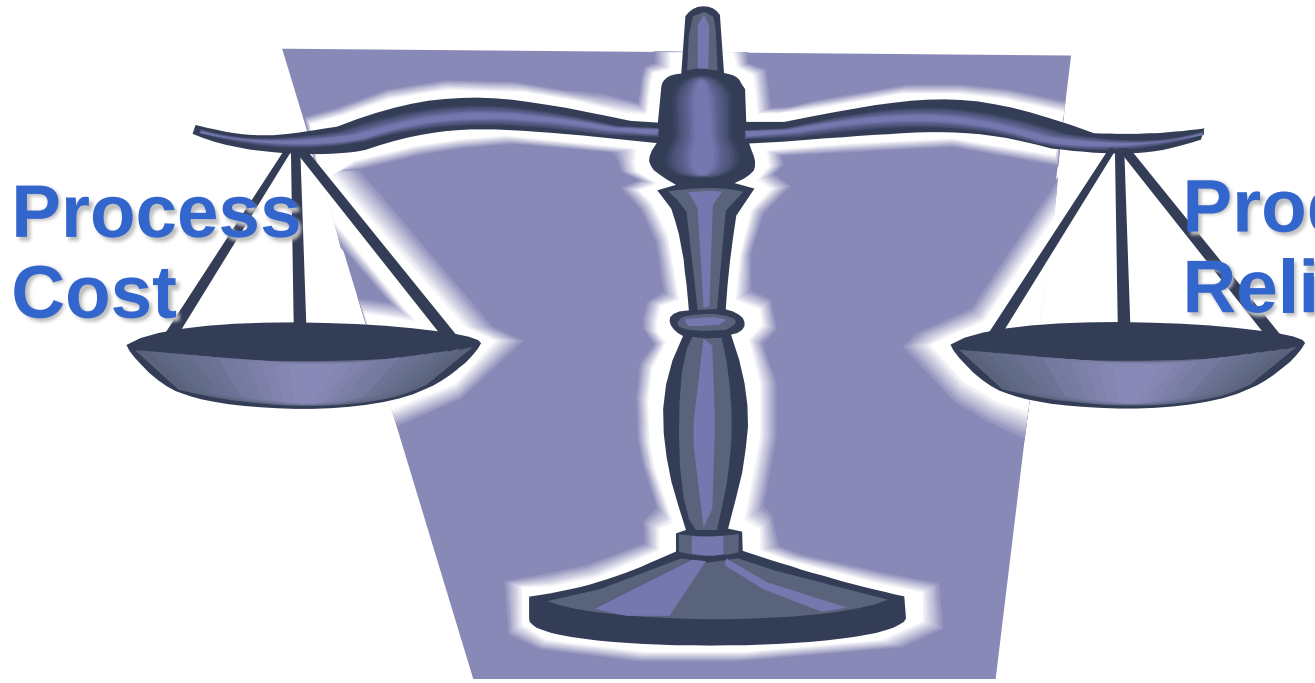



[Semi. International 2007 by BeSang Tech.]

# Future Technology Analysis

| Technology | Strong Points | Weak Points |
|---|---|---|
| Planar FG | Friendly Structure | High-k Dielectric Stability |
| FG-3D | Reliability<br>Small Interference | Scaling Limitation<br>Stacking Limitation |
| Stacked 3D | Low Cost<br>Small Interference | New Materials<br>SONOS Reliability |
| Si Pillar | Approved Materials<br>Scalability | Wafer Bonding Cost<br>SONOS Reliability |

# What are Decision Points ?



# Who is Winner at Post 1x or 1y nm ?

Somebody will find a solution.


Thank you!