400 MT/s NAND Interface Solutions

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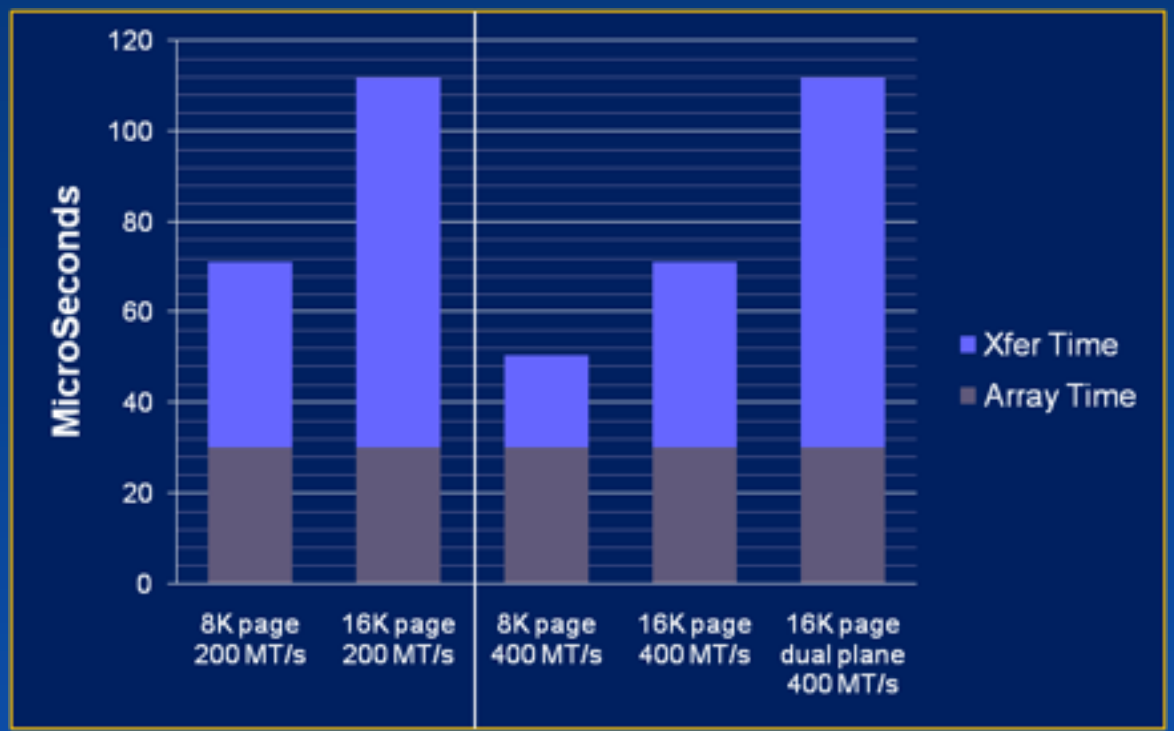
Why 400 MT/s interface speeds?

- NAND architectures are moving towards larger data transfer sizes
- Increased Bandwidth
  - High performance computing applications
    - High density SSDs
    - USB 3.0
- Reduced latency



400 MT/s NAND interface solutions

- ONFI 3.0 NV-DDR2
  - Released March 2011
  - ONFI 3.0 Webinar: www.micron.com/ONFI-3
- Toggle Mode 2.0
  - Announced July 2010
- Work occurring in JEDEC on 400 MT/s
- Reduced CIO
  - Removes features to reduce loading

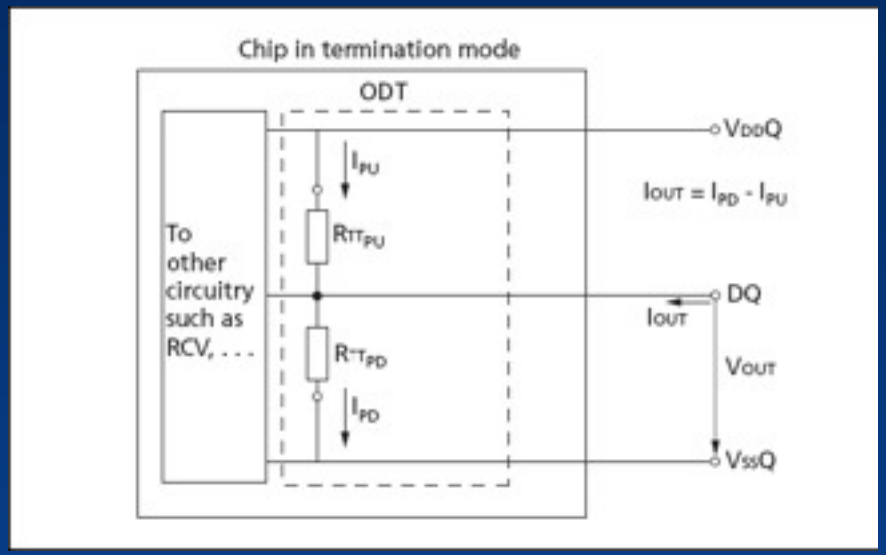
Toggle Mode 2.0

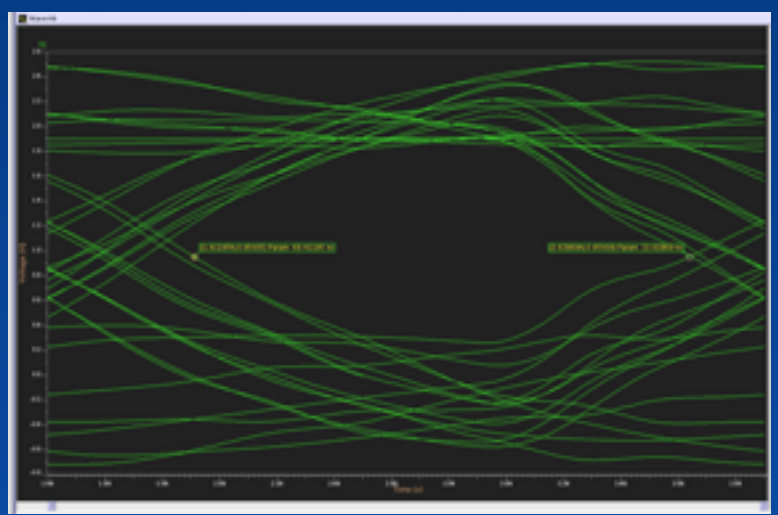
- 400 MT/s DDR interface
  - Compatible with ONFI 3.0 NV-DDR2
- Differential signaling (RE and DQS)
- On Die Termination
- External VrefQ
- Reduced signaling (SSTL_18)
- Warm up cycles

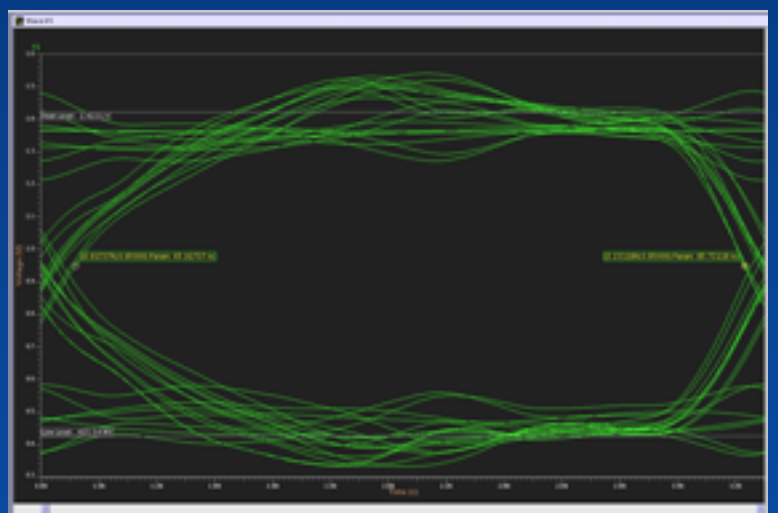
ONFI 3.0 NV-DDR2

- 400 MT/s DDR interface
  - Superset of Toggle Mode 2.0
- Differential signaling (RE and DQS)
- On Die Termination
- External VrefQ
- Reduced signaling (SSTL_18)
- Warm up cycles
- Matrix On Die Termination
- Volume Addressing

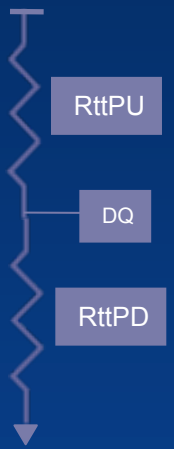
Benefits of termination







Power costs of termination



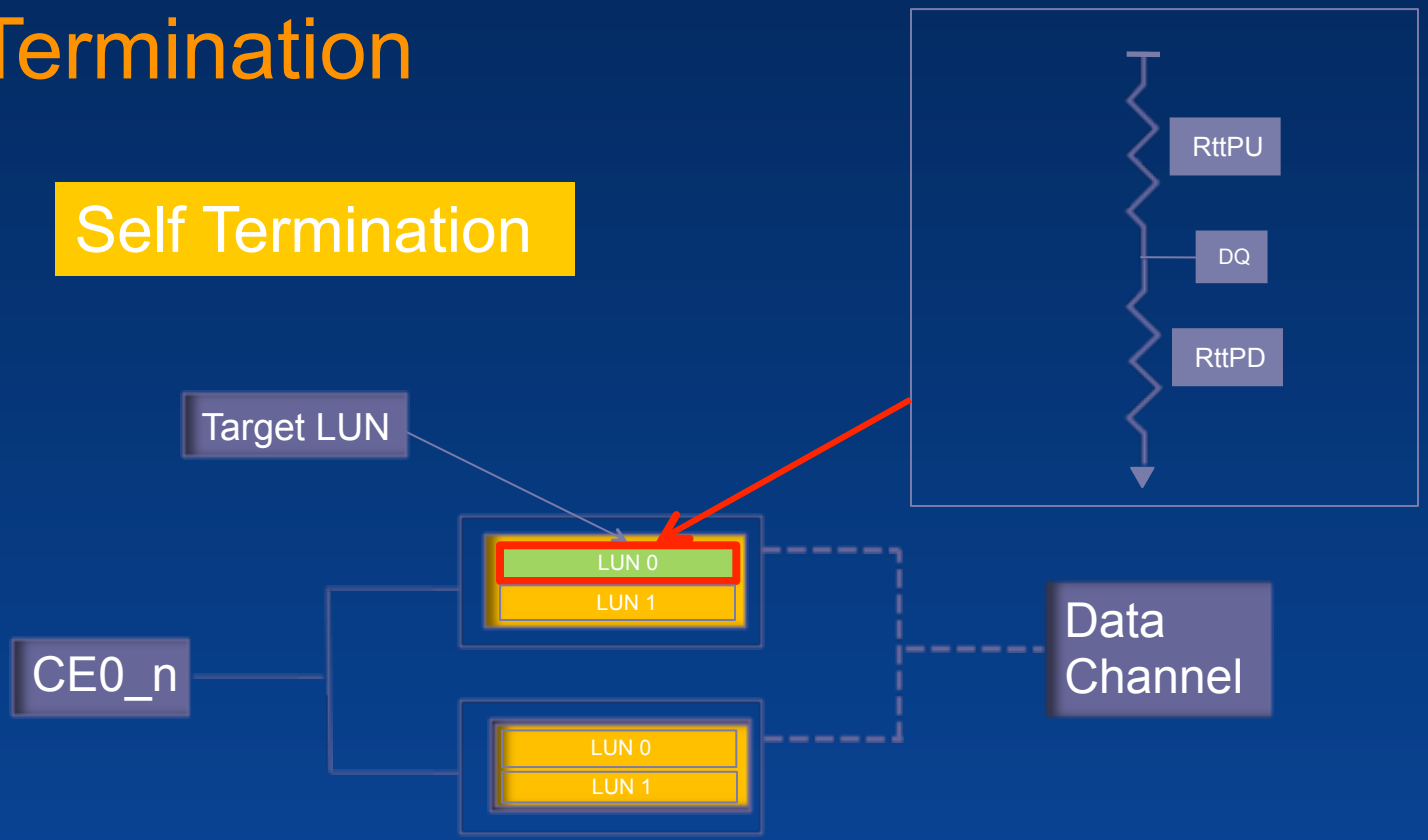
To achieve Rtt of 50 ohms:

RttPU = 100 ohms
RttPD = 100 ohms

With 1.8V VccQ each DQ draws ~9mA

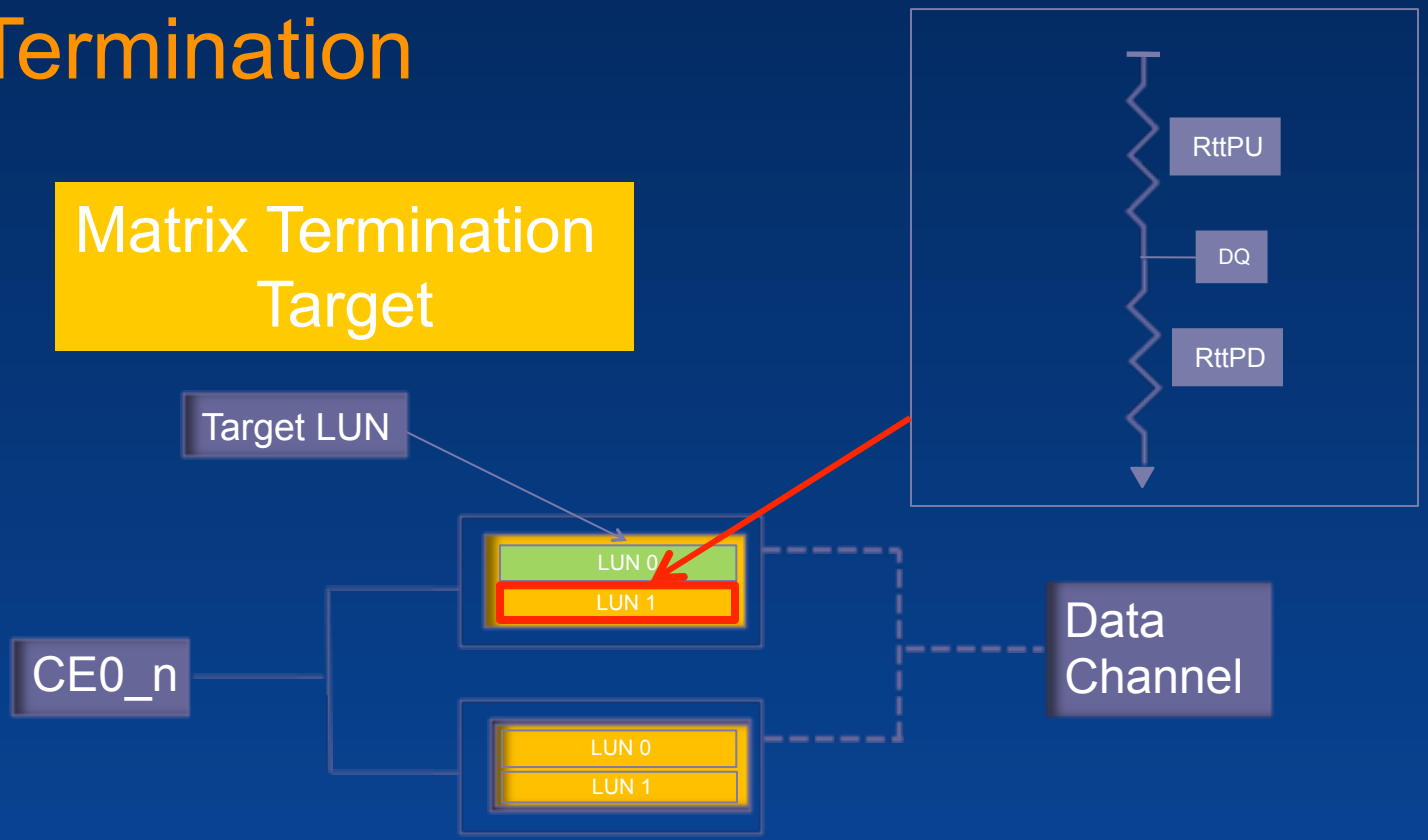
For all terminated signals this amounts to ~160mW per channel to achieve 50ohm termination with linear termination

Matrix Termination vs. Self Termination



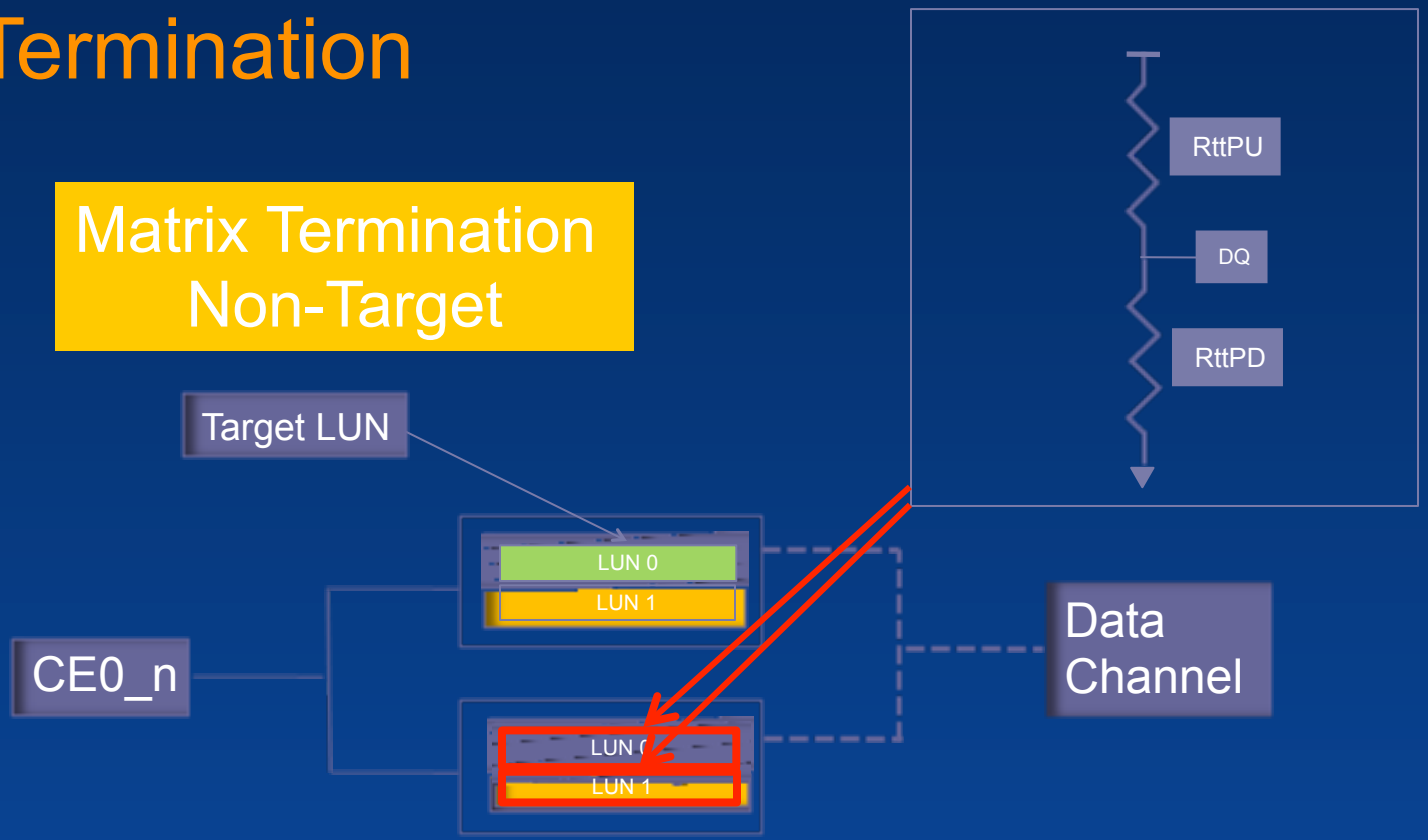
- Target only termination available
- If supported for Reads cannot use output drivers for termination

Matrix Termination vs. Self Termination



- Target or Non-target termination capable
- Supported for Reads and Writes

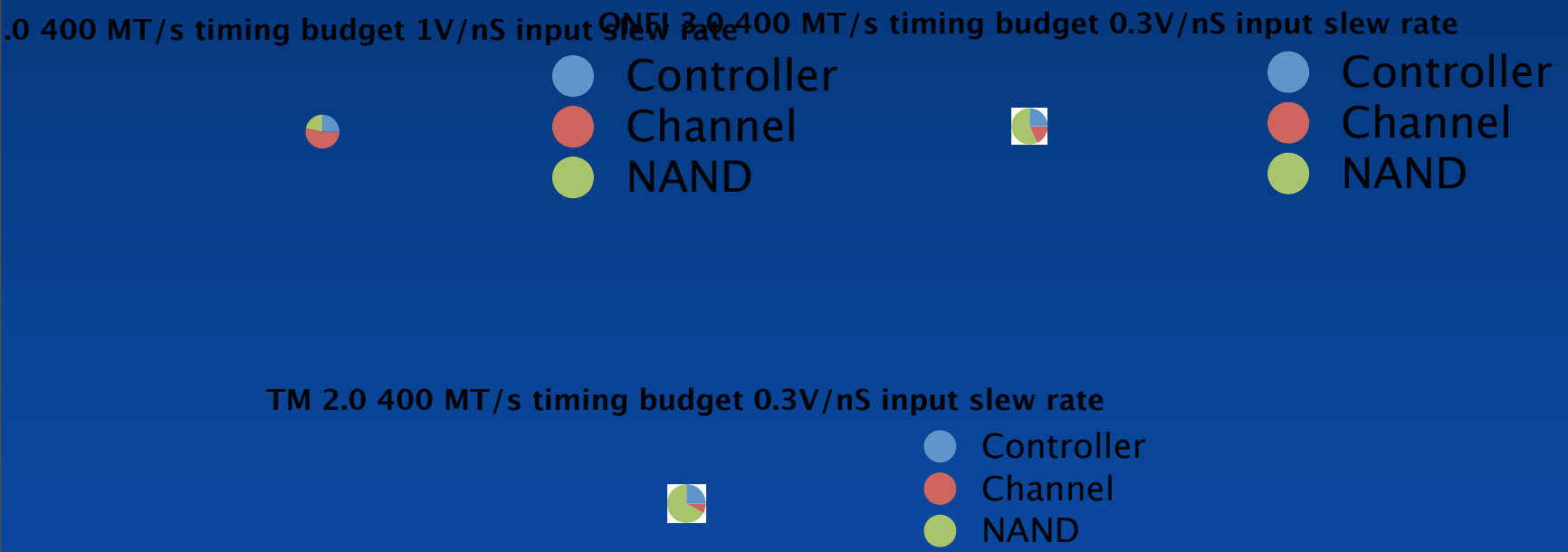
Matrix Termination vs. Self Termination



- Multiple LUNs can be terminators providing a flexible array of termination values and locations

Timing Budget considerations

- With heavy loading and long trace lengths slew rates can become very slow.



Topology considerations